Design of a 2 MSample/s Second Order TFT-based Passive Sigma-Delta Modulator

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Abstract: - Sigma-delta ADCs achieve high resolution using low-precision circuitry and are typically based on switched-capacitor integrators employing high-bandwidth operational transconductance amplifiers (OTAs), which are difficult to realize in TFT technologies because of the intrinsically low carrier mobility of TFT devices compared to CMOS. Passive sigma-delta architectures provide an attractive alternative, requiring only switches, an intermediate amplifier, a comparator, and clock-generation circuitry. This paper presents a TFT-based passive sigma-delta modulator operating at a 2 MSample/s clock frequency with a 5 V supply using Pragmatic flexible-substrate IC technology. High-speed operation is achieved through system-level adaptation together with optimized gated-amplifier and comparator circuits. Circuit simulations demonstrate an SNDR of 87 dB over a 1.953 kHz signal bandwidth. The proposed design operates at a substantially higher clock frequency than previously reported TFT-based sigma-delta modulators, which are generally limited to the kHz-to-sub-MHz range.

Key-Words: - flexible electronics, passive sigma-delta, TFT, data conversion, nFET-only, IGZO, thin film.

Received: March 11, 2026. Revised: May 24, 2026. Accepted: June 12, 2026. Published: September 3, 2026.

1 Introduction

Flexible thin-film transistor (TFT) technologies are useful in low-cost applications, including biomedical and tracking. TFTs have a lower bandwidth than MOSFETs due to their intrinsic lower mobility. MOSFET-based sigma-delta (SD) ADC architectures typically rely on closed loop switched-capacitor integrators based on OTA structures with high open-loop gain and unity gain bandwidth requirements, which are not possible to achieve using TFTs. An alternative approach is the use of passive SD topologies. TFT-based SD designs, which often operate in the sub-MHz range, have been implemented using almost entirely passive components, except for the comparator [1], [2], [3], [4], [5] or by using continuous-time integrators, [6], [7]. Some passive SD designs have been based entirely on switches and capacitors, [8]. Entirely passive SD designs have no amplifiers but require a high-resolution comparator due to the attenuated signal present at its input. In this passive SD approach, a high-value resistance is used together with a voltage source. For sampling intervals much smaller than the RC time constant, the combined voltage source and resistance act as a current source, which charges a capacitor, and thus the resulting voltage provides the integration function. This paper presents the necessary building blocks for a TFT-based high-speed passive SD design and utilizes an intermediate amplifier between the integrators. The main system parameters, including first and second integrator time constants and the intermediate amplifier gain, have been scaled from the values presented in a previous CMOS passive SD design [6]: this previous work involved extensive numerical optimization of the various system parameters with respect to SNR and stability and is not within the scope of this paper. The novel aspect of this paper is in the adaptation of the overall topology to TFT circuit implementation, as well as in the design of the actual TFT building blocks. The primary contributions of this work lie in the TFT implementation of the circuit building blocks and their adaptation to high-speed operation.

2 Implementation

2.1 System-Level Modulator Model

The linearized block diagram of the passive second-order SD, shown in the block diagram of Figure 1 (Appendix), consists of two discrete-time integrators,

a clocked comparator, and a D-flip-flop (FF) for signal quantization and the generation of the feedback signal. In this case, the integrators are approximated by passive RC circuits whose time constant is much higher than the clock period, thus acting as an almost constant current source charging a capacitor. The integrator coefficients α_n and β_n, for the respective integrator stage n, depend on the chosen RC time constant in relation to the integration time T_i and are given by [6]:

$$\alpha_n = \frac{T_i}{(RC)_n} \; and \; \beta_n = 1 - \alpha_n \quad (1)$$

Ideal integration is approached when α_n approaches 0 ($\beta_n \rightarrow 1$), but this will also result in an increased attenuation in the signal path. The coefficient G_{Av} represents the gain of an intermediate amplifier introduced between the two integrators to compensate for signal attenuation inherent in the passive SD architecture, while G_{comp} represents the linearized gain of the comparator. The feedback ratios G_{fb1} and G_{fb2} are set by the feedback reference voltages $VREFP_n$, $VREFN_n$, and are given by:

$$G_{fbn} = \frac{VREFP_n - VREFN_n}{V_{dd}} \quad (2)$$

The resulting signal transfer function (STF) and noise transfer function (NTF) are given by:

$$STF(z) = \frac{G_{Av}G_{comp}\alpha_1\alpha_2 z^{-1.5}}{1+A_1z^{-1}+A_2z^{-2}} \quad (3)$$

$$NTF(z) = \frac{z^{-0.5}\left[(1-\beta_1 z^{-1})(1-\beta_2 z^{-1})\right]}{1+A_1z^{-1}+A_2z^{-2}} \quad (4)$$

where the coefficients A_1 and A_2 are given by:

$$A_1 = G_{fb2}G_{comp}\alpha_2 - \beta_1 - \beta_2 \quad (5)$$

$$A_2 = G_{comp}\alpha_2\left(G_{fb1}G_{Av}\alpha_1 - G_{fb2}\beta_1\right) + \beta_1\beta_2 \quad (6)$$

For $|STF| = A_{SD}$, where A_{SD} is the closed-loop signal gain of the SD modulator, the comparator will operate with a mean value of G_{comp} given by:

$$G_{comp} = \frac{A_{SD}}{G_{Av}\alpha_1\alpha_2} \quad (7)$$

Furthermore, for a low-pass SD, $A_1 = A_2 = 0$ and therefore the feedback ratios must be set to:

$$G_{fb2} = \frac{G_{Av}\alpha_1(\beta_1+\beta_2)}{A_{SD}} \quad (8)$$

$$G_{fb1} = \frac{{\beta_1}^2}{A_{SD}} \quad (9)$$

2.2 System Architecture

The corresponding top-level implementation of the second-order passive SD modulator architecture is shown in Figure 2 (Appendix). The SD modulator consists of switches (SW1-SW16), integration resistors (R1-R8), integration capacitors (C3, C4, C7, C8), common-mode capacitors (C1, C2, C5, C6), an intermediate voltage amplifier (Av-Stage) and a comparator. The switch design necessitates that one side (denoted Vin) of the switch is connected to a voltage source with a low-impedance output. The SD modulator operates using a clocking system with two non-overlapping clock phases (P1, P2), having voltage levels of 0 V and 5 V. P1BST and P2BST are clock signals coincident with P1 and P2, respectively, but have a higher voltage swing of 0 V to 7 V, which is necessary for the correct operation of the switches. Signals P1Q_BST and P2Q_BST are similarly high-swing logic signals obtained from the logical AND operation of the comparator output Q with the clock phases P1 and P2, respectively. Similarly, signals P1QB_BST and P2QB_BST are high swing logic signals obtained from the AND operation of the comparator's complementary output QB and P1, P2.

Integration for the first integrator stage occurs during phase P1: during this phase, SW1, SW2, SW5/6, and SW8/7 are turned on. Integration for the second integrator stage occurs during phase P2: during this phase, SW9, SW10, SW13/14, and SW16/15 are turned on. Voltages $VREFP_1$ and $VREFN_1$ set the feedback ratio for the first stage, while $VREFP_2$ and $VREFN_2$ set the feedback ratio for the second stage. In this case, $VREFP_1$ = 3.5 V and $VREFN_1$ = 1.5 V while $VREFP_2$ = 2.65 V and = VREFN2 = 2.35 V. The integrated signal output from the first stage, represented by the voltages on C3 and C4, is transferred to the second stage during clock phase P2 (SW3, SW4 on), via the intermediate voltage amplifier (Av-Stage). The integrated value of the second stage is compared during P1. The comparator building block has an integrated flip-flop (FF) whose output is updated on the falling edge of P1.

The integration resistors for each stage are split into two equal resistors, one connected to the input switch and the other to the feedback switches, unlike the single resistance used in [6]. This is done to prevent large input voltage swings on the Av-Stage and comparator from occurring during the integration phase. Furthermore, to prevent possible saturation of the Av-Stage during the P1 clock phase, the amplifier has additional TFT switches to disable its gain and reset its output voltage during this clock phase; this speeds up its response during the subsequent P2 phase when it is activated. The integrator time constants (RC products) for this design have been determined in such a way as to achieve the same values of $\alpha_{1,2}$ optimized in [9] by scaling to 2 MHz clock operation (250 ns integration time). It should be noted that in this case, integration

takes place over the corresponding entire clock phase (P1 for the first integrator and P2 for the second integrator). This is different from the approach taken in [9] where a monostable circuit is used to limit the integration time and thus reduce the required value of the RC product. Since the TFT technology employed here permits relatively large values of R and C elements, this monostable circuit is not required, thus reducing the timing complexity as well as noise generated due to the monostable jitter. It should be noted that the capacitor values adopted in this design have been increased by a factor of 4 compared to the values used in [9], with a corresponding reduction in the scaled resistor values. Larger integration capacitors are used in this TFT design to mitigate the loading effect of the relatively high input capacitances of the TFT-based Av-Stage and the comparator stages on the corresponding passive integrators: this large input capacitance is a result of the high aspect ratio of the TFTs used in the corresponding input differential pairs of these building blocks, which are sized in this way, to compensate for the relatively low mobility of the TFTs when compared to silicon-based FETs. A summary of the SD component values is shown in Table 1. A further advantage of using higher capacitance values for the same value of α is a reduction in the integrator input-referred thermal noise $P_{N,}$ which is given by [9]:

$$P_N = \frac{2kT}{\alpha C} \tag{11}$$

Table 1. Selected component values and corresponding system parameter values

System closed loop Gain	A_{SD}	2.437
Integration time	T_i	250 ns
First integrator	R_1, R_2,R_3, R_4	550 kΩ
	C_1	18 pF
	α_1	0.0126
Second integrator	R_5,R_6,R_7, R_8	550 kΩ
	C_2	36 pF
	α_2	0.0063
Intermediate amplifier gain	G_{Av}	6
Feedback to first integrator input	$VREFP_1$	3.5 V
	$VREFN_1$	1.5 V
	G_{fb1}	0.4
Feedback to second integrator input	$VREFP_2$	2.65V
	$VREFN_2$	2.35V
	G_{fb2}	0.06
Mean comparator gain	G_{comp}	5117

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Figure 3 shows the digital building blocks that control the switches and the comparator timing. The clock generator building block generates the required non-overlapping clock phases P1 and P2, together with their corresponding complementary signals, from a single clock source.

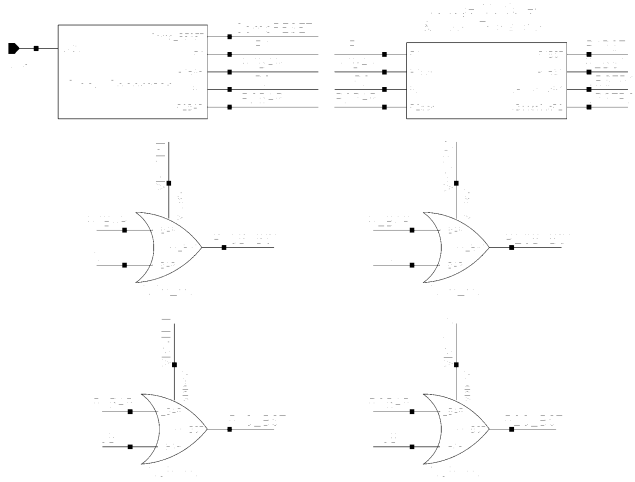

Fig. 3: Digital control section of the SD modulator
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Furthermore, it also generates the comparator reset signal whose falling edge determines the comparison instant. Since the switches, used in this design, require signal voltages exceeding the supply voltage Vdd, a voltage multiplier and level translator building block is also required to generate supply voltages VBoostOutP1/2, which are intended to be connected to the drain of the pull-up TFT in logic gates having a high voltage output swing. This building block also generates high-voltage clock phase signals P1BST and P2BST, coincident with P1 and P2. Feedback switches, which are synchronized with the P1/2 clock phases and are also dependent on the comparator output Q/QB, are generated via NOR logic gates (NOR_HV), exhibiting a high-voltage output swing. NOR logic is exclusively used in this design as it tends to be faster than NAND logic employing series pull-down transistor stacks.

2.3 Boot-Strapped Switch Design

For this design, the gate boot-strapped switch shown in Figure 4 is adopted. This approach ensures reliable switching of the signal without the necessity of a p-channel device. Furthermore, since the gate overdrive is fixed, it also ensures that the switch on-resistance of M3 is kept constant, independent of the signal voltage: this is essential to reduce distortion, which may occur in passive SD topologies as the switch on-resistance is effectively in series with the R1-R4 and R5-R8 and thus affects the integration current. Gate bootstrapping also ensures that charge injection is kept relatively constant, independent of

the signal voltage (Vin, Vo), and is thus canceled using the differential topology.

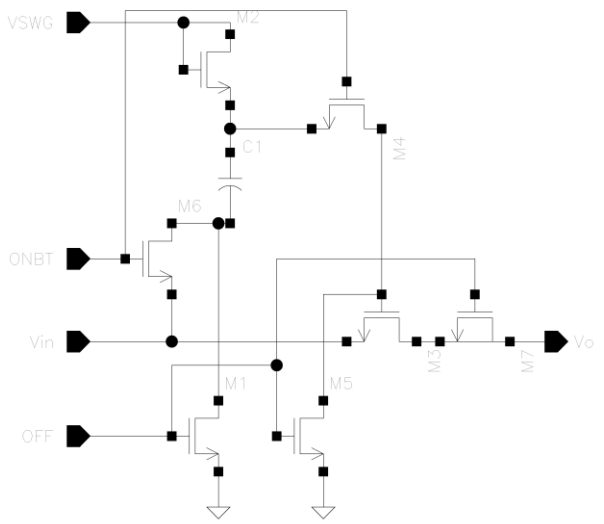

Fig. 4: Schematic diagram of the gate boot-strapped switch
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During the off-state, M1 and M5 are turned on via a voltage applied to the OFF pin. M2 acts as a forward-biased diode, causing the boot-strap capacitor C1 to charge to approximately VSWG, which is set to 3 V. M5 ensures that the switch M3 is kept off. During the on-state, M4 and M6 are turned on via a voltage applied to the ONBT pin, causing the voltage on C1 to be applied to the switch M3. The voltage (7 V) on the pin ONBT must be higher than Vdd for reliable operation, and for this reason, the driving clock signals are designed accordingly. The maximum on-resistance of M3 is below 5 kΩ, which is 0.5% of the integrator resistance value, and thus it presents a negligible effect on the integrator time constant. M7, which is half the size of M3, acts as a dummy switch to partially cancel out the charge injection introduced by M3 during turn-off: this feature reduces the downward drift in the common-mode voltage which would otherwise occur due to charge injection.

2.4 Intermediate Gated Voltage Amplifier (Av-Stage)

The intermediate amplifier, shown in Figure 5 (Appendix), acts as a buffer between the first and second integrator stages and also provides a fixed voltage gain of 6, which is chosen to optimize the signal-to-noise ratio. Furthermore, this amplifier ensures that the second integrator stage operates at the correct common-mode voltage (2.5 V), independent of common-mode drift introduced by the first integrator stage. Voltage amplification is carried out using the source-degenerated differential pair M2, M3, which is cascoded via M6, M7. The voltage gain is fixed to approximately R2/R4, provided that the transconductance of M2 and M3 is sufficiently high. Source degeneration ensures accurate voltage gain control as well as linearity of the amplifier, which is crucial as it is used in an open-loop configuration. A buffer stage consisting of the source follower stage M8, M9, is also used to further lower the output resistance and improve isolation between the two integrator stages. Transistor M21 is used to disable the differential stage gain during the integration phase (P1) of the first stage of the SD modulator. Furthermore, to prevent saturation, during this clock phase, the output of the differential pair is also short-circuited via M22. This results in a rapid response during the clock phase P2, when the amplifier is activated for its output to be subsequently processed by the second integrator stage.

Output common-mode voltage sensing is carried out using R5, R6. This voltage is compared to the common-mode reference voltage (VCM_REF = 2.5 V) via the differential pair M12, M13. Transistors M14 - M19 perform the necessary level shifting and signal subtraction to generate the common-mode correction signal, which is applied to the gates of the current source transistors M4 and M5 of the first stage. This ensures that the output common-mode voltage of the intermediate amplifier is maintained at 2.5 V, which is essential for controlling the common-mode voltage level of the second integrator and thus ensuring correct operation of the comparator stage.

2.5 Comparator – FF Design

The schematic diagram of the clocked comparator and D-FF is shown in Figure 6 (Appendix). The comparator section consists of a high-speed, low-gain pre-amplifier with a source follower and a clocked latch. The pre-amplifier is designed around the differential pair M1, M2, with M4-M7 acting as loads. This load structure has been chosen as it provides the required DC voltage level for the subsequent source follower stage M11-M14. Furthermore, this load structure presents a relatively high load resistance for small signals and a lower resistance for larger signals, resulting in signal compression: for the comparator stage, signal linearity is not important, while compression of large signals limits the large signal voltage swing and thus improves comparator recovery response after it has been subjected to a relatively high input signal.

Comparison is activated during clock phase P1, while during the previous clock phase P2, the comparator is subjected to a high input voltage, which essentially occurs during the integration phase of the second stage. For this reason, switch M8, which is activated during clock phase P2, is introduced to effectively short-circuit the pre-amp stage output nodes and thus further enhance recovery and comparison speed during the P1 clock phase. This switch is activated by the P2BST signal, which is a high-swing signal (0, 7 V) coincident with P2.

The subsequent buffer M11-M14 further reduces the output resistance and drives the latch driver stage consisting of the differential pair M16, M17. Kick-back noise, generated by the latch, is significantly reduced by this buffer stage as well as by the M8 switch. This is an important aspect in passive SD modulator design, where the input voltage levels presented to the comparator stage can be significantly smaller than in standard switch-capacitor SD modulators employing active OTA-based integrators.

Comparison takes place during clock phase P1 and coincides with the falling edge of the Reset signal controlling the comparator latch stage. When Reset is active, M24 keeps the latch outputs QR, QRBAR at equal voltage levels, with all the transistors M18-M23 operating in the active region. R1 and R2 act as the load resistors for the latch driver differential pair M16, M17. On the falling edge of the Reset signal, M24 turns off, causing QR and QRBAR to flip to the required logic levels via the positive feedback introduced by M20 – M23. It should be noted that none of the transistors in the latch are turned off during the reset phase, thus optimizing comparison speed as soon as the falling edge of the Reset signal occurs.

The latched comparator outputs are stored and kept constant during the P2 phase via the subsequent D-FF stage. Loading of the comparator latched outputs QR, QRBAR onto the FF occurs when the load signal is activated and the hold signal deactivated. During this instance, the current through M29 and M30 is switched off via M34, thus reducing the positive feedback in the FF. Simultaneously, with the LOAD signal applied, M31 and M32 are activated, causing the FF outputs Q and QB to follow the latched comparator outputs QR and QRBAR. The transistors are sized such that the comparator-driven signal path consisting of M31, M32, M25, M26 over-rides the residual latching (positive feedback) effect of M27, M28, thus ensuring that the FF outputs latch in the required direction. This is important as, for speed optimization, M27 and M28 are not switched off in this FF design. When the HOLD signal is activated, the FF is effectively isolated from the comparator as the current through M31 and M32 is switched off and control is transferred to the positive feedback transistors M29, M30, thus keeping the required output logic levels at Q, QB constant during clock phase P2.

2.6 Clock Generator Design

The clock generation circuitry, shown in Figure 7 (Appendix), generates the two non-overlapping clock phases P1 and P2, their complements, as well as the reset signal (Comp_RESET) for the comparator timing. Clock phases P1 and P2 are generated using a standard NOR-based flip-flop built around NOR1 and NOR2, with inverters IN4-IN11 in the feedback path, which set the deadband between the two clock phases. It should be noted that inverters denoted by INH have a slightly higher drive capability than those denoted by IN.

The comparator reset is controlled via the monostable designed around M1, R1, and C1. On the rising edge of P2, C1 is quickly discharged by M1, causing Comp_RESET to go high, thus keeping the comparator latch in a reset phase during P2. Since R1 is connected to P1, no current passes through R1 during this time. When P1 goes high, C1 starts charging through R1 as M1 is switched off. When the voltage on C1 reaches the input-high threshold for IN12, Comp_Reset quickly flips to zero, thus initiating the comparison. At this instant, M2 is also turned off, causing M5 to turn on and quickly charge C1, thus resulting in a very sharp falling edge of the Comp_Reset signal, which is important as this defines the comparison instance. Thus, the comparison instance is defined by the time constant set by R1, C1, and the input high threshold of IN12. This delay is adjusted to allow enough setup time for the comparator pre-amp stage to settle to the input voltage before comparison is triggered. Comp_RESET again goes low on the subsequent P2 phase with M4 being turned on to quickly switch off M5, thus ensuring abrupt discharge of C1. Transistor M3 and capacitor C2 are used for gate-bootstrapping of M5, which ensures that the voltage on C1 can quickly reach Vdd at the comparison instance, thus ensuring reliable operation on IN12 and the subsequent cascaded gates.

2.7 Voltage Multiplier and Level Translation Signal Generation

The boot-strapping circuitry employed in the switches controlling the integration function requires high voltages of around 7 V, exceeding

Vdd for their correct operation. For this reason, a voltage multiplier and voltage level translators have been designed as shown in Figure 8 (Appendix). High voltage generation is carried out via the voltage multiplier, consisting of M1, M2, C1 and C2, which generates boosted voltages VBoostOutP1 and VBoostOutP2. These two high-voltage signals, coincident with P1 and P2, are used as the supply voltage for the level translators generating P1BST and P2BST, as well as some of the high-voltage output NOR gates, which control the feedback switches in the SD integrators. The level translators consist of inverters driven by P1bar and P2bar with a gate-bootstrapped transistor (M4, M8), in the output stage, whose drain is connected to the boosted voltages generated by the voltage multiplier. It should be noted that these high-voltage clock signals drive only capacitive loads and thus do not sustain any quiescent current dissipation. For this reason, the values of C1 and C2 can be kept relatively low and do not impose high driving capability requirements on P1 and P2.

2.8 Logic Gate Design

Logic implementation has been carried out solely using NOR gates (rather than NAND gates).

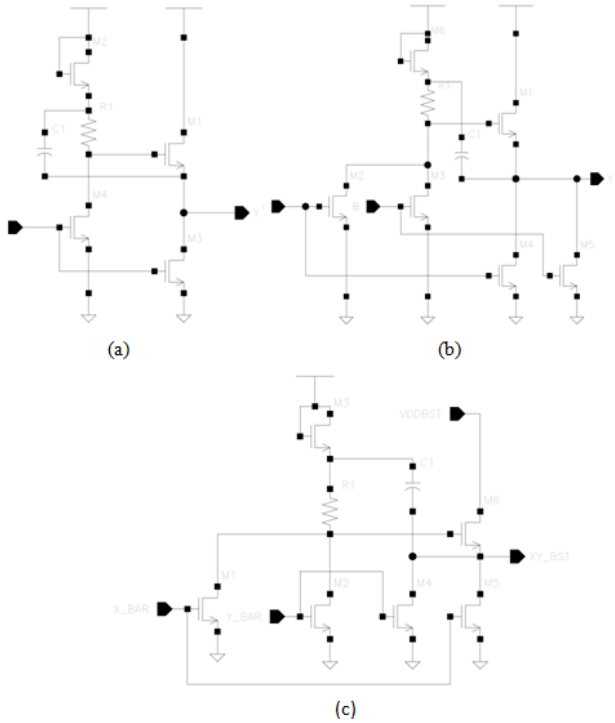

Fig. 9: Logic gates used in this design: (a) inverter, (b) NOR gate, (c) NOR gate with high voltage output
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This feature avoids the use of series pull-down transistor stacks, which are prone to increased resistance and capacitance, thus exhibiting lower speed performance. In addition, some of the NOR gates must generate high-voltage outputs for the correct functionality of the switches connected to the reference voltages, which are controlled by the comparator feedback signals Q and QB. The implementation of the logic gates used in this design is shown in Figure 9. Gates intended for voltage levels within Vdd are implemented using a gate-bootstrapped transistor at the output stage with its drain connected to Vdd. For the high output voltage version of the gates, the output transistor drain (VDDBST) is connected to the respective VBoostOutP1/2 voltage corresponding to the coincident phase on which that output may be activated.

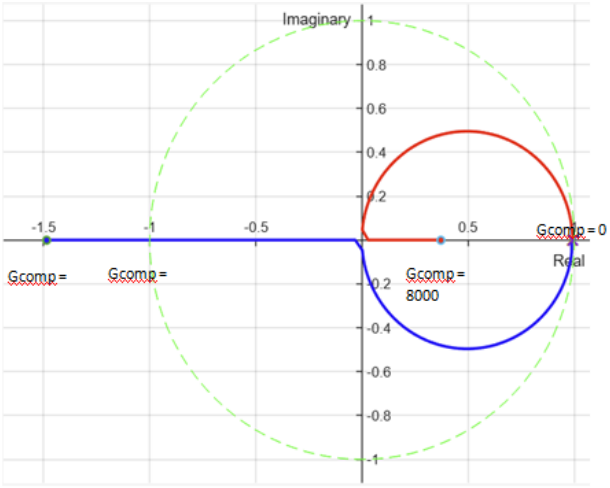

Fig. 10: Root locus of the passive SD modulator plotted for comparator gain values 0 to 8000
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3 Simulation Results

3.1 System Level Stability Analysis

The system parameters were chosen such that the passive SD architecture approximates a standard second-order system, having a gain (A_{SD}) = 2.437. Stability was verified using the root locus technique, where the comparator gain was varied between 0 to 8000 and the corresponding plot is shown in Figure 10 (Appendix). The system is stable for comparator gain values less than 6852, at which point the root locus crosses the unity circle at z = -1, indicating that the system is effectively stable as the comparator gain will dynamically reduce if the system approaches instability.

Furthermore, sensitivity analysis of the stability to system parameter variation shows that the system will become unstable if the values of α_1 and α_2 are

both doubled, with no adjustment of the feedback ratios gf_1, gf_2, in which case the root locus will coincide with the unity circle. This means the system is stable even with extreme process variations as these would not be sufficient to cause the integrator time constants to decrease by up to 50%.

3.2 Timing Generation

Figure 11 shows the transient simulation for the main clock phases P1 and P2, with their corresponding high-voltage phases P1BST and P2BST. The diagram also shows the comparator and FF load, hold, and reset control signals.

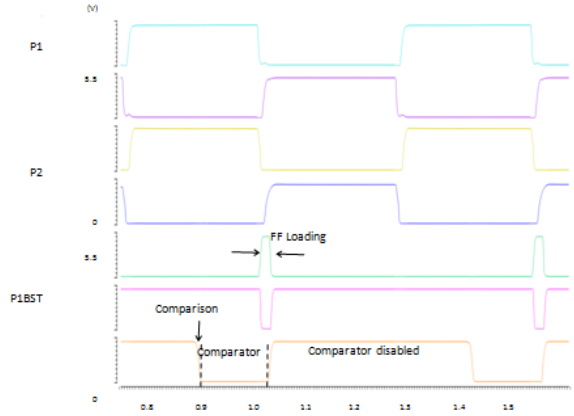

Fig. 11: Timing signals for the main clock phases (P1, P2 and their high voltage coincident signals P1BST, P2BST) and comparator load, hold and reset

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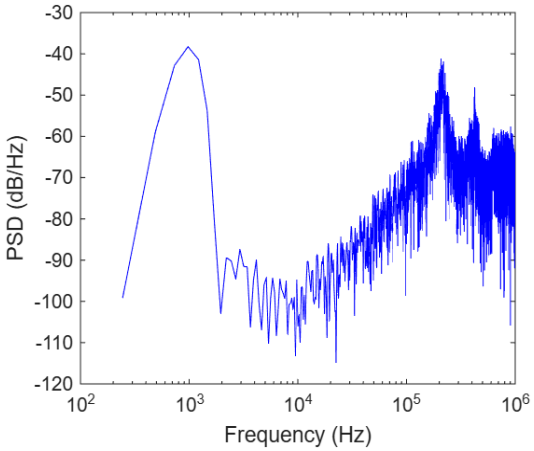

Fig. 12: Power spectral density of the sigma-delta output stream for a 1 kHz, 100 mV amplitude sinusoidal input signal

Source: created by the authors

Comparison takes place during the P1 phase on the falling edge of the reset signal. Between the falling edge of the P1 signal and the rising edge of the reset signal, a load signal is generated to transfer the comparison result onto the FF: during this period, the FF hold signal is deactivated to reduce positive feedback and enable loading to occur.

3.3 Power Spectral Density

The 12000-point simulated power spectral density, excluding device noise and process-induced mismatch, for the SD modulator operating at a clock frequency of 2 MHz with a 100 mVpk 1 kHz sinusoidal input signal is shown in Figure 12. This plot was obtained from a 10 ms transient device-level circuit simulation of the SD modulator, after truncating the first 4 ms, thus resulting in a 6 ms window. For a bandwidth of 1.953 kHz, corresponding to an oversampling ratio of 512, the simulated SNDR is 87 dB, resulting in an ENOB of 14. Since the SNDR reported here corresponds to noise- and mismatch-free device-level simulation, it represents an upper bound on achievable performance.

4 Conclusion

This paper presented the key TFT-based building blocks for passive SD converter design optimized for high-speed operation. At the system level, since the Pragmatic technology allows the implementation of high capacitor values, these have been utilized to mitigate the effect of the amplifier and comparator input capacitance, while also reducing timing complexity and noise. Split integration resistor elements have been implemented to prevent saturation of these building blocks during the integration phase, thus resulting in further speed optimization. Further speed optimization has been achieved via the use of NOR-based logic and by employing gain reduction and reset circuitry in the amplifier during the inactive phase, as well as optimized comparator-FF circuitry, which avoids complete turn-off of the TFT devices during the reset phase. Since these circuit building blocks are largely topology-independent, the proposed design techniques may be extended to other TFT-based sigma-delta architectures, including higher-order and MASH-based implementations.

Future work will investigate the impact of TFT device noise, mismatch, and process variation on the achievable SNDR.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- Ivan Grech was responsible for conceptualisation, circuit optimisation, simulation and compilation of results and writing this paper.
- Joseph Micallef was responsible for technical checking of this paper.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.

APPENDIX

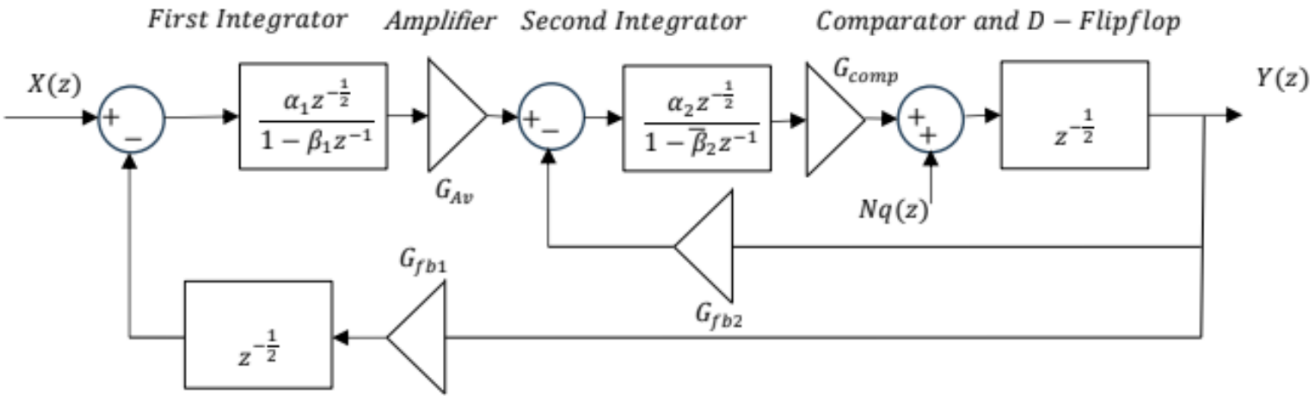

Fig. 1: Block diagram of the second order passive sigma-delta Modulator
Source: adapted from [10]

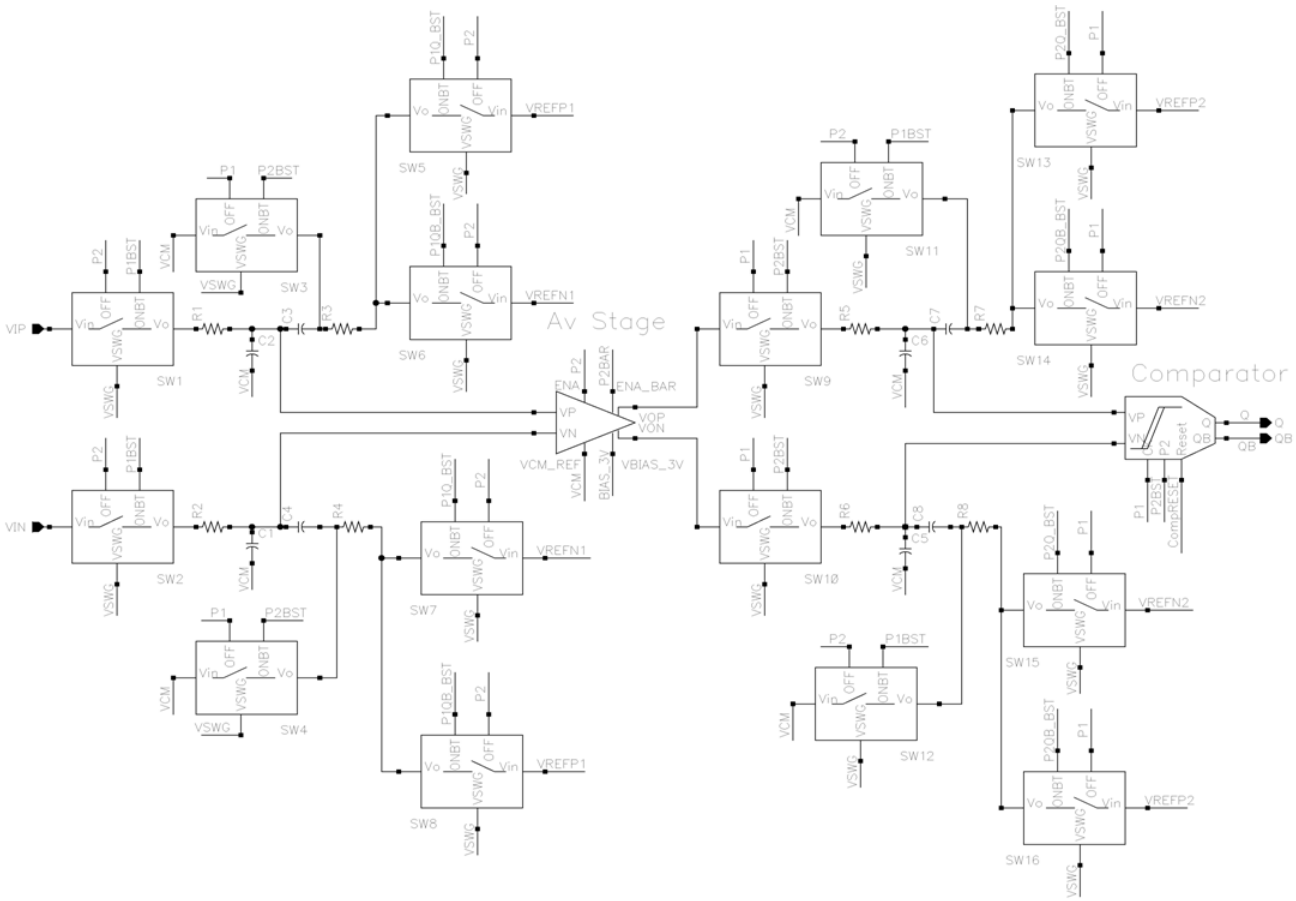

Fig. 2: Top-level view of the analog section of second-order passive sigma-delta modulator
Source: created by the authors

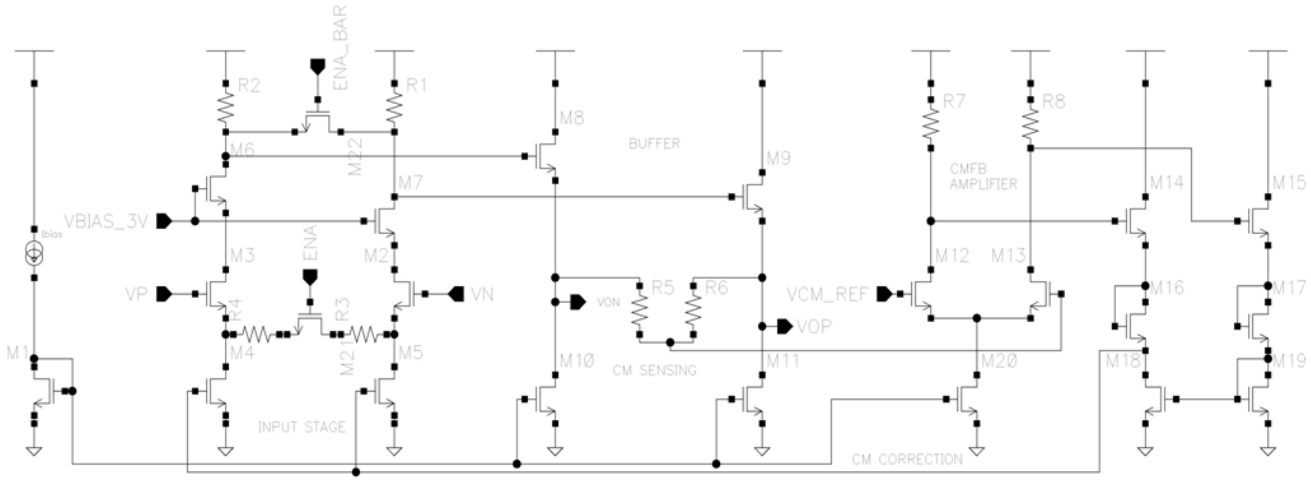

Fig. 5: Schematic diagram of the intermediate voltage amplifier (Av-Stage)
Source: created by the authors

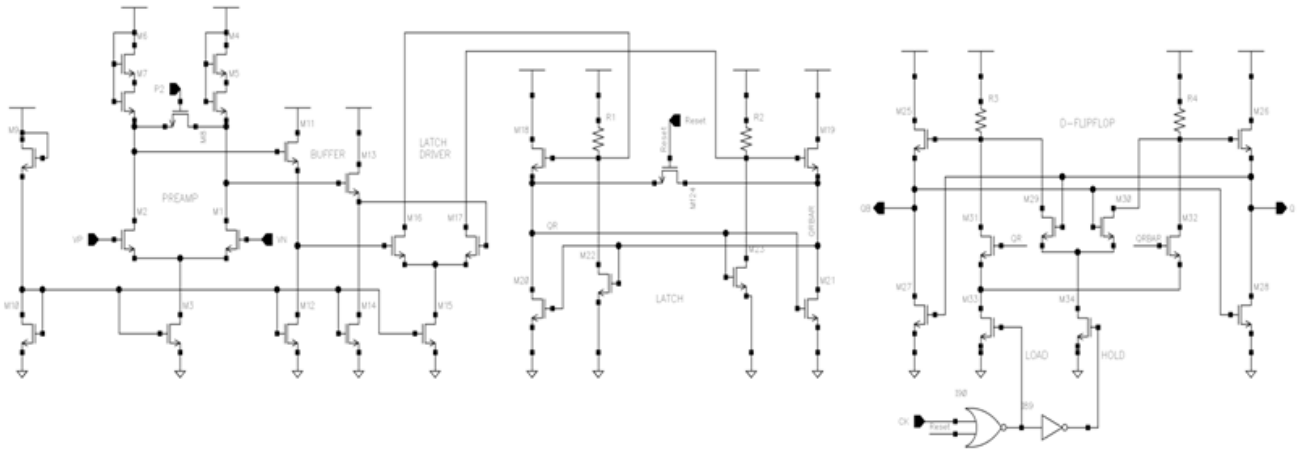

Fig. 6: Schematic diagram of the clocked comparator and D-FF
Source: created by the authors

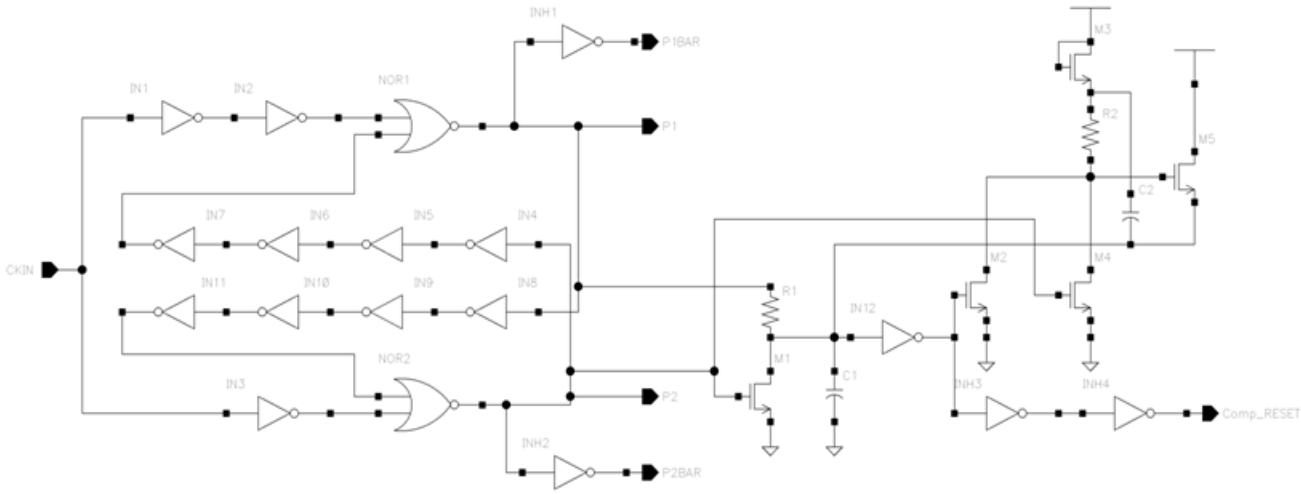

Fig. 7: Schematic diagram of the clock generation circuitry
Source: created by the authors

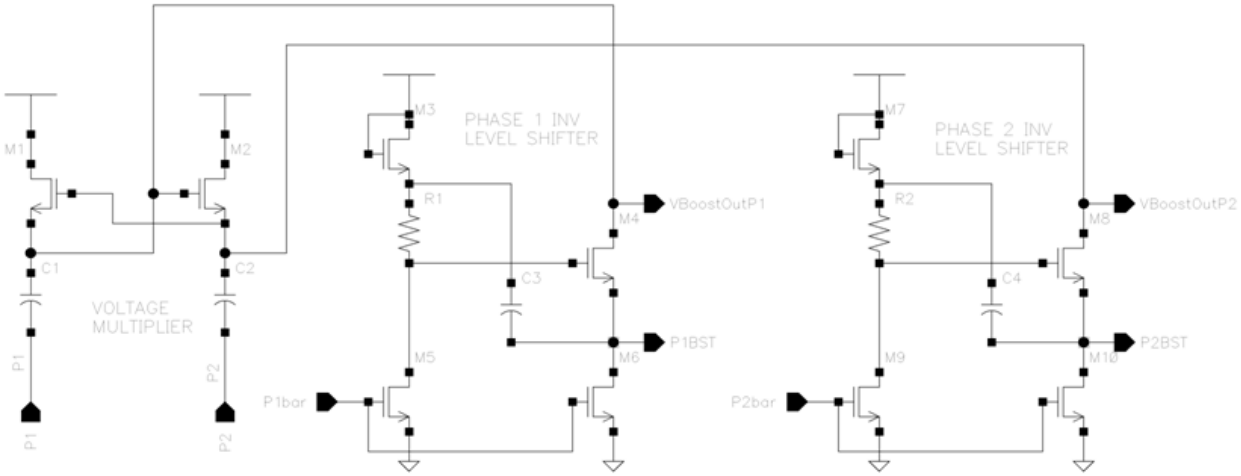

Fig. 8: Schematic diagram of the voltage multiplier and the level translators
Source: created by the authors