Implementation of a Digitally Controlled MOS based Tuned Reconfigurable Filter for High Frequency Applications

MD TANZIM AHMED[1], MANASH PRATIM SARMA[1], NIKOS E MASTORAKIS[2],
[1]Dept of ECE, Gauhati University,Guwahati, INDIA
[2]Faculty of Engineering, Technical University of Sofia, BULGARIA

Abstract- With the advent of recent standard of high data rate communication standards, the systems need to meet the requirement of multi-frequency processing. Moreover to achieve backward and forward compatibility across communication standards, reconfigurable and tunable designs are preferred. This paper proposes a fully digital reconfigurable all pass filter (APF) with a tunable passband to meet such requirements. The reconfigurable APF is capable of band tuning using a digital current control source (DCCS) which uses a digital word count making it most effective and simple reconfigurable design than the already reported designs. This can be widely used in different systems, e.g., 5G receivers, radar communication, cyber security, sensor interfaces, etc. This APF is also connected to Schmitt trigger inverter for smooth communication. Moreover, the circuit is designed to be inductor less thus making the design area efficient and suitable for wide range of applications and systems. The proposed design is simulated using 65 nm GPDK CMOS technology that achieves a wideband range of 0.1-15 GHz and achieves a bandwidth of 12.6 GHz with a gain of 15.5dB with a time delay of 1.62ps. The static power consumption of the circuit is only 2.52mW.

Keywords: DCCS, CMOS, 65-nm technology, flip flop.
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1. Introduction

In today's world, technology plays a very important role, especially in communication sector. Filters using CMOS technologies are the most preferred filter circuits in today's advance world as the variability and reconfigurability can be easily adjusted in a CMOS filter which is most preferable aspect in any filter circuit and more importantly they can be further modified in terms of noise reduction, bandwidth increment, etc.

Filters with reconfigurable nature and true time delay cells are being widely used and implemented. This filters have achieved high capability of tuning with true delay cells[1-3]. Nowadays filters are also available with intrinsic switching that exhibits a quasi-elliptic-type transfer function which can be tuned in for both frequency and bandwidth (BW) and can be intrinsically switched-off and on and thus achieving the reconfigurability of the filter circuit [4]. Active RC filters have also emerged as a growing field in filter circuits which filters out the most unwanted signals, as they separate and allow to pass only those sinusoidal input signals based upon their frequency and required bandwidth [5]. Recent studies shows adaptive bandpass filters are used in grid synchronization widely as it provides a means to adjust the various parameters attached to it according to an optimization algorithm, which is very effective and fruitful [6].Defected ground structures are also recently used in order to design filter circuits as they help in enhancing the bandwidth and gain of microstrip antenna and also helps in suppressing mutual coupling between elements [8] and also various applications are being proposed of filters using lumped components as it maintains a minimal change in phase of a waveform between the input and output connections whenever it is in operating mode. [9].

The digital current control source (DCCS) is an integral part of digital control oscillators which forms the basic reconfigurable part of any filter circuit. It helps in tuning of the circuit in wide range along with required reconfiguration and efficiency [20, 21].

In this paper, a first order voltage mode inductor less all pass filter is being proposed. The proposed filter circuit consists of 3 parts, firstly an inductor less all pass filter circuit is designed then the proposed filter circuit is reconfigured using a digital current control source (DCCS) which is then connected to a parallel source of Schmitt trigger inverter. The proposed filter circuit achieves a wideband range of 0.1-15 GHz and achieves a bandwidth of 12.6 GHz with a gain of 15.5dB having a time delay of 1.62ps. The circuit consumes only 2.52mW from 2-V supply. This paper is

organized as follows: Section II describes the design of the reconfigurable filter. Section III consists of simulation and results. Conclusion is drawn in Section IV.

2. The Design of the Reconfigurable Filter

The design of the entire system starts with the system block diagram as shown in figure 1. Here the block diagram is basically divided into 3 parts: digitally controlled current source (DCCS), Schmitt trigger inverter and all pass filter.

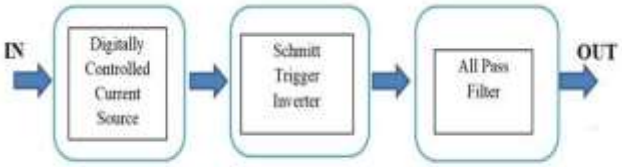


Fig.1. Block diagram of the system

The input signal is taken into the DCCS which does the main work of reconfiguring the filter by taking input from various word counts after which the output is sent to Schmitt trigger inverter for reducing the noise in the circuit before passing it to the all pass filter. The signal after passing through the all pass filter gives an output of high bandwidth and free from noise. We get a desirable range of frequency from the stated all pass filter.

2.1 Inductor less design of the All Pass Filter

The first stage of the design is the block diagram of inductor less all pass filter as shown in figure 2.

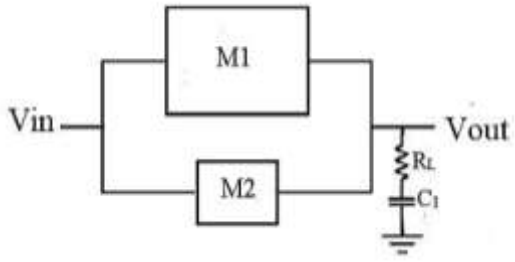


Fig.2. Block diagram of inductor less all pass filter

Here the block diagram consists of two transistors M1 and M2, resistor R_L and capacitor C_1.Here, 2 parts are formed, the low pass part and unity gain part. The low pass part is the combination of resistor R_L, transistor M1 and capacitor C_1 while resistor R_L, capacitor C_1 and transistor M2 together forms the unity gain part. The schematic inductor less all pass filter circuit is shown in figure 3.

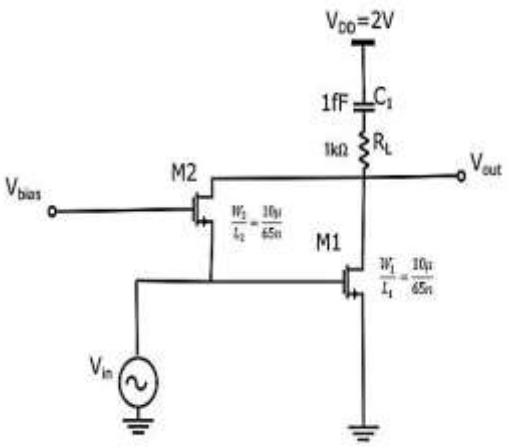


Fig.3. Inductor less first order voltage mode all pass filter.

If transistor parasitics is ignored, the transfer function of the all pass filter circuit is given by:

$$\frac{V_{out}}{V_{in}}(s) = -\frac{g_{m1}R_LC_1}{1+g_{m1}} + g_{m2}R_LC_1$$

$$= \frac{\{-g_{m1}R_LC_1 + g_{m2}R_LC_1(1+g_{m1})\}}{1+g_{m1}}$$

$$= \frac{-g_{m1}R_LC_1 + g_{m2}R_LC_1 + g_{m1}g_{m2}R_LC_1}{1+g_{m1}}$$

$$= \frac{-R_LC_1(g_{m1}-g_{m2})+g_{m1}g_{m2}R_LC_1}{1+g_{m1}} \quad (1)$$

The transconductances of M1 and M2 are given as g_{m1} and g_{m2} respectively. Taking, $g_{m1} = 2g_{m2}$ and$g_{m2}R_LC_1 = 1$.

Pole/zero frequency of the first order all pass filter is given by:

$$\left|\omega_{p,z}\right| = \frac{1}{g_{m1}} \quad (2)$$

Phase response of the first order all pass filter is given by:

$$\emptyset(\omega) = -2tan^{-1}\frac{\omega}{|\omega_{p,z}|} \quad (3)$$

$$= -2tan^{-1}\omega g_{m1} \quad (4)$$

Group delay response is given by:

$$D(\omega) = 2g_{m1}\frac{1}{1+(\omega g_{m1})^2} \quad (5)$$

Here, ω is the angular frequency given by frequency f, where ω = 2π f.

Here, after designing the required inductor less all pass filter, there is a need to make the circuit digitally reconfigurable in nature. So that it can adjust to variable frequency ranges and attains the required bandwidth automatically.

2.2 Reconfigurable & Tunable design of Digital APF

To make the APF digitally reconfigurable in nature, the APF is connected to a Digitally Controlled Current Source (DCCS) which enables the APF to adjust its frequency range automatically. Figure 4 represents the block diagram of the APF connected to a DCCS.

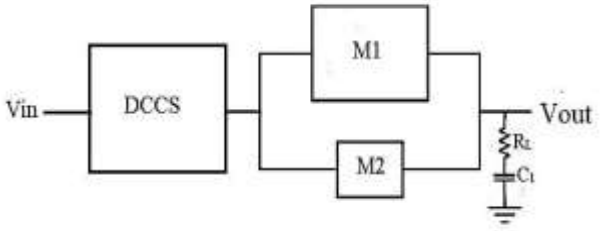


Fig.4. Block diagram of digitally reconfigurable inductor less all pass filter

The transfer function of the digitally reconfigured inductor less all pass filter is given by:

$$\frac{V_{out}}{V_{in}}(s) = -\frac{g_{m1}R_LC_1}{1+g_{m1}} + g_{m2}R_LC_1 + I_{ctrl}$$

$$= \frac{\{-g_{m1}R_LC_1 + g_{m2}R_LC_1(1+g_{m1}) + I_{ctrl}(1+g_{m1})\}}{1+g_{m1}} \quad (6)$$

The used digitally controlled current source is depicted in figure 5. In order to illustrate reconfigurability and tuning process, 4 current branches are selected. Transistors M_{00}, M_{01}, M_{02} and M_{03} are connected in parallel and controlled by switch transistors SW_0, SW_1, SW_2 and SW_3. The switches are controlled by digital control word (D_3, D_2, D_1, D_0) which is generated with the help of a 4 bit D flip flop counter.

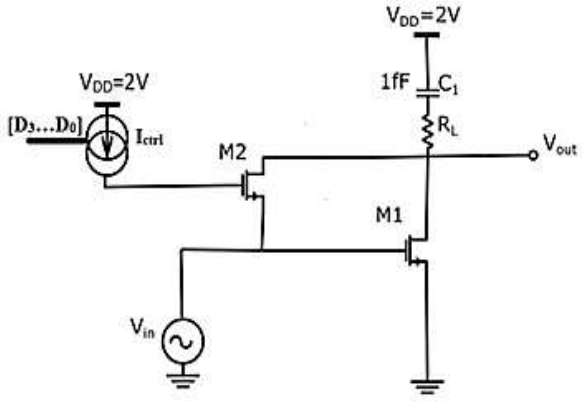


Fig.5. Digital current control source tunable all pass filter

If the value is 1, the switch is turn on and when the value is 0 the switch is turned off and current cannot reach the output terminal. The equivalent current source has high linearity and precision. I_{ctrl} is the sum of current accounted by each branch I_0, I_1, I_2 and I_3 as shown in figure 6.

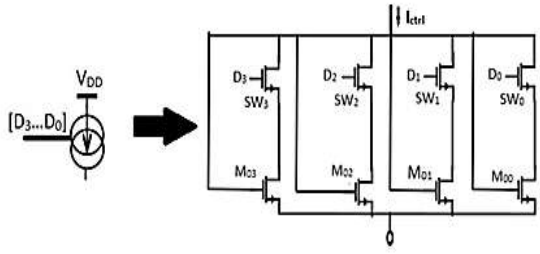


Fig 6. I_{ctrl} descriptive diagram

$$I_{ctrl=}\, I_0 + I_1 + I_2 + I_3 \quad (7)$$

$$I_{ctrl} = V_{out}\left(\frac{D_0}{M_0}+\frac{D_1}{M_1}+\frac{D_2}{D_3}+\frac{D_3}{M_4}\right) \quad (8)$$

After attaching the DCCS to the APF circuit the digital control mechanism is guided by a 4 bit word count which gives various input bits in order to provide the range of frequency needed to reconfigure the filter.

2.3 Digital Control Mechanism

The 4 bit digital word count is achieved by using a D Flip Flop counter. Each input of the counter acts as the input of each switch as D_0, D_1, D_2 and D_3. The count generates 1 or 0 every time to make the current flow and stop through each switches coming from the branches of I_0, I_1, I_2 and I_3.The D Flip Flop counter is shown in figure 7.

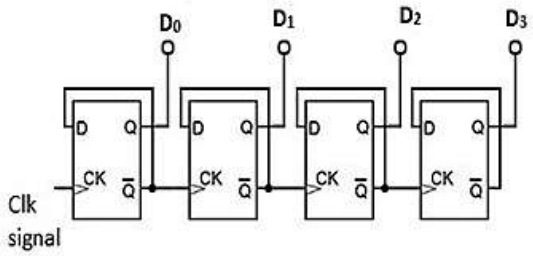


Fig. 7. 4 bit D Flip Flop Counter

The Truth table of the counter generating the reconfiguration of the filter is shown in Table 1.

Table 1. Truth table

Word Count	D_0	D_1	D_2	D_3
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Here, after making the APF reconfigurable in nature, the circuit is vulnerable to high noise as the DCCS contributes to increase in noise level in the circuit and disrupts the signal, leading to poor signal. Hence, there is a need to reduce the noise in the circuit to make the signal noise less.

2.4 Modified Design of Digital APF

In order to reduce the noise in the circuit, the proposed reconfigurable APF filter circuit is connected to Schmitt trigger inverter. Figure 8 represents the block diagram of the reconfigurable APF filter connected to Schmitt inverter. The block diagram represents 3 parts, 1stly the signal passes through DCCS which is digitally reconfigured and passed onto Schmitt trigger inverter for smoothening and noise removal, after which the final signal passes to APF circuit and the final output is obtained.

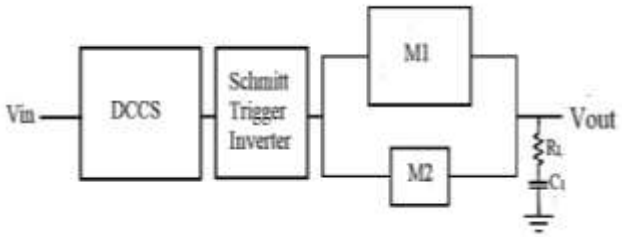


Fig.8. Block diagram of digitally reconfigurable inductor less all pass filter connected to Schmitt trigger inverter

Two Schmitt trigger inverters connected in parallel are attached to the circuit to make the signal smooth and reduce noise for transmission and communication purpose as shown in figure 9.The Schmitt trigger doesn't alter any output only enhances the output signal and reduce noise. The used Schmitt Trigger Inverter is depicted in Fig 10.

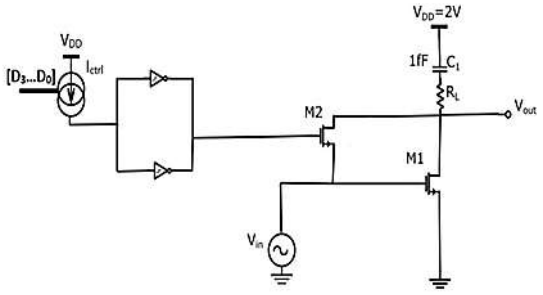


Fig.9. Reconfigurable APF circuit with Schmitt trigger inverter

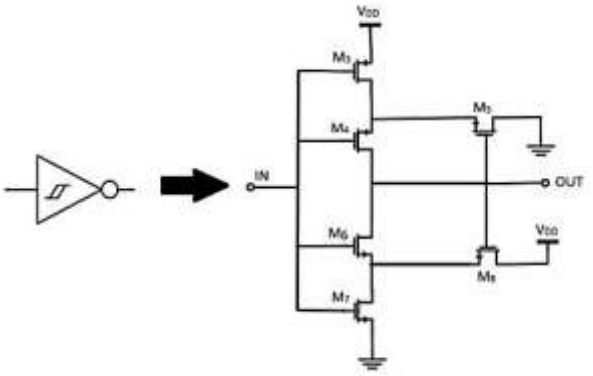


Fig.10.Schmitt trigger inverter

2.5 Complete Reconfigurable APF circuit

Finally all the circuits combined forms the reconfigurable filter circuit as shown in figure 11. Here the circuit starts by getting input signal through the digital current control source which acts as the word count facilitator using the help of D flip flop sending 0's and 1's. The word reconfigures the range of frequency to be passed with every signal passing. Once the required signal is generated it is passed through a Schmitt trigger inverter to reduce the noise, in order to get a hassle free signal. Once it is achieved, the final signal is passed through the all pass filter circuit in order to get the desired bandwidth and frequency output as well various other parameters.

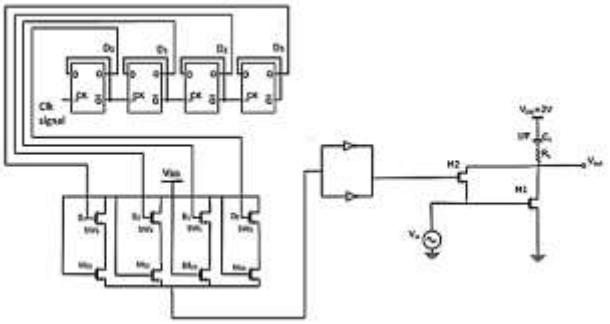
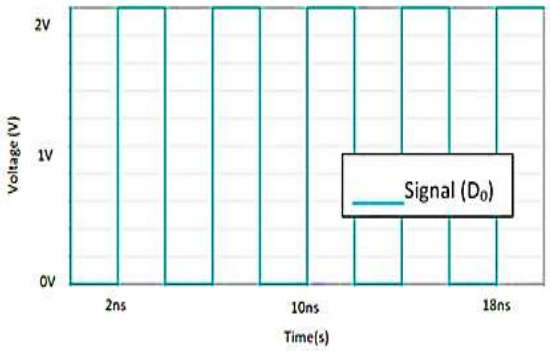


Fig 11. Complete Reconfigurable APF circuit

3. Simulation and Results

The reconfigurable inductor less all pass filter is simulated in LtSpice using a 65nm CMOS process. The reconfiguration is achieved using a D Flip Flop counter to generate 4 bit word count in DCCS. As a result using delay in every counter, 4 bits are generated as shown in figure 12, 13, 14 and 15. D_0 has no delay, D_1 has a delay of 2s, D_2 has a delay of 6s and D_3 has a delay of 10s to generate binary outputs of 0's and 1's. These outputs together contribute to a total of 16 bit and as a result frequency and other parameters are plotted with it.



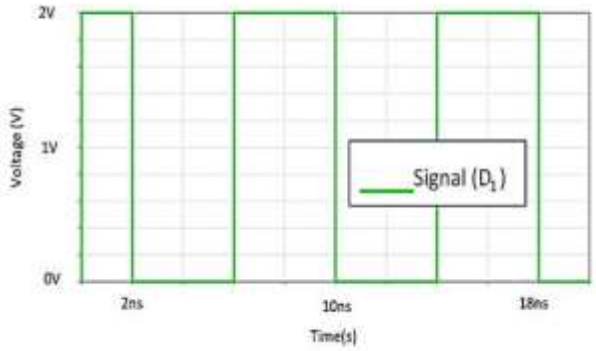


Fig. 12. D_0 word count

Fig. 13. D1 word count

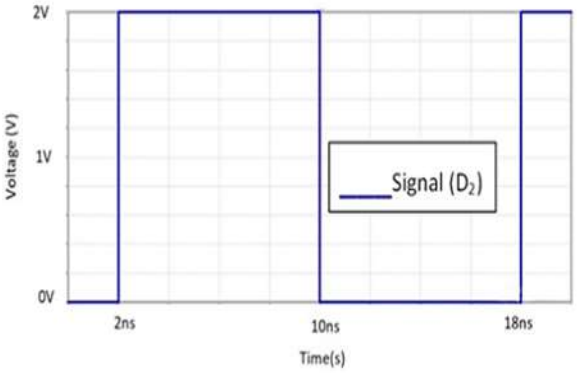


Fig 14. D_2 word count

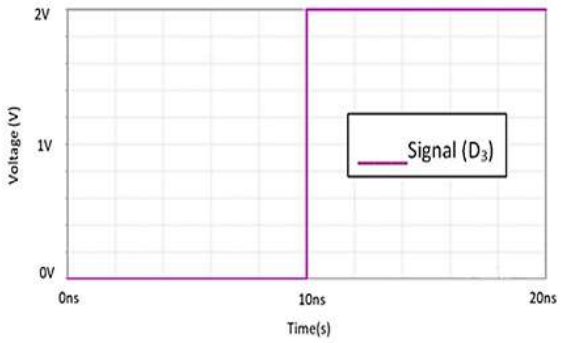


Fig 15. D_3 word count

The circuit is operated at 2V which consumes a total power of 2.52mW which is shown in figure 16.The total power consumption of all the individual components is shown in figure 8.The sharp rise in the plot is due to the sudden switching on and off the switches in DCCS accounting 0 and 1. As, the power consumption is pretty less for rest of the circuit thus easily compensating the sudden rise of power. Thus, the entire circuit consumes very less amount of power to operate smoothly.

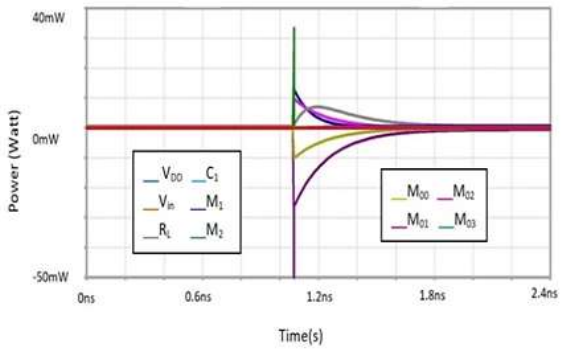


Fig16. Simulated power consumption response of the reconfigurable voltage mode all pass filter.

2 different frequency range output has been plotted, corresponding to Inductor less APF and reconfigurable Inductor less APF.

Figure 17, represents output plot corresponding to simple Inductor less APF ranging from 0.1GHz to 15GHz. The Bandwidth of the circuit is 13.1 GHz with a gain of 15.42dB. The group delay is equal to approximately 1.2ps, having a range of 1.20ps to 1.08ps

Figure 18, displays frequency range of the reconfigured inductor less all pass filter ranging from 0.1GHz to 15GHz. The Bandwidth of the circuit is 12.6 GHz with a gain of 15.5dB. The group delay is equal to approximately 1.62ps, having a range of 1.51ps to 1.77ps.

As visible, output of both simple APF and reconfigurable APF is identical which indicates that the digital reconfiguration is achieved without altering the output and performance of the filter.

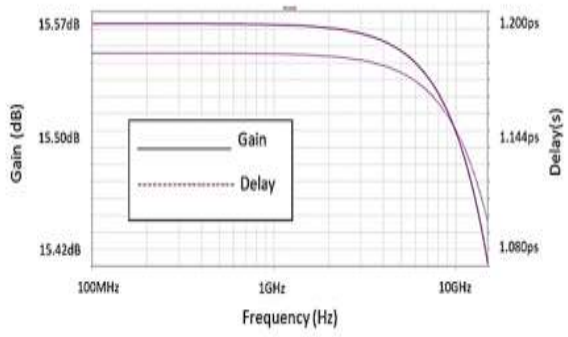


Fig.17. Simulated group delay and gain response of the reconfigurable inductor less all pass filter.

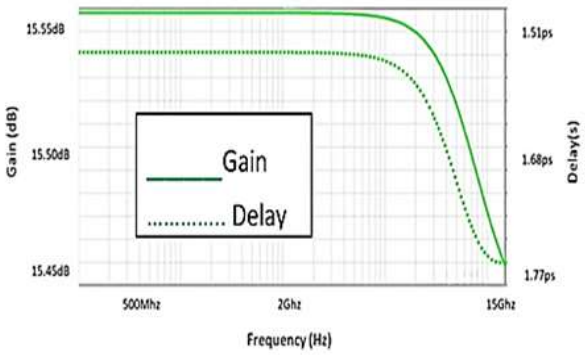


Fig. 18. Simulated group delay and gain response of the simple inductor less all pass filter.

Moreover, the circuit shows a smooth gain attainment achieved due to linearity of the circuit and also delay is very less which indicates no loss of information while transmitting signal. Thus, the circuit operates at a very low group delay, indicating the high efficiency of the

circuit and also the circuit works at a varying range of frequency and giving output of high gain and bandwidth.

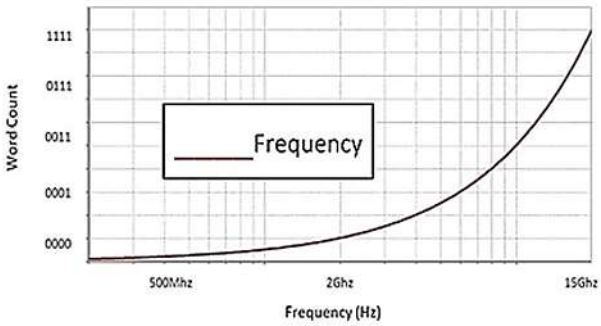


Fig. 19. Simulated frequency response of the reconfigurable voltage mode all pass filter on account of 4 bit word count

Figure 19, displays the frequency response of the reconfigurable voltage mode all pass filter at a frequency ranging from 0.1GHz to 15GHz with the input of word count as shown in table 1. Word count of 4 bit generates a total combination of 16 bit and hence the output. The graph clearly displays slow rise of frequency range from 0.1Ghz to 15Ghz as per word count, this accounts to the stability of the circuit and also the fast rise from 10Ghz to 15Ghz is due to word count 1111 which accounts to switching on all the switches together in the circuit.

Since some bit generates the same value and range. Table 2 and 3, shows the values along with the frequency range they are depicting.

Table 2. Word count representing same values

Sl no.	word count representing same values					
1	0001	1000	0100	0010		
2	0011	0101	0110	1010	1100	1001
3	0111	1011	1110	1101		

Table 3. Frequency range corresponding each word count

Word Count	Frequency Range(approx.) Experimental values (in Ghz)
0000	0.1-2
0001	2.1-6
0011	6.1-9
0111	9.1-12
1111	12.1-15

Figure 20, displays leakage current flowing through the circuit due to the two CMOS transistors. Operating at 2V, M1 transistor has a leakage current of -614.57nA and M2 transistor has a leakage current of 614.57nA, operating within a voltage range of 20mV to 2V. The leakage current also flows at a steady rate with little inclination when the voltage increases. Thus, the low amount of leakage current indicates that the circuit operates smoothly at normal condition without any disturbances or tripping.

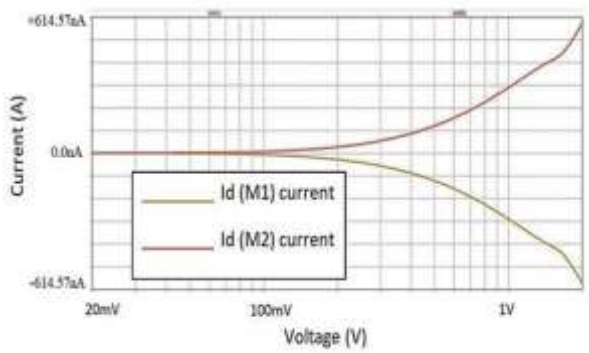


Fig.20. Simulated leakage current response of the reconfigurable voltage mode all pass filter.

2 different Noise plots are plotted where, in one case Schmitt trigger inverter is used in the circuit and in other case Schmitt trigger is not used.

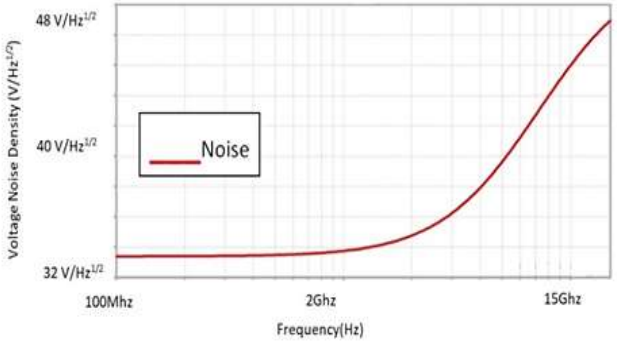


Fig.21. Simulated circuit noise response of the reconfigurable voltage mode all pass filter connected to Schmitt trigger inverter.

Figure 21, displays total noise in the circuit when the circuit is connected with Schmitt trigger inverter. The voltage noise density ranges from $32pV/Hz^{1/2}$ to $48pV/Hz^{1/2}$ and total circuit RMS noise is 6.65µV.

Similarly, Figure 22 displays total noise in the circuit when the circuit is not connected with Schmitt trigger inverter. The voltage noise density ranges from from 44pV/Hz$^{1/2}$ to 64pV/Hz$^{1/2}$ and total circuit RMS noise is 21.77μV.Clearly, noise is more when not connected to Schmitt trigger inverter and hence use of Schmitt trigger inverter is useful to reduce noise and commence a smooth communication. The abrupt inclination of the noise occurs due to the capacitor present in the all pass filter. However, noise in the circuit is found to very low, i.e. 6.65μV which indicates the filter circuit will have very less error and at the same time free from malfunctions.

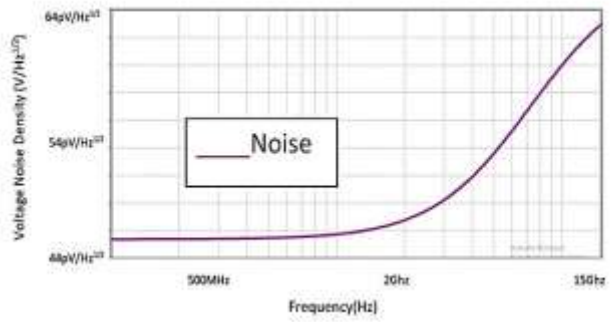


Fig 22. Simulated circuit noise response of the reconfigurable voltage mode all pass filter without Schmitt trigger inverter.

The performance summary and comparison with other active filter circuits are presented in Table 4.Comparing all the results the proposed reconfigured voltage mode all pass filter has made significant improvement in frequency range, low maximum delay value, high bandwidth, lower power consumption, high gain and also lower noise value in the filter circuit.

4. Conclusion

A reconfigurable filter design with tunable passband has been proposed in this paper. The proposed reconfigurable filter works on the principle of digital current control source (DCCS). In the previously reported works every DCCS depends entirely on the digital control oscillator (DCO) circuit to operate but in our design the DCCS functions independently and efficiently. Moreover the frequency ranges of previous designs are around 0.1 Ghz to 3 Ghz using DCO which is improved to the range of 0.1Ghz to 15Ghz using DCCS. The D Flip Flop is acting as the energy supplier by providing the word counts in the form of 0's and 1's.The 16 bit range of word count is providing the range for frequency to operate, which is fully digital in nature and also free from any anomalies or mismatch. The counters in the flip flop perfectly matches the frequency ranges and provides smooth reconfiguration. Thus reducing area in size of the project and also no impact of negative feedback occurs in our circuit. Moreover, Schmitt trigger is used here for the first time in such circuit, which reduces the noise in the signal thereby making it suitable for transmitting. Also the circuit is designed to be inductor less hence it can be claimed to be an area efficient one. The performance comparison with recently reported works clearly shows the efficacy of this filter.

The proposed first order voltage mode all pass filter has achieved a group delay of approximately 1.62ps with a bandwidth of 12.6 GHz. The static power consumption of the circuit is only 2.52mW under a 2V supply. Also, the range of operating frequency is 0.1-15 GHz and the circuit has achieved a gain of 15.5dB with a minimum noise factor of only 6.65μV. Moreover the leakage current of the circuit is only±614.57nA, which justifies the stability of the filter circuit.

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TABLE 4. Performance summary and comparison between similar all pass filters.

Reference	Technology	Mode	Order	Frequency (GHz)	Max. Delay (ps)	Bandwidth (GHz)	Power consumption (mW/V)	Gain (dB)	Noise (μV)
[10]	140nm CMOS	Voltage	1st	1-2.5	550	1.75	10^2/1.5	1.4	N/A
[14]	SiGe2RFHBT	Voltage	2nd	3-10	75	4.1	38.8/2.5	4	N/A
[15]	130nm CMOS	Voltage	2nd	6-7	55	6	18.5/1.5	7.5	N/A
[16]	130nm CMOS	Voltage	1st	6-9	33	4	20.4/1.5	11	N/A
[17]	130nm CMOS	Current	1st	0.9-5.1	82	N/A	6.15/1.5	-22	N/A
[18]	180nm CMOS	Voltage	2nd	3-12	6	7.5	12/1.8	-8	N/A
[19]	65nm CMOS	Voltage	1st	0.4-2	30-57	7.7	2.74/2	-4.7	N/A
This work (Reconfigurable filter)	**65nm CMOS**	**Voltage**	**1st**	**0.1-15**	**1.62**	**12.6**	**2.52/2**	**15.5**	**6.65**

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