

A Self Threshold Voltage Compensated Rectifier for RF Energy Harvesting using 45nm CMOS Technology

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Abstract— A high frequency rectifier is the core of a RF energy harvesting system. It should offer a very good efficiency at low input power levels and to obtain that compensation of threshold voltage is a very important aspect. A threshold compensation scheme for MOSFETS for RF rectifier applicable in RF energy harvesting system is presented in this paper. The switching of the MOSFET is improved with overall enhancement of output rise time of the system. The design emphasis is to have a simplified circuit without the requirement of any external source so as to achieve self-sustainability in the true sense. The rectifier circuit is derived from the basic Dickson charge pump model and is evaluated using 45nm CMOS process. The design has utilized Metal Oxide Semiconductor Field Effect Transistor instead of basic diodes which ensures low power along with fabrication feasibility. The maximum measured PCE of the design is obtained to be 33% at 4dBm input power level at 500Mhz frequency with 1 Kilo Ohm load resistance. The output transient response rise time has been measured to be 85ns at 500MHz and 50.10ns at 1Ghz.

Keywords—Power Conversion Efficiency, Peak to Peak Voltage, Dickson Charge Pump, Threshold Value.

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1. Introduction

Radio frequency (RF) energy harvesting is becoming a very important research area in the advent of green communication. The basic idea of implementation of RF energy harvesting system is to avoid external batteries or connection to any other power source [1,2,3]. This makes the communication nodes self-sustainable in terms of power and eliminates the difficulties in remote locations. Among all other renewable sources RF energy harvesting is a promising candidate with advantages of flexibility and portability. The RF energy harvesting system consists of a receiving antenna, a RF rectifier to convert the RF energy into DC energy and a power management unit to manage the harvested power. This is shown in figure 1. The output DC energy can be used by any load or can be stored in capacitors or external batteries. With the advancement of communication, along with faster and reliable data transfer mechanisms, energy management and conservations are getting more attention and is becoming a major and indispensable part of communication research. As self-sustainability to communication nodes is a very important aspect, RF energy harvesting must play a powerful role.

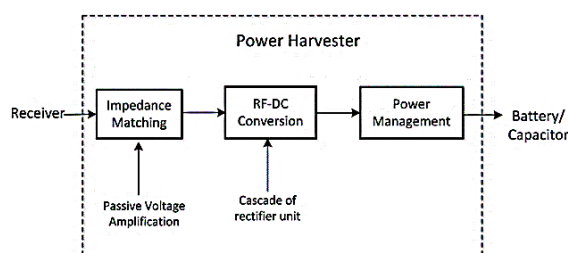


Figure 1: Block diagram of a RF energy harvesting system

The overall performance of the RF energy harvesting system is based on the sensitivity and the overall efficiency. The rectifier circuit is one of the main blocks that is responsible for determining the overall performance of an RF harvesting system. Recently, there has been an increased demand for highly-sensitive and highly-efficient rectifier circuits. Rectifier's sensitivity is defined as the lower limit input power level at which the rectifier is able to operate. The efficiency of a rectifier circuit indicates how well the rectifier is capable of converting the received RF power into dc power along with self-loss of power in the rectifier.

Design of a reconfigurable rectifier will also give a wide PCE response for a wide input power range. Gradually increasing the efficiency of the RF EH system. In this paper, the design of a reconfigurable rectifier with circuit-based solution for threshold reduction of the devices is implemented. The maximum measured PCE of the design is obtained to be 33% at 4dBm input power level at 500MHz frequency with 1 Kilo Ohm load resistance. The output transient response rise time has been measured to be 85ns at 500MHz and 50.10ns at 1Ghz. Further details of the theory, design, and experimental results for the circuit are given in following sections.

2. Proposed Design

2.1 The Charge Pump

The rectifier plays a signification role in the RFEH system. So, the prime objective of this work is to develop a rectifier with faster response time that is to develop certain technique for effective threshold compensation and better conversion efficiency. Fig. 2 shows the circuit schematic of a single stage Dickson charge pump. In order to find the optimum device sizes a single stage Dickson charge pump [10] was examined.

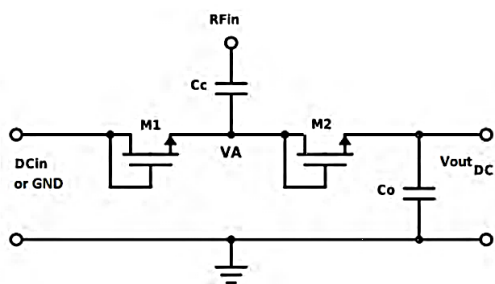


Figure 2: Dickson Charge Pump

A single-stage Dickson charge pump rectifier consists of two NMOS transistors, M1 and M2, one coupling capacitor (Cc), and one multiplying/output capacitor (Co). The RF signal is applied to RF input terminal. The DC input node is connected to an external DC supply or it is grounded as per requirement. The RF-to-DC conversion in the charge pump is during the first negative half cycle (as $V_{RF} < V_{TH}$), turns on M1 and Cc charges until the voltage across its nodes is equal to the amplitude of the RF input signal and As the RF input reaches its positive half cycle (where $V_{RF} > V_{TH}$). M2 turns on allowing Co to charge through the input RF signal and through the Cc. The charged Cc gets discharged into Co. At this point, the potential of VA is

$$V_A = 2V_{RF} - V_{TH} \text{-----(1)}$$

where VRF is the amplitude of input signal and the output voltage is

$$V_{out} = 2(V_{RF} - V_{TH}) \text{-----(2)}$$

From equation (1) and (2), it is observed that the threshold voltage of the used transistors (V_{TH}) plays a very important role in the value of the output voltage. Hence, lower the threshold voltage of transistors is, the higher is the magnitude of the output voltage.

2.2 The Proposed Rectifier

Fig. 3 shows the proposed threshold compensated rectifier constructed by cascading a comparator circuit with a Dickson charge pump. The positive terminal of the comparator has an input feedback from the output of the Dickson charge pump. The output of the comparator circuit is providing the bias voltage to the M1 device of the Dickson charge pump.

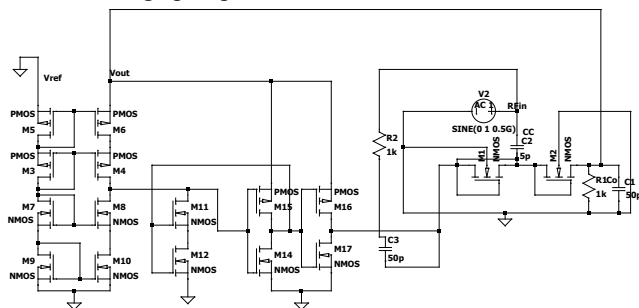


Figure 3: Proposed Rectifier Circuit

The comparator circuit provides an in phase bias voltage with respect to the RF input signal to the M1 device of the charge pump. This in phase bias voltage always remains in

the positive phase which results in providing a alternating bias voltage to trigger the M1 device of the charge pump.

3. Experiment Results

3.1 Comparator output voltage

In Fig. 4 the output voltage waveform of the comparator circuit with reference to RF input signal is shown. V(n006) is the output of the comparator and V(n002) is the input RF signal.

It is observed from the figure above that the comparator provides a phase bias voltage at similar phase as that of input RF signal. This output of the comparator is providing a bias voltage of average value 742.18mV to the drain gate node of M1 device.

For the conditioning of the comparator output signal the RC circuit is implemented in the circuit. The comparator is grounded in its inverted terminal and the non-inverting terminal is an input of the looped back voltage of the output of the Dickson charge pump.

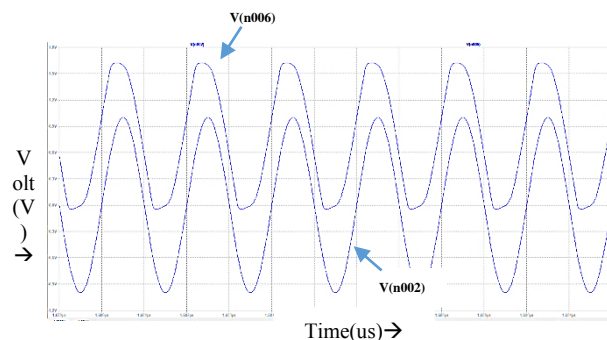


Figure 4: Waveform of the output of the comparator and the input RF signal

The output signal cannot be directly feedback to the M1 device because if it is done there will be more negative node voltage and leakage current will develop at M1 drain node. The comparator serves a more positive output voltage which serves its purpose of pre biasing the device near its threshold region. So, at even lower magnitude voltage of the input RF signal M1 gets into saturation region. It is observed that the output of the comparator gives a higher peak to peak voltage than the RF input signal this is due to internal gain of the comparator. The output current of the comparator is 2.3028mA RMS value.

The manually set Vth of the device is 429mv. In the traditional Dickson charge pump the RF signal has to reach this value to make the device on. But now when the comparator output voltage reaches 721m V the RF signal value is at this point of time is approx. -287.12301mV. Therefore, at this point the overall voltage is more than the threshold voltage. The device will remain in on state until the RF input value reaches -75.65mV. Hence the device is on much faster than in the traditional configuration. This enhances the switching time and on state duration of the device.

3.2 Rectifier parameter analysis

The first parameter that needed to be selected was the device length Fig. 5 shows the output voltage variation when the transistor length is varied from 65nm to 500nm.

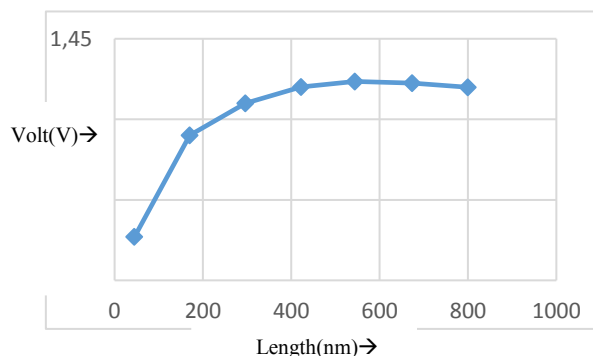


Figure 5: Simulated output voltage variation versus channel length

It is observed that after 500nm the output voltage of the rectifier starts to degrade. The second parameter to be examined is the transistor width. Fig. 6 shows the alterations in output voltage when channel width is swept from 65nm to 2000 nm.

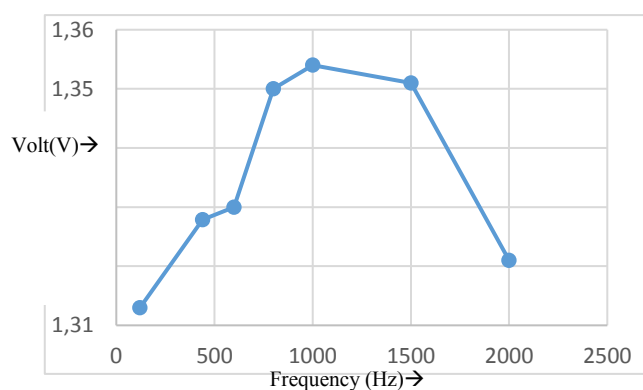


Figure 6: Simulated output voltage variation versus channel width

So, it is clear from the graph that after 1000nm the output voltage of the rectifier starts to degrade. From these two figures the aspect ratio of the devices was chosen.

Initially the operating frequency band of the proposed design is analyzed in the simulation platform. The RF source frequency here is swept in the RF range 20KHz to 300GHz. The magnitude and phase plot of the frequency sweep is given in the Fig. 8 below.

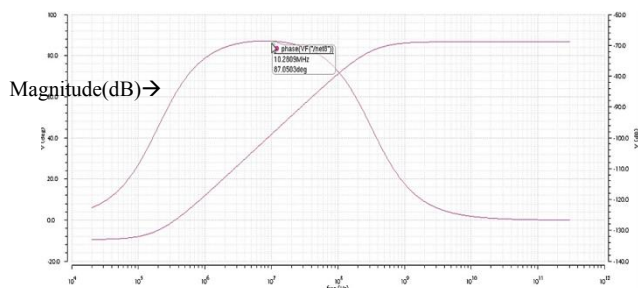


Figure 8: Magnitude vs Phase plot

As a result, it is observed that the gain of the rectifier remains constant after 1 GHz so we choose the operating frequency range for the circuit to be between 200MHz to 1GHz.

The load resistance of the rectifier is swept from 500 ohms to 100K ohms. The graph in the Fig. 9 below shows different varying parameters of the circuit with variation of the load resistance.

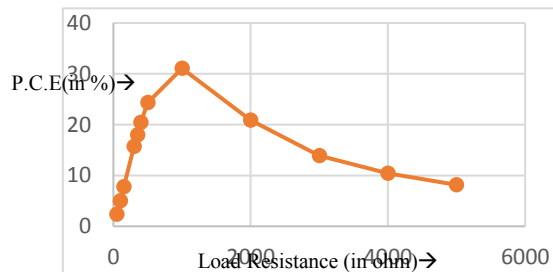


Figure 9: RL vs PCE graph

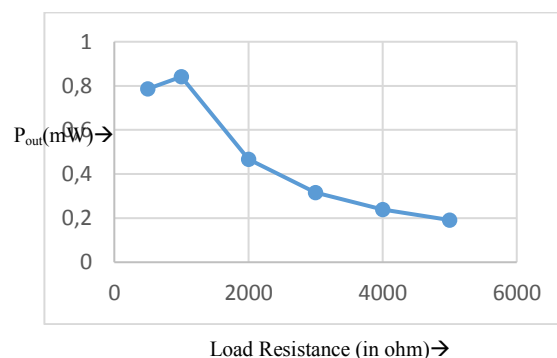


Figure 10: RL vs P_{out} graph

Fig 10. shows the Load Resistance vs Output Power graph. Here it is observed that at 1 Kilo ohm load resistor value maximum power is delivered to the load. The calculated input power at this value is 4.09 dBm.

3.3 MOSFET Output Rise Time

Turn on time $t_{on} = t_d (on) + t_r$ (Rise time)

It is clear from the above equation that if the rise time (t_r) of the MOSFET is increase then the turn on time of the device also increases. So, the rise time for the conventional Dickson Charge pump is $t_r = 98.6309607$ ns

But, in the proposed circuit the turn on time at 500MHz and 1 GHz operating frequency is 85.055859 ns and 50.10 ns approx.

The plot for the rise time from 100MHz to 1GHz is shown in Fig. 11 below

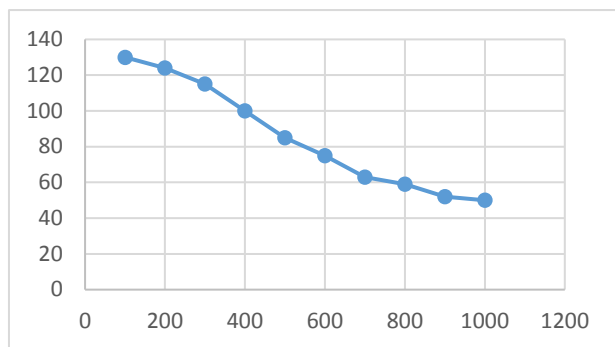


Figure 11: Frequency vs Rise time plot

It is observed from the above graph that the rise time keeps degrading when the Frequency is higher. At 500 MHz the PCE of the rectifier calculated is 33% at 4dBm input power and at the 1000 MHz the PCE farther degrades to 26% at 5.7dBm input power. Farther increasing the operating frequency, the rise time will certainly fall which is desired but at the cost of PCE degradation.

The Optimized parameters of the proposed rectifier is shown in Table I below.

Frequency (MHz) →

TABLE I. Optimized parameters of the proposed rectifier

Parameter	Optimized Value
MOSFET Channel Length	45nm
MOSFET Channel Width	120nm
Operating Frequency	200 MHz to 1 GHz
Load Resistance	1kilo ohm
PCE	33% (Max)
M1 Device Turn on voltage	-287.12301mV
Comparator output current	2.3028 mA (RMS)
Coupling Capacitor (CC)	5pf
Output Capacitor (Cout)	70pf
Output Rise time (tr)	85 ns at 500 MHz to 50 ns at 1 GHz

Hence, it is observed that the threshold voltage to trigger the M1 device of the charge pump is lowered from 400mv to -287.1 mV and the turn on period of the device is also increased.

Table II summarizes the various threshold level compensated rectifiers parameters for RF energy harvesting. It can be seen that our proposed rectifier achieves peak 33% efficiency at 4dBm input power and achieves an output rise time of 85.055859 ns at 500MHz and efficiency of 26% at 5.7dBm input power and achieves output rise time of 50ns at 1 GHz. Compared to other designs the proposed rectifier achieves better efficiency and certainly lowered threshold value for better switching of MOSFET operating regions.

TABLE II. Performance Comparison with other Reported Works

Technology	Reference	Frequency	Input Power (dBm)	Output Voltage	Load (K ohm)	PCE (max)
65 nm CMOS	Single Stage Dickson	500	-11.39	201.2 mv	10	11.25 %
180 nm Cmos	[7]	433	-5 to -9	--	10	22% to 30 %
130 nm CMOS	[8]	--	-15	1v	1000	32%
65 nm CMOS	[9]	900MHz and 2.4GHz	-18	1v	1000	16.8 %
45 nm CMOS	This Work	500MHz	4	916.698mv	1	33%

4. Conclusion

The design is implemented using 45nm CMOS process. The threshold compensation is achieved by a scheme that completely removes the requirement of any other external source and thereby making it fully self-sustainable. The proposed design has attained a PCE of 33% at 4 dBm input power and 26% at 5.7dBm input power at 10K ohm load resistance. The design gives a better magnitude gain after 1 GHz which leads to better sensitivity at low input power levels. The average output voltage at 500MHz input is 916.698mv and at 1GHz the average output voltage is 992mv. The aspect ratio of the devices is 3/8. The output rise time is measured to be 85.055859 ns at 500MHz and 50.10 ns at 1GHz. This validates the suitability of the circuit in RF frequencies with an acceptable PCE and faster response.

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