We can see that the curves 1, 2, and 3, which correspond to the switch points before the optimal point (4) have not intersections. On the other hand, the curves 5, 6, and 7 that are based on the switch point after the optimal one have intersections and each this curve lies upper the curve 4 till some time point. It means that from this time moment the graph *W(t)* for the optimal switch point lies below all of other graph. So, from one hand the optimal switch point corresponds to a minimal computer time, from the other hand, this point corresponds to the graph of *W(t)* function that lies below all of other graphs. This property anew serves as a principal criterion for the optimal switch point selection. The function *W(t)* that corresponds to the optimal switch point has a maximum absolute value leading off the 15th integration step. It means that from this integration step we can confidently predict the optimal switch point position that leads to the minimal computer design time. The time gain of a complex strategy consisting of MTDS and TDS with an optimal switching point between them at the 9th integration step compared to TDS is 40.4 times.

Next example corresponds to the one-stage transistor amplifier in Fig. 7.

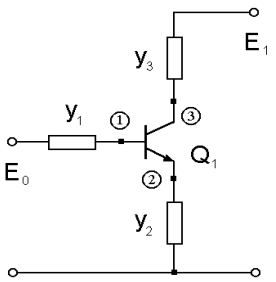

Fig. 7 One-stage transistor amplifier

The vector *X* includes ten components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4 = V_1$, $x_5 = V_2$, $x_6 = V_3$. The model of this network (2) includes three equations (*M*=3) and the optimization procedure (5) includes six equations. The total structural basis contains eight different design strategies. The control vector includes five control functions: $U=(u_1, u_2, u_3)$. The Ebers-Moll static model of the transistor has been used [16]. When using TDS (*U*=(000)), the CPU time is 4.17 seconds.

We will search for the optimal strategy, consisting of two parts MTDS (*U*=(111)) and TDS (*U*=(000)).

Fig. 8 shows the behavior of the functions *V(t)* and *W(t)* during the design process with different switch points.

The behavior of these functions helps us to determine the optimal position of the control vector switch point. We have been analyzed the strategy that consists of two parts. The first part is defined by the control vector (111) that corresponds to MTDS and the second part is defined by the control vector (000) that corresponds to TDS. The optimal switch point was an aim of the analysis. The consecutive change of the switch point was realized for the integration step number from 2 to 50. The behavior of the functions *V(t)* and *W(t)* for the switch points from 33 to 39 are shown in this figure and the data, which correspond to these graphs, are presented in Table 3.

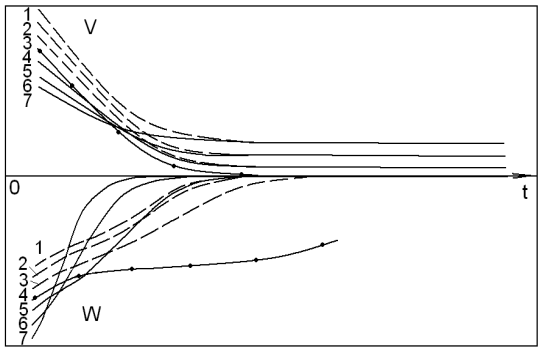

Fig. 8 Behavior of the functions *V(t)* and *W(t)* during the design process for seven different switch points (from 33 to 39) for network in Fig. 7

Table 3. Iterations number and computer time for strategies with different switch points for one-stage transistor amplifier

N	Switch point	Iterations number	Total design time (sec)
1	33	2433	0.404
2	34	2180	0.361
3	35	1748	0.289
4	36	61	0.01
5	37	1705	0.281
6	38	2111	0.349
7	39	2349	0.389

The analysis shows that the optimal switch point corresponds to the step 36 (graph with dots). The computer design time has a minimal value for this step. The function *W(t)* has a maximum absolute value for the optimal switch step (number 4) leading off the 55th integration step. It means that from this integration step we can confidently

predict the optimal switch point position that leads to the minimal computer design time. The time gain of a complex strategy with an optimal switching point at the 36th integration step compared to TDS is 417 times.

The last example corresponds to the two-stage transistor amplifier in Fig. 9.

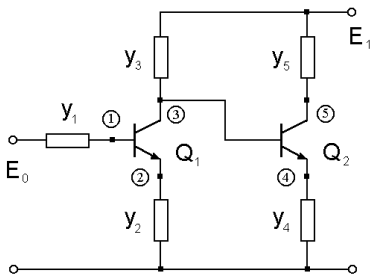

Fig. 9 Two-stage transistor amplifier

The vector X includes ten components: $x_1^2 = y_1$, $x_2^2 = y_2$, $x_3^2 = y_3$, $x_4^2 = y_4$, $x_5^2 = y_5$, $x_6 = V_1$, $x_7 = V_2$, $x_8 = V_3$, $x_9 = V_4$, $x_{10} = V_5$. The model of this network (2) includes five equations (M=5) and the optimization procedure (5) includes ten equations. The total structural basis contains 32 different design strategies. The control vector includes five control functions: $U=(u_1, u_2, u_3, u_4, u_5)$. When using TDS ($U$=(00000)), the CPU time is 967.4 sec.

We will search for the optimal strategy, consisting of three parts MTDS (U=(11111)), TDS (U=(00000)) and MTDS (U=(11111)) with two switch points.

Fig. 10 shows the behavior of the functions *V(t)* and *W(t)* for some design strategies with different switch points including the optimal one.

The data, which correspond to these graphs, are presented in Table 4.

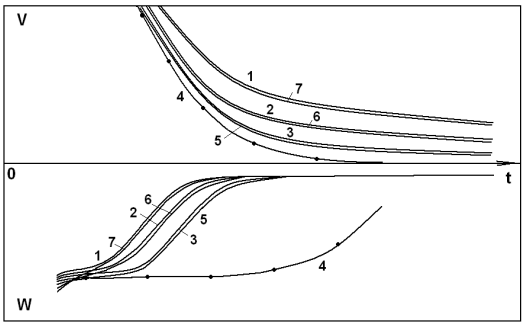

Fig. 10 Behavior of the functions *V(t)* and *W(t)* during the design process for seven different switch points (from 7 to 13) for network in Fig. 9

The integration of the system (5) was realized by the optimal integration step.

Table 4. Iterations number and computer time for strategies with different switch points for network in Fig. 9

N	Switch point 1	Switch point 2	Iterations number	Total design time (sec)
1	7	8	4900	9.912
2	8	9	4486	9.113
3	9	10	3785	7.691
4	10	11	1354	2.742
5	11	12	3618	7.341
6	12	13	4424	8.981
7	13	14	4882	9.893

In this case the quasi-optimal control vector includes two switching points. We changed the control vector from (11111) to (00000) and from (00000) to (11111). The consecutive change of the switching point was realized for the integration step's number from 2 to 20.

The behavior of the functions *V(t)* and *W(t)* for the optimal switch steps and some steps near the optimal confidently detect the optimal position of the switch points.

The time gain of a complex strategy with optimal switching points at the 10th and 11th integration steps compared to TDS is 352.8 times.

We observe a specific behavior of the function *W(t)* near the optimal switch point's position. Before the optimal switching points the function *W(t)* graphs are "parallel". Function *W(t)* has the maximum negative value for the optimal switch points. The graphs of the function *W(t)* that correspond to the optimal switch point's position (number 4) and before the optimal position (1, 2 and 3) have not intersection. After the optimal points the graphs of the function *W(t)* intersect the graphs that correspond to the optimal switch point and before the optimal one. It means that we can detect the optimal position of the switch points during the initial design interval.

Thus, the optimal structure of the control vector, that is, the structure of the time-optimal design strategy, can be determined by analyzing the relative time derivative of the Lyapunov function during the initial time interval of the design process.

Summarizing all the results obtained, we can conclude that the behavior of the time derivative of the Lyapunov function of the design process allows

us to determine the optimal switching points of the control vector, that is, the optimal or quasi-optimal structure of the control vector. This means that the optimal structure of the control vector can be obtained during the initial interval of the design process.

5 Conclusion

The task of constructing a minimum-time design algorithm can be adequately solved on the basis of control theory. The design process in this case is formulated as a controlled dynamic system. The Lyapunov function of the design process and its time derivative contain sufficient information to select more promising design strategies from the infinite number of different design strategies that exist in the generalized design methodology. A special function W (t) was proposed to predict a time-optimal design strategy. This function can be used as the main tool for constructing the optimal sequence of control vector switching points. The solution to this problem allows you to build a system design algorithm in minimal CPU time. Moreover, the time gain of the optimal strategy in comparison with the traditional strategy is 2–3 orders of magnitude.

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