

# Automated control systems of increased reliability based on the use of configurable functionally complete tolerant logic elements

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*Abstract:* The article deals views one of the options to improve the reliability of automatic control systems through the use of the quality of the circuitry complete functional tolerant look-up table (FCTLUT) with the ability to save original function in case of transistor failure. The authors present the analysis of the features offered with FCTLUT elements included in the FPGA for high-reliability applications in the case of restrictions on the length of the sequential chain of transistors. The article has the conclusion about the preference of FCTLUT on the probability of fail-safe operation over triple redundancy structures.

*Keywords:* logic element, FPGA, LUT, transistor, functionally–complete tolerant element logical (FCTLUT), redundancy, probability of failure, triple redundancy, quadruple redundancy.

## 1 Introduction

The tasks performed by modern automatic control systems are quite diverse, including the tasks of managing various processes of increased responsibility. Failures in such systems can lead to catastrophic consequences. The examples of such systems can be control systems used in such industries as weapons, rocket and space and energy industries, transport management, hazardous industries, etc. Thus, the actuality of relevance of the issue of improving the reliability of automatic control systems of various systems it becomes obvious. One of the alternatives to solve this problem can be the use of logical elements with the property of increased reliability as the element base underlying the development of control systems.

The issue of developing such logic elements is associated with a number of problems, such as technological limitations of Mid and Convey on number of consequently connected CMDS transistors in design of large-scale integration circuits – LSI [1]. According to [1] more than 4 transistors in consequent chain are not permitted. Same limitation is observed in logical elements of gate-array chips [2-5], using CMDS transistors – Fig.1.

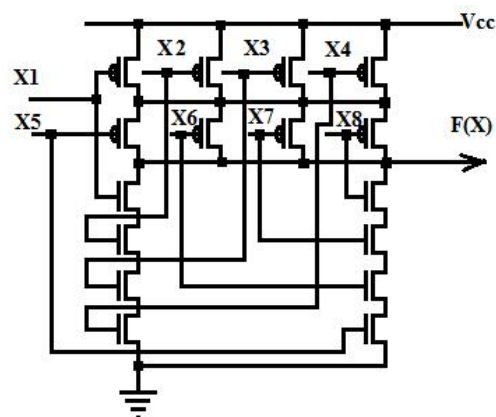


Fig. 1. CMDS implementation of 4AND-NOT elements with four transistors in «Zero volts» bus connection line

Meanwhile even stricter limitation is considered preferred – not more than 3 transistors. The point is that the longer is the chain the lower is interference immunity. «4 transistor» limitation is fulfilled also in logical elements of field-programmable gate arrays FPGA [6, 7]. That is why implementation of function of 5, 6 and more variables requires cascading of elements implementing function of 4 variables [8, 9]. There is information on weakening

of «4 transistor» limitation to 5 in micrometer range projects, and even to 7 for submicron projects) [10]. Nevertheless, in special applications, especially operation at lowered supply voltage and demanding high fail-safety, «3 transistor» limitation persists [11].

This creates problems for structural redundancy at transistor logic level [12,13], as in this case number of transistors in sequential chain should be increased 2 times, and if for «4 transistor» limitation it is possible to build a redundant element with binary operation, then for «3 transistor» limitation it is impossible. Such limitation is acceptable only for implementation of invertors, for example, static RAM cell [14], but inverter has no functional completeness. In this respect, it is interesting to resolve this problem, especially in relation of creating fail-safe circuits [15].

**2 FPGA LUT logic cell**

Logic element – LUT (Look Up Table) cell of FPGA implements any function of one variable and is built on basis 2-1 multiplexer – Fig.2:

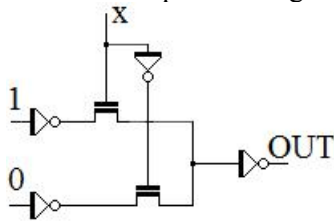


Fig. 2. LUT1 –multiplexer 2-1

Adjustment is performed by feeding constants to inverter inputs 0,1. For building LUT2 – 4-1 multiplexer three LUT1 are necessary – Fig.3:

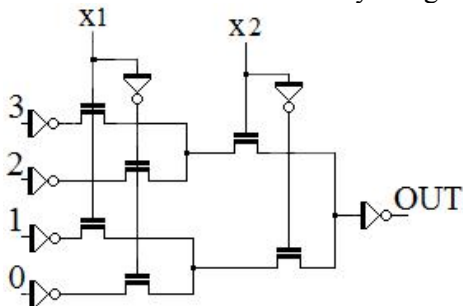


Fig. 3. LUT2 – 4-1 multiplexer

In case of «4 transistor» limitation invertors are not necessary on input of last, third LUT1. Adjustment is performed by feeding constants to inverter inputs 0,1,2,3. Similarly LUT3 –8-1 multiplexer is build – Fig.4:

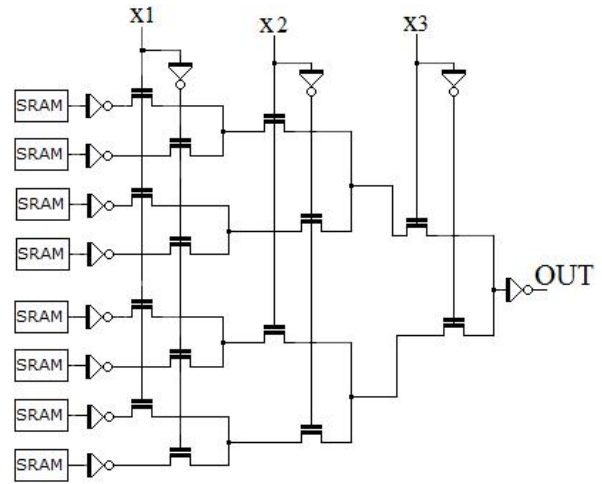


Fig. 4. LUT3 – 8-1 multiplexer

Fig.4 shows cells of configuration SRAM.LUT4 – 16-1 multiplexer is shown at Fig.5:

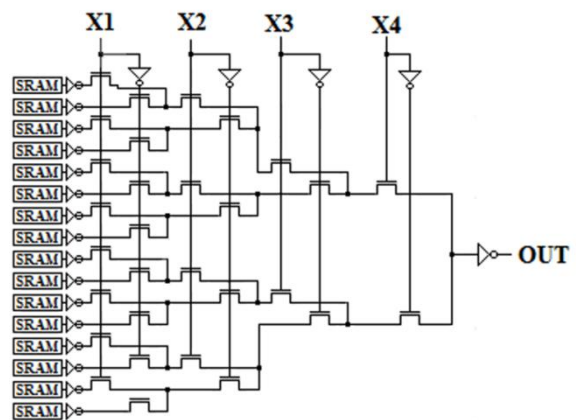


Fig. 5. LUT4 – 16-1 multiplexer

To further increase number of variables to 5, it is necessary to input invertors (signal restorers) at input of last LUT1, otherwise limitation is violated – Fig.6:

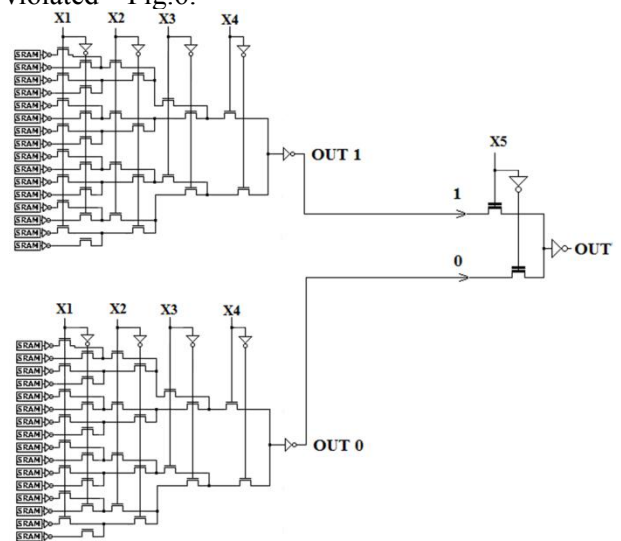


Fig. 6. LUT5 - 32-1 multiplexer

That means that restoration of signal coming over branches of transistor tree is provided for. In this case, adjustment of function will be inverted (three invertors in a branch). Similarly could be

built LUT6 – 64-1 multiplexer and LUT7 – 128-1 multiplexer. There is information on using even LUT8–256-1 multiplexer.

### 3 Evaluation of complexity of decomposing FPGA LUT logic cell

Source transistor tree without redundancy («ideal» complexity, as this could be only up to  $n=4$ , not more) is evaluated by expression:

$$L_n = 2^n \cdot 8 + 2^{n+1} + 2n. \quad (1)$$

When decomposing  $n$ -tree by  $k$  LUT,  $k \in \{1,2,3,4\}$ ,  $n \geq k$ ,  $n \leq 8$ :

$$L_{n,k} = 2^n \cdot 8 + (2^{k+1} + 2k) \cdot 2^{n-k} + (2^{2^{n-k}+1} + 2^{n-k+1}) + 2n, \quad (2)$$

where  $2^{k+1}$  - complexity of tree  $k$  LUT,  $2k$  – number of transistors in  $k$  inverters, such trees are necessary  $2^{n-k}$ , to combine  $2^{n-k}$  trees received during decomposing are necessary more LUT at  $2^{n-k}$  inputs (which are also could be decomposed), accordingly

$$\text{complexity } 2^{n-k+1} + 2 \cdot 2^{n-k} = 2^{n-k+2},$$

where  $2^{n-k+1}$  - complexity of tree with output inverter,  $2 \cdot 2^{n-k} = 2^{n-k+1}$  – complexity of input inverters. Here we shall not proceed further than  $n=8$ , that is why it is supposed that additional LUT will «fall» within required decomposition parameters by  $k$  LUT,  $k \in \{1,2,3,4\}$ . Comparison of complexity of decomposing of  $n$  LUT by  $k$  is shown at Fig.7:

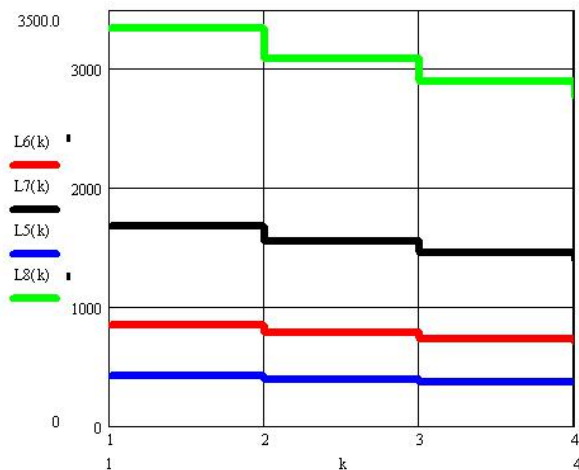


Fig. 7. Comparison of complexity of decomposing of  $n$  LUT by  $k$

The result is quite expectable – the larger is construction block – the smaller are costs for implementing complex LUT at 5, 6, 7 and 8 variables.

Temporary delay at decomposition is evaluated by length of maximal path in logic element from input to output. Here without decomposing – at «ideal» option (1) we have:

$$T_n = n + 2. \quad (3)$$

In case of decomposition path in transmitting transistors also is evaluated by value  $n$ , but due to

additional inverters at input and output of LUT chain (Fig.6) it will be greater:

$$T_{n,k} = n + 2 \left\lceil \frac{n}{k} \right\rceil. \quad (4)$$

Graphs of variation (4) at  $n=5 \dots 8$  are shown at Fig.8:

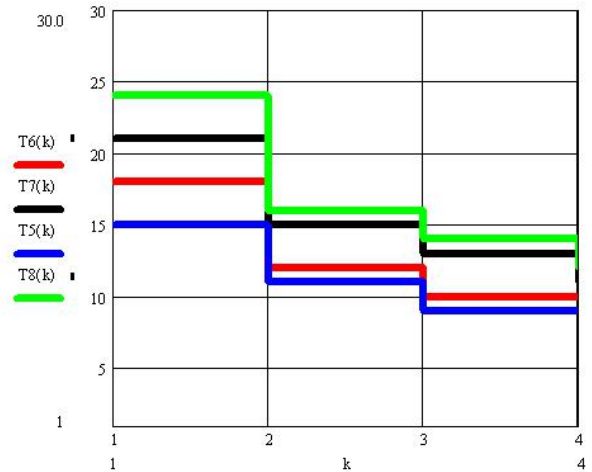


Fig. 8. Comparison of time spent for decomposition  $n=5 \dots 8$  by  $k$

Graphs of variation(4) at  $n=7 \dots 10$  are shown at Fig.9.

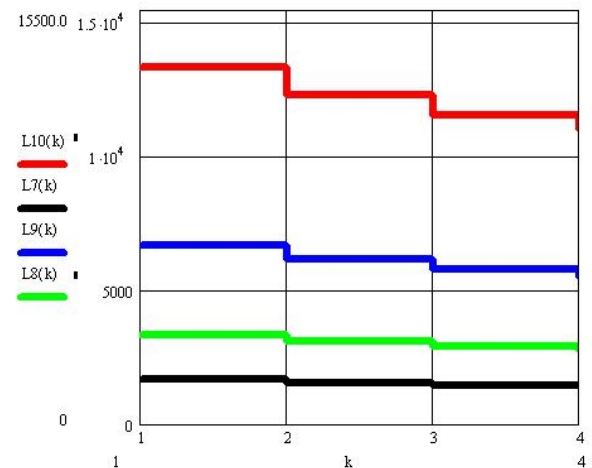


Fig. 9. Comparison of time spent for decomposition  $n=7 \dots 10$  by  $k$

### 4 Fail-safe FPGA FCTLUT

To obtain a fail-safe functional-fulltolerant logic element PTLA [13-15] – FPGA FCTLUT1 so-called quadruple redundancy of transistors may be proposed – Fig.10:

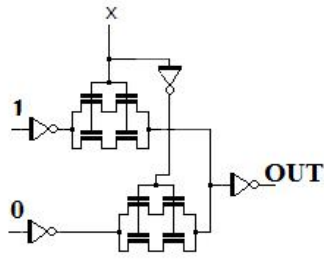


Fig. 10. Fail-safe FCTLUT1 with transistor redundancy

Such redundancy leads to fact that required «4 transistor» limitation is fulfilled only to LUT2 – Fig.11:

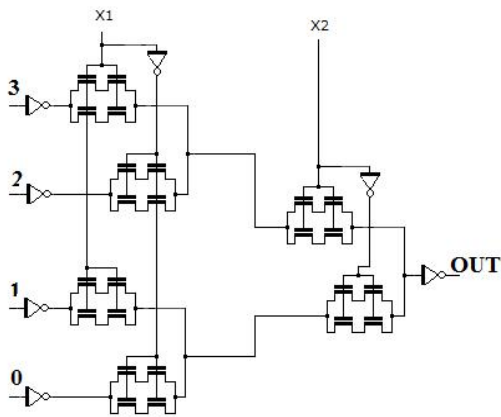


Fig. 11. Fail-safe FCTLUT2 with transistor redundancy

So, for LUT3 already signal restoration and inverse adjustment are required – Fig.12:

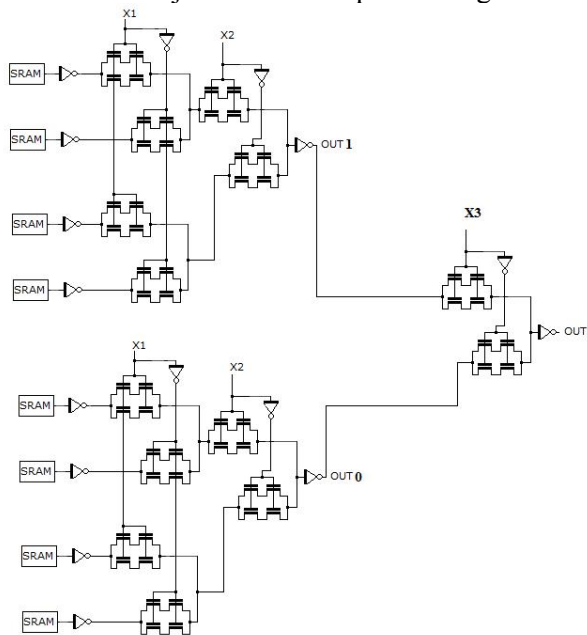


Fig. 12. Fail-safe FCTLUT3

In case of «3transistor» limitation option of Fig.12 already fails, that is why restoration is necessary after each LUT1 – Fig.13:

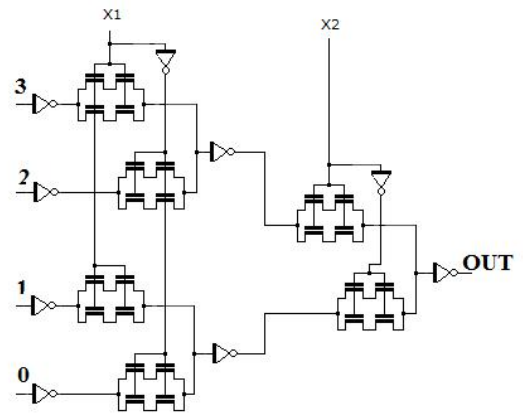


Fig. 13. Fail-safe FCTLUT2 with limitation of 2 transistors in chain

**5 Evaluation of complexity of FPGAFCTLUT with limitation of 2 transistors in chain**

When decomposing n-tree by 2 FCTLUT,  $n \geq 2$ :

$$L_{n,2} = 2^{n+5} + (2^3 + 4) \cdot (2^n - 1) + 8n(5),$$

where  $2^n \cdot 32 = 2^{n+5}$  – complexity of adjustment (6\*4=24 transistors in one fail-safe SRAM, 2\*4=8 – complexity of fail-safe inverter, in total  $2^n$ ),  $2^{2+1} = 2^3$  – complexity of 2LUT tree, 4 – number of transistors in fail-safe output inverter, such 2LUT for n tree ( $n \geq 2$ ) is necessary  $2^n - 1$ ,  $8n$  – number of transistors in input variable inverters. Graphs of variation of probability of fail-safe operation of 4LUT without redundancy  $P(t)$  of proposed FTLUT  $P(t)_{ftm}$ , with triple redundant scheme with one majority  $P3(t)$  and with triple redundant scheme with three majorities  $P3.3(t)$  at failure rate 10 in degree minus five 1/hour are shown at Fig.14:

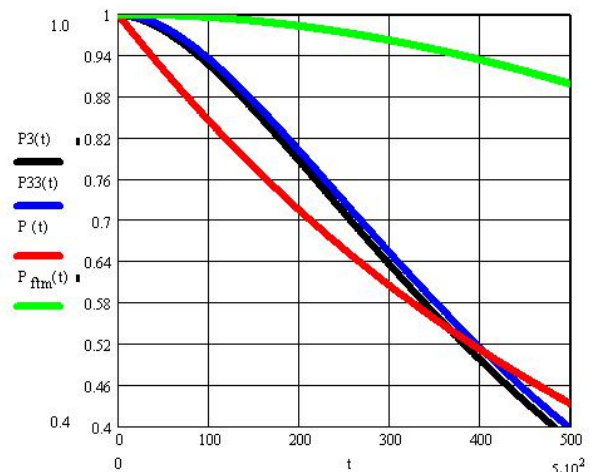


Fig. 14. Graphs of variation of probability of fail-safe operation of 4LUT without redundancy  $P(t)$  of proposed FCTLUT  $P_{ftm}(t)$ , with triple redundancy scheme with one majority  $P3(t)$  and with triple redundancy scheme with three majorities  $P3.3(t)$  at failure rate 10 in degree minus five 1/hour

Graphs of variation of probability of fail-safe operation of nLUT with decomposition without



redundancy  $P(t)$  of proposed FCTLUT  $P_{f_{tm}}(t)$ , with triple redundancy scheme with one majority  $P_3(t)$  and with triple redundancy scheme with three majorities  $P_{3.3}(t)$  at failure rate 10 in degree minus five 1/hour are shown at Fig.15:

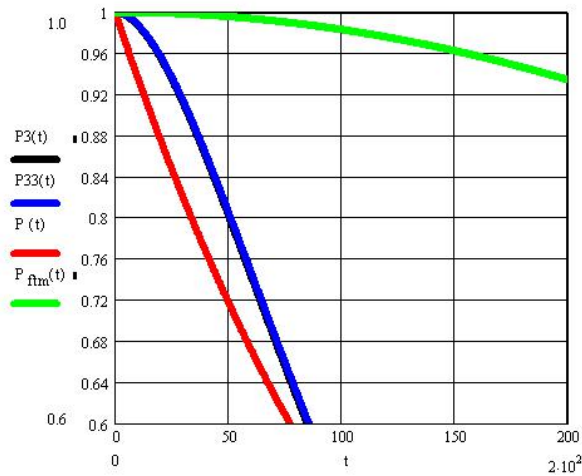


Fig. 15. Graphs of variation of probability of fail-safe operation of 6LUT with decomposition without redundancy  $P(t)$  of proposed FCTLUT  $P_{f_{tm}}(t)$ , with triple redundancy scheme with one majority  $P_3(t)$  and with triple redundancy scheme with three majorities  $P_{3.3}(t)$  at failure rate 10 in degree minus five 1/hour

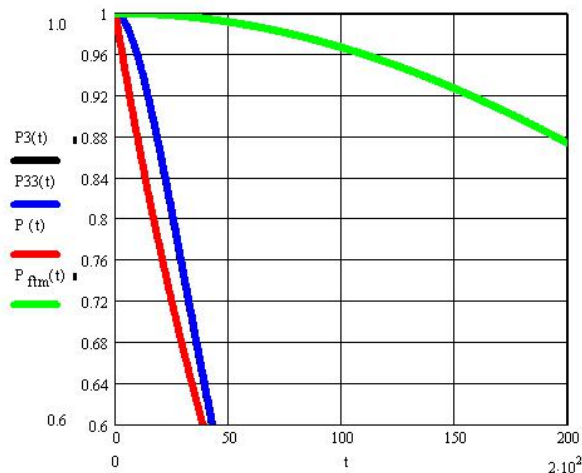


Fig. 16. Graphs of variation of probability of fail-safe operation of 7LUT with decomposition without redundancy  $P(t)$  of proposed FCTLUT  $P_{f_{tm}}(t)$ , with triple redundancy scheme with one majority  $P_3(t)$  and with triple redundancy scheme with three majorities  $P_{3.3}(t)$  at failure rate 10 in degree minus five 1/hour

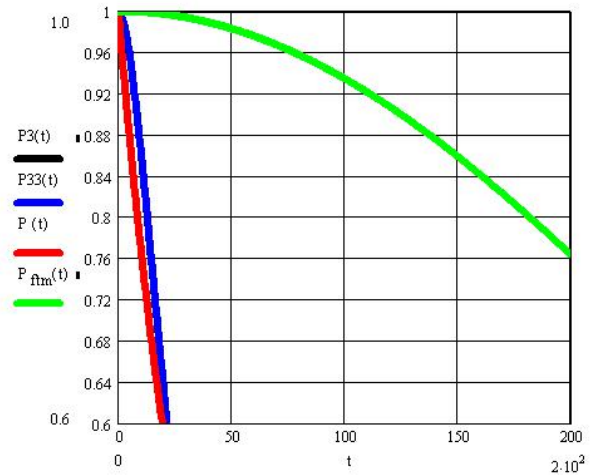


Fig. 17. Graphs of variation of probability of fail-safe operation of 8LUT with decomposition without redundancy  $P(t)$  of proposed FCTLUT  $P_{f_{tm}}(t)$ , with triple redundancy scheme with one majority  $P_3(t)$  and with triple redundancy scheme with three majorities  $P_{3.3}(t)$  at failure rate 10 in degree minus five 1/hour

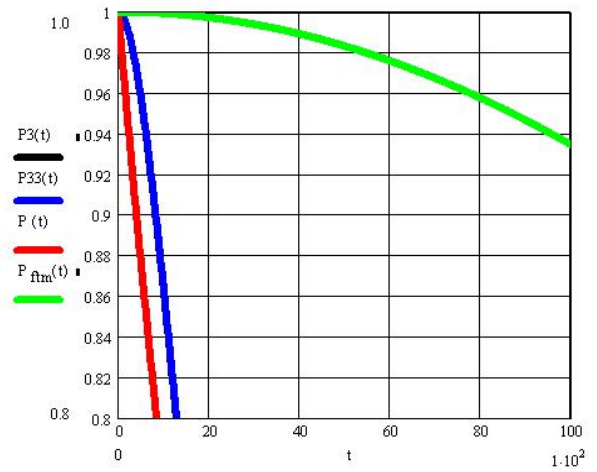


Fig. 18. Graphs of variation of probability of fail-safe operation of 4LUT without redundancy  $P(t)$  of proposed 4LUT-FCTLUT  $P_{f_{tm}}(t)$ , triple redundancy scheme  $P_3(t)$  at failure rate 10 in degree minus five 1/hour

## 6 Conclusions

So, application of configurable FCTLUT on basis of FCTLUT2 permits to provide for passive fail-safety while fulfilling limitation of «2 transistors in chain» in multistage LUT. Logic function of FCTLUT is preserved in case of failure of one transistor in each group of four transistors.

Such creation of groups of four transistors provides a higher probability of failure-free operation than tripling. Proposed FCTLUT on basis of FCTLUT2 may be used in so-called adaptive logic modules ALM FPGA [8] for RHBD (Radiation Hardening by Design) processors and devices for onboard digital computer complexes, providing for radiation resistance by architecture solutions [15]. It is proposed to apply similar approach also to configurable FCTLUT base matrix

crystals universal fail-safe logic element configurable by constants during one-time programming in case of rigid limitations of consecutive transistor chain length with simultaneous requirement of passive fail-safety.

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