Design of Delay Unit for Synchronizing EEG Signal with FPGA-based Hardware Accelerator

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Abstract: - The technology used for processing EEG signals from the brain for a specific application is called the brain-computer interface (BCI). This method has numerous applications as a non-intrusive signal capture technique. Hardware accelerators are used to implement an accurate and stable system for capturing these low-frequency signals, as EEG signal acquisition is highly sensitive, particularly in seizure detection. A critical challenge in this integration is precisely synchronizing EEG signals with the hardware accelerator to ensure real-time processing and accurate detection of epileptic seizures. Detecting a seizure from an EEG signal requires collecting much data from the brain's electrical activity. The general performance of the CPU is not enough to handle this massive data. So, the proposed system used FPGAs (Field-Programmable Gate Arrays) family Zynq 7000 series as a hardware accelerator. FPGAs offer the designer the benefits of custom hardware design, eliminating costly development expenses and time-consuming production processes. This article aims to propose a VLSI design using built-in IP cores provided by Xilinx and evaluate an EEG delay system that can synchronize the built memory of FPGA with the real-time data acquired from brain signals. The Experimental results demonstrate that the proposed approach enables the creation of a controllable delay platform with a minimum delay step of less than 1ns and a maximum delay time exceeding 200us, compared to skew, resulting in the efficacy of the delay unit in providing seamless synchronization, enhancing the overall performance of the EEG-based seizure detection system. The post-synthesis estimated power is 134mW, a setup time of 0.420nS, and a hold time of 5.713nS.

Key-Words: - EEG signals, FPGA, IP cores, set-up time, Hold time, Seizure, non-intrusive signal.

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1 Introduction

Seizure prediction is a difficult task that has been investigated for over 25 years. Many approaches are based on the study of electroencephalogram (EEG) signals and the development of machine learning methods, [1]. However, physiological data, such as EEG and ECG, containing seizures are generally rare and frequently contain abnormalities and noise.

In humans, the brain is the most important organ that controls the body's functionality; the neuroscience field has played a vital role in gathering information regarding the workings of the brain that helps in learning about human behavior and sudden changes in the body, [2]. The study of the functionality of the brain study alone can't be considered for the activities performed by the human body. During World War II, they study the body's functionality by practically observing the brain working on dead bodies using invasive methods by giving external stimuli. As this is not an appropriate approach, a brain-computer interface (BCI) technology is utilized to acquire and process these impulses, allowing for non-invasive signal acquisition and analysis, [3].

The acquired EEG signal through the interface should be stored in memory, or the data should be compared with the preexisting data for various applications. Performing operations on memory is essential in cognitive functions such as storing the acquired data, retrieving data, and making decisions. The interface system design is crucial for creating a precise and reliable system that connects EEG signals with memory efficiently. This interface enables the transfer of digital EEG data obtained from ADC of EEG signals, resulting in progress in neurofeedback, brain-computer connection, and the diagnosis of neurological disorders, [4].

The EEG signal interface is a challenging task. There are several parameters to be considered for interfacing. The first parameter to be considered is the EEG signal frequency obtained. The second parameter is the number of bits considered for interfacing in a single clock cycle. Based on the above parameters, signal delay is calculated, i.e., the time taken for EEG signals to propagate through the interface and reach the memory system. The calculation of signal delay affects the overall performance of the EEG-memory interface. Even a slight change in signal delay can introduce errors like data loss and miss alignment of data, thereby causing a lot of data misconception, which results in the overall performance of the interface. In order to solve these problems, it is necessary to make signal delay computations carefully to improve the EEG-memory interface performance. If the signal delay analysis is not done correctly, a single millisecond of change may cause data interface mistakes while handling a massive amount of data.

The data interface is done in serial communication, so while transferring the data, if there is a small change in data signal delay, the delay error will occur multiple times for further transfer. FPGA operating clock frequency should also be considered when interacting the EEG signal with FPGA signal delay. The proposed work aims to provide a detailed calculation for interfacing EEG signals with the inbuilt memory of FPGA. The computation results of various delay values are compared and explained clearly. This comparison between the theoretical calculation is based on the input EEG signal frequency, number of bits considered, and FPGA clock frequency, which differ a bit when implemented on hardware due to internal delay caused by the hardware RTL schematic circuit. To achieve high performance of the interface unit, it's always best to consider hardware delay parameters. The insights gained from the study will contribute to the development of advanced EEG-memory interface systems that can accurately and efficiently capture, process, and analyze EEG signals, opening up new avenues for understanding brain functions, diagnosing neurological disorders, and designing innovative neurotechnologies.

2 The Significance of Signal Delay

The pre-existed seizure-related data was stored in the inbuilt memory of FPGA which had a clock frequency of 100MHz. It means for every 10nS the EEG sample will be accessible for comparison with real-time data. The EEG data will be accessible for every 4.1mS. So to compensate for the timing between on-board memory data and real-time data the delay system was introduced with the Verilog model. The delay unit is designed with highly efficient time scaling in order to overcome the data loss during comparison. The loss of data for a 1nS impacts the decision to early detection of seizure identification. The EEG signals basically include very weak voltage and frequency ranges. The EEG signal is acquired at 240Hz frequency. To predict seizure occurrence in EEG signals, 4mS (1/240) continuous data is required. If data is collected every 4 milliseconds, approximately 15,000 data samples, each 10 bits in size, are required for a 60-second duration. A hardware accelerator gives better performance for this kind of application while dealing with large amounts of data.

In the proposed model delay circuit is designed to synchronize the real-time EEG data with the memory through interfacing to FPGA [5] and utilizing it as a hardware accelerator. Hardware accelerators are purpose-built designs that accompany a processor for accelerating a specific function or workload. However, they require intensive CPU operations and memory bandwidth that make general CPUs fail to achieve the desired performance levels. Field-Programmable Gate Arrays (FPGAs) are widely used for digital circuit designs due to their reconfigurable nature and parallel processing capabilities, [6].

3 Synchronizing Hardware Accelerator

EEG was once considered the most reliable method for diagnosing tumors, seizures, and other intensive brain diseases. A healthy human EEG will exhibit activity patterns that correspond to how awake a person is. In clinical and scientific research, EEG is often recorded at sampling rates ranging from 250 to 2000 Hz and the amplitudes range between 20 and 100μV, [7], [8]. The on-chip frequency of FPGA, Zynq-7000 series is 100MHz. However, the maximum range of EEG signal frequency is 250Hz. In order to synchronize the recorded data in FPGA memory to real-time EEG-acquired data the delay unit is very much important. The delay unit will step down the system frequency. The EEG signal frequency 240Hz converted to time i.e. 4mS. The AFE(Analog Front End) module in the EEG acquisition board contains an analog to digital converter [9], which converts the signal into to digital form of 10bits (minimum required) for every

4mS. The clock frequency of the FPGA board taken is of 100MHz i.e 10nS. The EEG signal is given at a frequency of 240Hz and the FPGA board frequency is 100MHz both should be synchronized for further computations. A Delay unit is attached to the FPGA clock to reduce the frequency by increasing the time. The conversion equation is given below:

$$\text{Decimal value for delay} = \frac{\text{Frequency of FPGA}}{\text{Frequency of EEG device}} \quad (1)$$

$$= \frac{100\text{MHz}}{240\text{Hz}}$$

$$= (416666.667)_{10}$$

$$\text{With 50\% duty cycle} = (208333.335)_{10} \quad (2)$$

$$= (65B9A)_{16}$$

After computation the result is in decimal form converted into 5-digit hexadecimal, it requires total 4-bits*5digits i.e 20bits. The clock signal is of 50% duty cycle. The delay is divided by 2 gives $(208333.335)_{10}$. The decimal number is given as delay in the code.

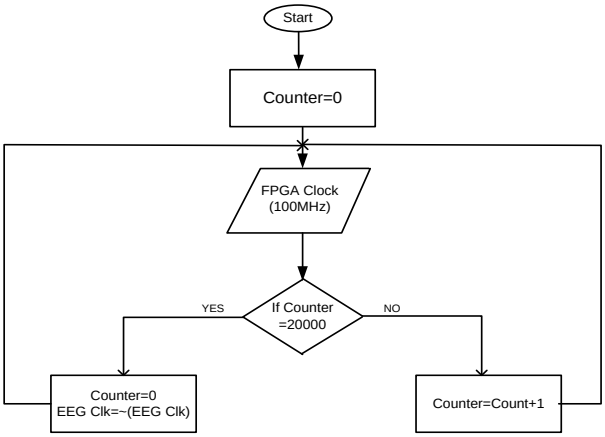

Fig. 1: Delay Unit Process Flow

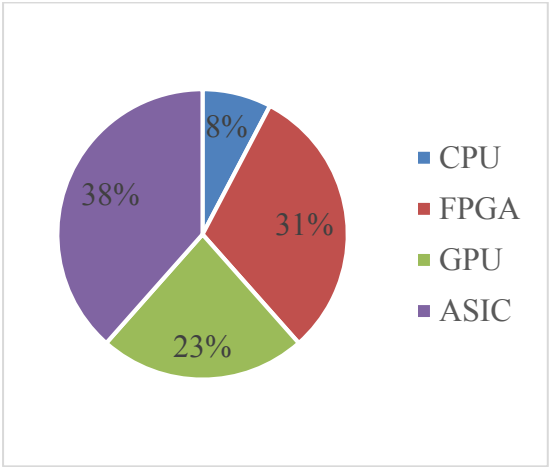

Fig. 2: Comparison of computational efficiency

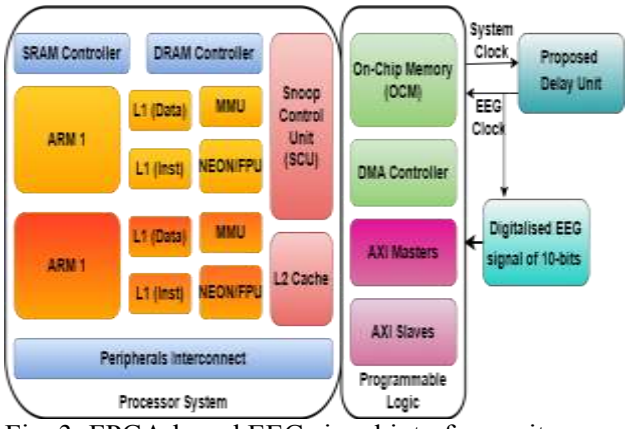

Fig. 3: FPGA-based EEG signal interface unit

The process of synchronization of the accelerator is shown in Figure 1. The Verilog model design undergoes synthesis using an appropriate synthesis tool, tailored for the target FPGA device. Once synthesis is finished, the tool generates post-synthesis reports containing resource utilization specifics. These reports are represented in Table 1, furnish comprehensive data on input and output pin counts, the number of buffers employed, and the LUT count following the synthesis procedure. The performance among various resources is shown in Figure 2, the ASIC model gives better performance because it is a full custom-based design. The optimization parameters can be defined in every stage of ASIC. However hardware complexity and programmability can be achieved better in FPGA-based, [10]. The proposed delay unit can be understood in a better way from the Figure 3.

Table 1. Utilization report for Post-Implementation: Verilog code

Parameter	Utilization	Available	% Utilization
FF	22	106400	0.02
LUT	19	53200	0.04
I/O	2	200	1.00
BUFG	1	32	3.12

4 Results

The implementation of this work is a comprehensive undertaking that involves both hardware and software development. The foundation of the system is the Zed Board, which is equipped with a reconfigurable device from the Zynq-7000 family that allows the system to be highly versatile and adaptable, [11], [12].

The selected FPGA provides hardware compatible with programming the design of the interface unit, resulting in a less complex design. If the hardware doesn't support design programming, a

new complex design should be made to make the hardware compatible with the software. This complex design can be done by adding one more layer of programming to the core software.

Figure 4 shows the output EEG clock signal produced from the FPGA operating clock signal as input. The operating FPGA clock signal consists of a high-frequency clock signal of 100MHz. The FPGA's primary timing reference generates this inbuilt clock frequency. The delay unit needed for interfacing consists of an adder, multiplexer, memory, and registers. This interface delay unit is implemented using a counter with high resolution, taking advantage of the FPGA clock's precise time period of 1nanosecond. The EEG signal delay in Milliseconds is computed for nanoseconds, which provides a very high resolution of approximately 1000 times. The counter value is adjusted based on equations 1 and 2 to achieve the desired EEG clock frequency of 240Hz at the output.

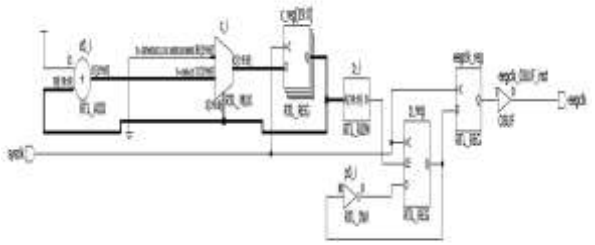

Fig. 4: Schematic of Verilog Model of Proposed Delay Unit

Fig. 5: Output Waveform at Counter Value $C=208333_{10}$

When the standard FPGA clock signal, operating at 100MHz, is input into the delay unit, the unit applies a specific time delay using a counter value of 208333_{10}, obtained from equation 2. This results in the generation of the EEG clock signal at the output with a time period of 4.16 milliseconds, as depicted in the simulation waveform shown in Figure 5.

Alternatively, by adjusting the counter value to 20000_{10}, the delay unit produces an EEG clock signal with a time period of 4 milliseconds, as illustrated in the simulation waveform shown in Figure 6. This EEG clock signal serves as a precise timing reference for synchronization purposes, enabling coordination and alignment of various processes or data in EEG signal processing applications.

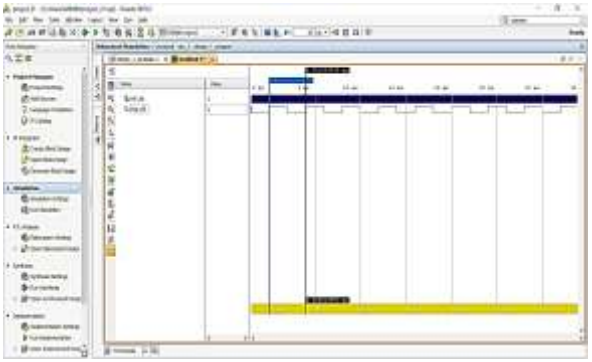

Fig. 6: Output Waveform at Counter Value $C=200000_{10}$

The total on-chip power consumption is shown in Figure 7. The power estimation report is generated using synthesized design from Xilinx Vivado by selecting 1.8V CMOS technology.

Fig. 7: Estimated On-chip Power.

The power details provided above include the total on-chip power consumption, measured at 0.134 W. The junction temperature of the device is recorded at 26.5°C. The thermal margin represents the difference between the junction temperature and the maximum permissible temperature (usually related to the thermal design limit), which is 58.45°C with a corresponding thermal headroom of 4.9 W. The following Figure 8 and Figure 9 give the information on data path delay in setup mode and hold mode respectively. The setup time is 0.420nS and the hold time is 5.713nS.

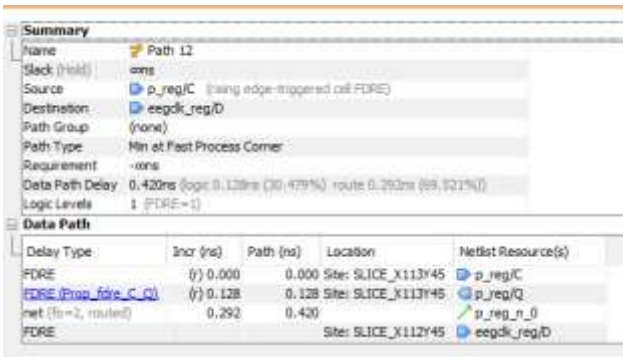

Fig. 8: Set-up time

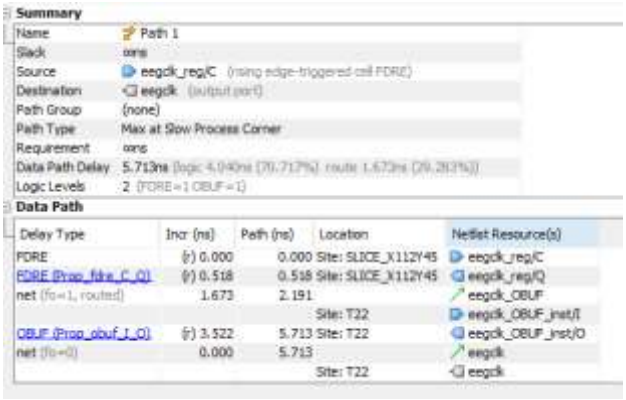

Fig. 9: Hold time

The EEG data is synchronized with FPGA system frequency by using a counter (count2) as shown in Figure 10. The initialization of the system will commence with a message “START” indicating that the seizure detection system is activated.

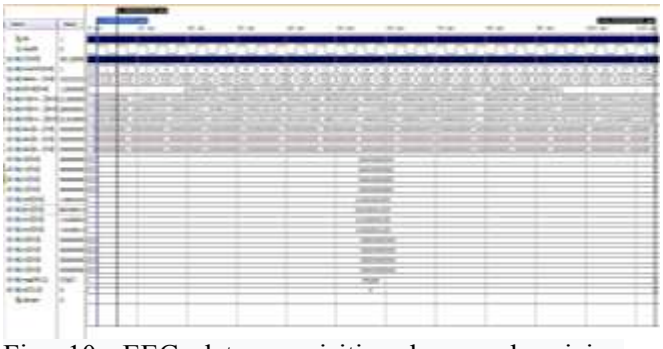

Fig. 10: EEG data acquisition by synchronizing FPGA clock frequency

5 Conclusion

In the proposed work, the delay unit is specifically designed to address the clock frequency difference between real-time EEG signals and recorded EEG data related to seizures. This is achieved by synchronizing the on-chip memory of the FPGA. The simulation results demonstrate that the FPGA clock frequency of 100MHz is successfully scaled down to 240Hz, which is crucial for accurate synchronization and analysis of EEG data. The post-synthesis results indicate a low on-chip estimated power consumption of 0.134µW, making the implementation power-efficient. Additionally, the set-up time of 0.420nS and hold time of 5.713nS ensure stable and reliable operation of the proposed delay unit.

By utilizing the proposed model of the delay unit, the generated EEG clock signal serves as a precise timing reference for synchronization purposes. This enables seamless coordination and alignment of various processes or data in EEG signal processing applications, facilitating accurate analysis and interpretation of EEG data related to seizures.

Declaration of Generative AI and AI-assisted Technologies in the Writing Process

During the preparation of this work the authors used Grammarly in order to proper sentence formation and Grammar checks. After using this tool/service, the authors reviewed and edited the content as needed and take full responsibility for the content of the publication.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

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Conflict of Interest

The authors have no conflicts of interest to declare.