Comparative Analysis of Two Op-Amp Topologies for a 40MS/s 8-bit Pipelined ADC in 0.18µm CMOS Technology

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Abstract: - The performances of two full differential operational amplifiers (Op-Amps) telescopic and folded-cascode are evaluated to satisfy the stringent requirements on the amplifier to be used in a Multiplying Digital-to-Analog Converter (MDAC) stage of a pipelined ADC (Analog-to-Digital Converter). The paper shows the solutions found to reach high gain, wide bandwidth and short settling time without degrading too much the output swing. The Op-Amp specifications are extracted according to the ADC requirements, then the two Op-Amp topologies are designed, tested and their performances are compared. Simulation results show that the Op-Amp folded-cascode topology is more suitable architecture for pipelined ADC than the telescopic one. Moreover, the use of this type of Op-Amp generates an Integral Non-Linearity (INL) error less than that of the telescopic one. The analyses and simulation results are obtained using 0.18 µm AMS (Austria Mikro System) CMOS process parameters with a power supply voltage of 1.8V. The predicted performance is verified by analysis and simulations using Cadence EDA simulator.

Key-Words: - CMOS analog circuit design; Op-Amp; Multiplying Digital-to-Analog Converter; pipelined ADC

1 Introduction

Data converters, analog-to-digital converter (ADC) and digital-to-analog converter (DAC), play a fundamental role in interfacing the digital processing core with the outer real analog world. ADCs are used in a wide range of applications, spanning from imaging to ultrasound and communication systems [1-3]. In particular, the pipelined ADC has become the most popular ADC architecture for sampling rates from a few mega samples per second (Msps) up to 100 Msps. Resolutions range from 8 bits at the faster sample rates up to 16 bits at the lower rates. These resolutions and sampling rates cover a wide range of applications, including CCD and medical imaging, digital receivers, cable modems, and fast Ethernet. The pipelined ADC architecture offers a good trade-off between conversion rate, resolution and power consumption [4-6].

Operational Amplifiers (Op-Amps) are one of the most widely used building blocks for analog and mixed-signal systems. They are employed from DC-bias applications to high speed amplifiers and filters. General purpose of Op-Amps can be used as summers, integrators, differentiators, comparators, and many other applications [7-9]. The Multiplying Digital-to-Analog Converter (MDAC) is a circuit which performs numerous of those functions. These functions include sampling the input signal (or residue voltage from a previous stage), reconstructing a voltage using a DAC, obtaining a residue (subtraction of the reconstructed voltage from the stage's sampled voltage), performing a gain to amplify the residue, and finally holding the amplified residue for the next stage [10].

Generally, there are four differential Op-Amp topologies presented in literature, i.e. two stage, telescopic, folded-cascode, and regulated-cascode. Due to the characteristics of the pipelined ADCs that are high speed, high gain, and low power consumption, telescopic and folded-cascode topologies are more suited to be a comparative study of Op-Amp topologies in this research work compared to other ones.

The goal of this work is to design and optimize an MDAC circuit for an 8 bit, 40MS/s pipelined ADC in sight of a front-end electronics of the semiconductor tracker (SCT) detector in ATLAS (A Toroidal LHC Apparatus) experiment [11]. ATLAS is a particle physics experiment at the Large Hadron Collider at CERN (the European Organization for Nuclear Research) in Switzerland. The converter is implemented with seven stages pipeline architecture, the design is based on switched

capacitor circuitry. Each stage consists of an Op-Amp and a sub-ADC.

This paper is organized as follows. Section 2 presents the ADC pipeline architecture. In section 3, the MDAC is presented and analyzed. Section 4 describes the comparative study of the two Op-Amp topologies optimized for the MDAC circuit and the obtained results. Finally, some concluding remarks are given in the last section.

2 ADC Pipeline Architecture

The pipelined ADC is constructed using switched capacitor circuits, which exploit the charge storing abilities of complementary metal oxide semiconductor (CMOS) to achieve precise signal processing and which is preferred in mixed signal and analog-to-digital converter (A/D) interfaces.

The conceptual block diagram of a generic pipelined ADC is shown in Fig. 1(a). It consists of several cascaded N stages, timing circuits, digital correction block, and a sample-and-hold (S/H) circuit at the front [12]. Each stage resolves partial code words of length q_i; i=1...n, which are all re-ordered and combined at the digital correction block to obtain the output of the converter.

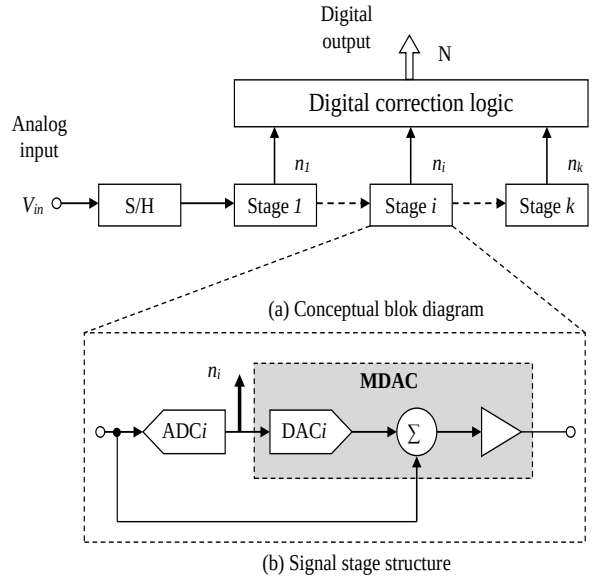

Fig. 1. Conventional bloc diagram of a pipelined ADC.

The i stage provides two outputs, the first one (q_i) is a digital coarse-resolution representation of the input while the second one (r_i) represents the residual voltage obtained by measuring the difference between the input and the voltage expected by q_i. This voltage will be measured by a gain factor (2^{qi-1}) before being sent to the next stage and the code qi will be sent to the digital error correction. The final code is tried to be improved by the subsequent stages by quantifying each time the residual voltage. All of the stages are driven from the same synchronous clock. Once the first stage has produced qi and r_i, the following stage will start to quantify r_i while the first one processes the next sample of the input.

The inner structure of a pipeline stage consists of four blocks, as illustrated in Fig. 1(b), a flash sub-ADC with output codes n_i, a sub-DAC with n_i output levels, a substractor, and a sample and hold (S/H) residue amplifier with gain G_i. The latter three blocks are implemented in practice by a single sub-circuit which is often referred to as MDAC. The blocks of the sub-ADC and the MDAC are combined together to get a single pipelined stage.

3 Multiplying Digital-to-Analog Converter

Figure 2 shows the block diagram of a generic MDAC. The MDAC circuit in the 1.5-bit/stage architecture is a switched capacitor circuit that can implement the function of sample/holder (S/H) operation, digital to analog conversion, subtraction and amplification. Normally, a switched-capacitor network is employed to accomplish all these functions. It can be implemented as shown in Figure 3. According to the charge conservation principle, the output in the hold phase is given by [13]:

$$V_{out} = \left(\frac{C_f + C_s}{C_f}\right) \times V_{in} - \left(\frac{C_s}{C_f}\right) \times V_{DAC} \qquad (1)$$

where Cs is the sampling capacitor, C_f is the feedback capacitor, and V_{DAC} is the output voltage of the sub-DAC circuit in MDAC as seen in Fig.2.

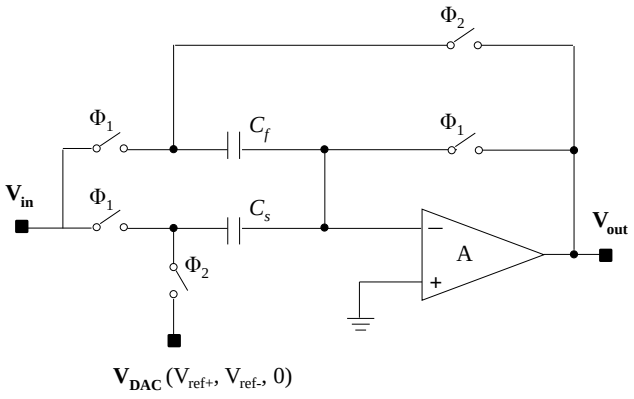

Fig. 2. Circuit implementation of the MDAC. Φ1 and Φ2 denote the sampling and the amplifying phase, respectively, according to an appropriate mechanism of switching.

3.1 Multiplying Digital-to-Analog Converter

Figure 3 presents the architecture of the 1.5-bit sub-ADC and DAC. The 1.5-bit sub-ADC consists of two comparators, the reference level of the comparators are optimally placed at Ref+ and Ref-. The 1.5-bit ADC has an encoder circuit to transfer the code from the comparator latch output to the binary code. Each sub-ADC stage gives a 2 bit most significant bit (MSB) and least significant bit (LSB) with only three useful codes 00, 01 and 10 depicting the 3-level ADC formed by two comparators. Finally, the 1.5-bit DAC converts back the digital signal of sub-ADC into an analog signal $V_{DAC.}$

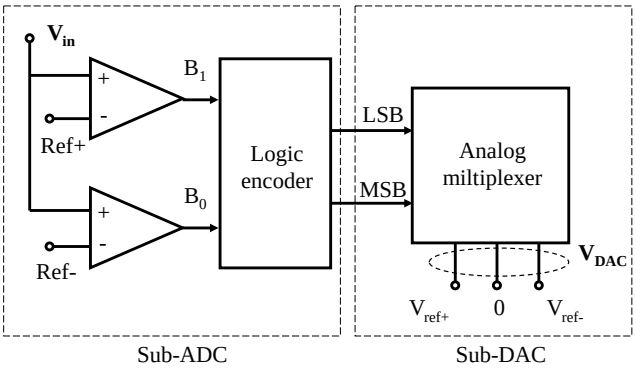

Fig. 3. Architecture of the 1.5 bit sub-ADC and DAC.

3.2 Amplifiers

Amplifiers in pipeline ADCs have a direct and major role in the operation of the individual pipeline stages [14] by performing active sampling and residue amplification. Consequently, the amplifier limitations have a direct impact on the overall ADC performance, which for high speed and very high resolutions may require the ADC to be digitally calibrated. We will discuss a comparison between two Op-Amp design topologies which are telescopic and folded-cascode and as shown in Figure5 and Figure 6, respectively.

Telescopic Op-Amps (Fig. 4) have high speed as the input device's current flows directly into output impedance, but they suffer from limited output swing. This topology is simple and there is only one current source in it, so they dissipate power less than other topologies. Its high frequency response stems from the fact that its second pole corresponding to the source nodes of the NMOS input devices is determined by the transconductance of NMOS devices as opposed to PMOS devices.

Folded-cascode Op-Amps compared to the telescopic ones dissipate more power but they have found their place in a wide range of applications due to their large output swing and their extended input common-mode. They can be implemented either employing NMOS input devices or PMOS input devices. The implementation of NMOS input transistors of folded-cascode topology with the associated Common-Mode Feedback circuit (CMFB) is shown in Fig. 5.

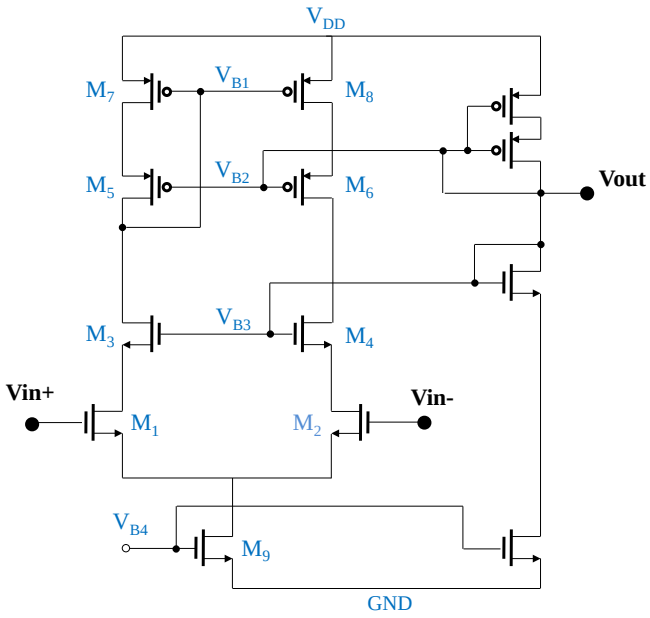

Fig. 4. Schematic design of telescopic CMOS operational amplifier.

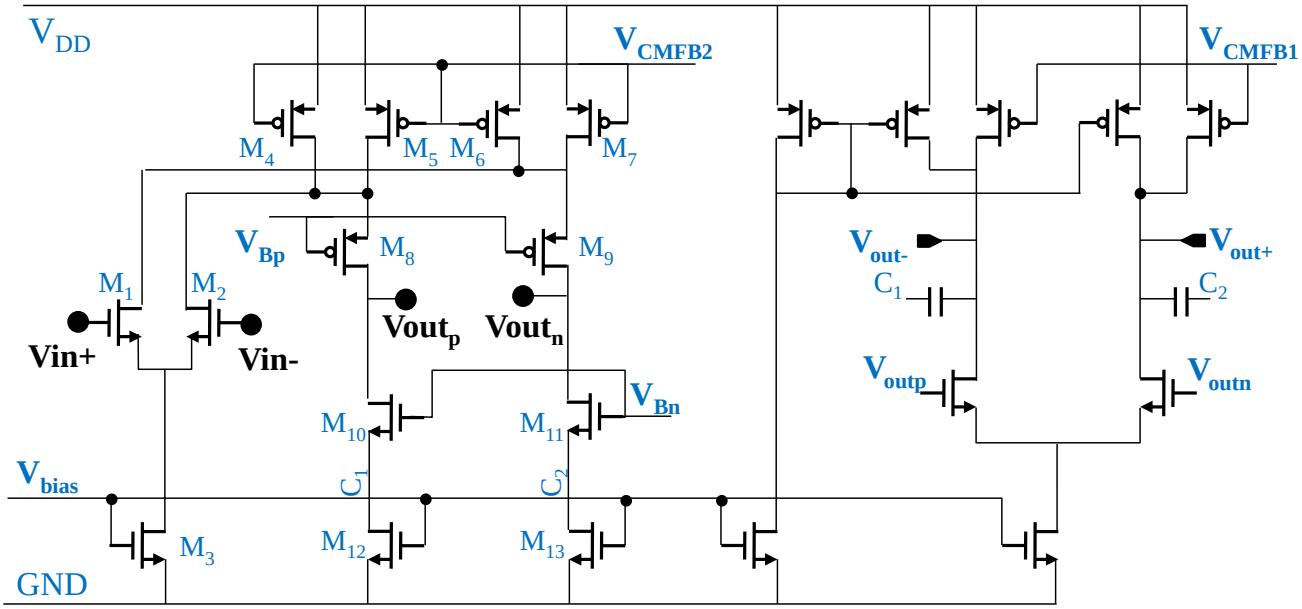

Fig. 5. Schematic design of folded-cascode CMOS operational amplifier with CMFB and NMOS input pair.

4 Simulation Results and Discussion

In this work a program based on Multi-Objective Genetic Algorithms (MOGAs) [15-17] has been developed in order to design an optimize telescopic and folded-cascode Op-Amp circuits. The Genetic Algorithm and equation based optimization are combined in order to determine the optimal dimensions (length and width) of CMOS transistors [18-19]. For that, A MOGAs-based approach is used to optimize the required performances of the Op-Amp circuit as described in Table 1. Six performances related to Op-Amp required specifications are considered in this study, direct current (DC) gain, unity-gain bandwidth (GBW), phase margin (PM), power consumption (P), circuit area (A), and slew rate (SR). Matlab optimization toolbox is used to implement the program.

By using results obtained from genetic algorithms, i.e. length and width of CMOS transistors, both Op-Amp topologies has been designed and simulated by using Cadence Virtuoso Spectre circuit simulator in standard AMS (Austria Mikro System) 0.18 µm CMOS technology. A very good agreement is observed between the program optimization and electric simulation.

The simulation results are summarized in the Table 1. Analysis shows that the folded-cascode type is more suitable architecture for pipelined ADC [20] since the design of the Op-Amp meets all the required specifications with DC gain of 71 dB, unity gain bandwidth of 335 MHz in excess of 255 MHz with 82° of phase margin compared to the telescopic type with DC gain of 56 dB, unity gain bandwidth of 210 MHz and phase margin equal to 46°.
We note that the telescopic Op-Amp outperforms the folded-cascode topology only in terms of power consumption.

Table 1. Comparison of Two Op-Amp Topologies Performances

Constraints	Op-Amp specification	Telescopic topology performance	Folded-cascode topology performance
Supply voltage (V)	1.8	1.8	1.8
DC gain (dB)	≥ 54	56	71
Unity gain bandwith (MHz)	> 80	210	335
Phase Margin (°)	≥ 45	46	82
Slew rate (V/µs)	Max	0.54	0.75
Settling time (ns)	Min	7	5.5
Power consumption (mW)	Min	9	11

To check the effectively of the devices designed, it is important to simulate if they work properly inside the environment it was made for. The test bench realizes the complete MDAC as it will be printed on the silicon; the input of the system is fed by a ramp.

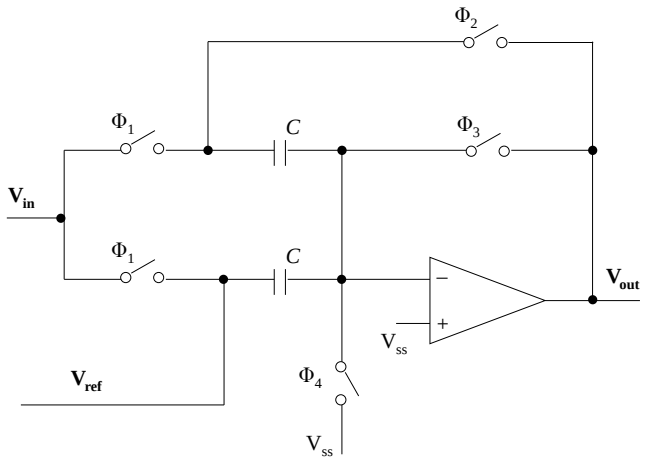

Fig. 6. MDAC test bench.

The main function of the sub-DAC is to output an analog voltage based on the comparators decisions. The residue plot in Fig. 7 is the transfer function which is created by the switched capacitor circuit (MDAC). Figure 8 represents the binary response of the 1.5 bit stage in the different three level of the reference signal. The transfer function of an ideal ADC can be represented by a best fit line as shown in Fig. 9, typically either an endpoint fit or a least squares fit.

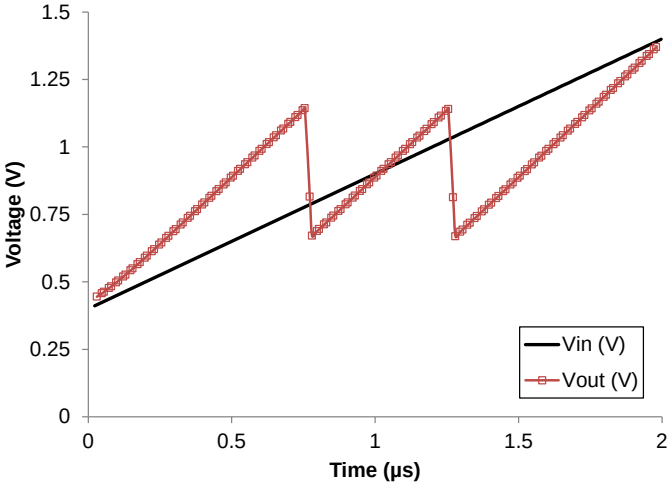

Fig. 7. Transfer function of the MDAC.

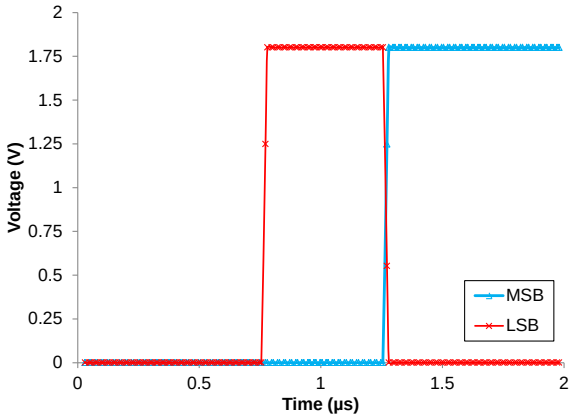

Fig. 8. Binary response of the MDAC for a ramp signal input.

An ADC that exhibits integral non-linearity (INL) will have a transfer function that is not a perfect line. The maximum difference between the actual and the ideal transfer characteristic is the INL. Each Op-Amp is placed in the test bench illustrated in Fig. 6 to be simulated and its INL is calculated. Figure 9 shows the output signal of the 1.5 stage and its best fit line using both Op-Amps. Figure 10 the INL of the MDAC for the telescopic and folded-cascode architectures of the Op-Amps, respectively.

We note that the use of the folded-cascode architecture generates an INL error less than 0.5 LSB while the telescopic architecture generates an INL error more than 1.3 LSB. So, the folded-cascode architecture generates an INL error less than that of the telescopic one.

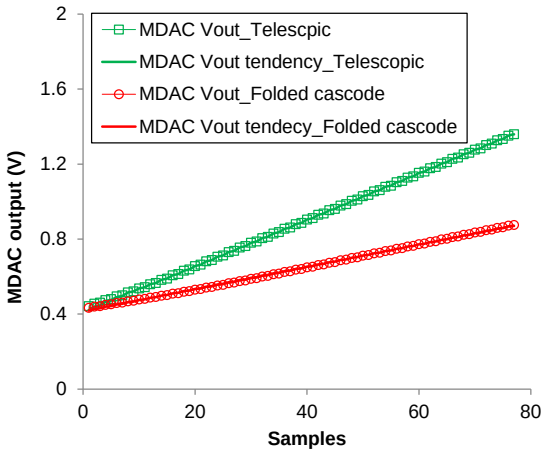

Fig. 9. Comparison of the transfer functions of MDAC and their best fitted line using two different Op-Amp topologies.

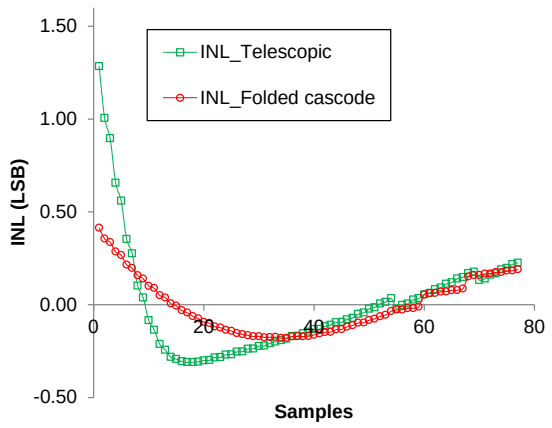

Fig. 10. Integral nonlinearity of MDAC using two different Op-Amp topologies.

4 Conclusion

This paper describes a comparative analysis of two CMOS Op-Amp topologies for an 8-bit, 40 MS/s, pipeline ADC with high gain-bandwidth and high linearity. The two considered Op-Amp topologies are folded-cascode and telescopic, they are analyzed and implemented via 0.18µm AMS process technology. The Op-Amps are placed in the MDAC which is also designed in transistor level for a 8-bit pipelined ADC.

From the simulation results, analysis shows that the folded-cascode type is more suitable architecture for pipelined ADC since the design of Op-Amp meets all the required specifications with DC gain 71 dB which is greater than 54 dB while unity gain bandwidth is 335 MHz in excess of 255 MHz with 82° of phase margin compared to the telescopic type with DC gain 56 dB, unity gain bandwidth is 210 MHz and phase margin equal to 46°.We note that the use of the folded-cascode architecture generates an INL (less than 0.5 LSB) error less than that of the telescopic architecture (more than 1.3 LSB).

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