A Proposed Advanced Controller Applied to a Single-phase Power Factor Correction Converter in Electric Vehicle Chargers

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Abstract: - This work proposes a novel approach for managing the output DC link voltage of a single-phase power factor correction (PFC) converter for electric vehicle (EV) charging without using a DC voltage sensor. The inputs and outputs of conventional boost PFC converters normally use several expensive sensors such as input voltage, input current, and output voltage. These sensors are employed to maintain system stability and control the quality of the power. A DC voltage sensorless control utilizing an estimator is used to lower the cost and hardware complexity of the power converter. The output DC link voltage is predicted using the available input voltage and current signals. For a high power factor, the controller follows the reference sine wave signal. Additionally, the converter exhibits extremely steady performance under transient fluctuations in load for a typical 1kW PFC converter. A novel Simplified Optimum Intelligent PID (SOI-PID) controller is designed for a 2.4kW, 400V output voltage, and 6A rated load, based on the second order transfer function of the system, both designs are analyzed, simulated, and compared for the same circuit parameters and loading conditions. The novel SOI-PID controller has shown advantageous performance in both transient and steady-state periods including lower rise and settling times, lower maximum overshoot, fast response to load variation, and lower stress on switching element which leads to better efficiency and lower fixed cost of the overall system.

Key-Words: - Simplified optimum intelligent PID, Sensor less control, PFC converter, DC link voltage, Electric vehicle, Adaptive Controller, process model PID.

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1 Introduction

As a result of the proper use of electronic power converters which results in fewer size, weight, and space restrictions and higher efficiency, the entire world has now shifted toward environmentally friendly electric vehicles (EVs) in the automotive industry, [1]. The EV batteries receive energy recovery via either on-board or off-board chargers. While EVs frequently use on-board chargers powered by a single-phase power supply that is typically accessible in most households, off-board chargers are frequently costly, heavy, and maintenance-intensive, [2]. The charger has a two-stage power supply that converts AC to DC in order to fulfill automotive regulations, [3]. A power factor correction (PFC) converter is used in the first stage, and an isolated DC-DC converter is used in the second stage. Single-phase PFC converters have been proposed in a variety of ways to enhance power quality and lessen harmonic content brought on by the usage of non-linear loads. A PFC with a boost converter arrangement is one of these sorts. It is widely utilized as a result of its straightforward design and straightforward input current controller, [4]. The overall layout of a two-loop control system for managing input current only and DC output voltage is depicted in Figure 1, which is present on all PFC converters with the three necessary sensors measuring the input voltage and current, as well as the DC output voltage. By utilizing operational amplifier-based converter circuits and high-accuracy resistive voltage dividers, the researchers tried to apply a variety of designs to lower the cost of the sensors. However, due to low noise immunity in these circuits, imbalanced operation results which causes the converter to operate in an unstable manner

as a result of several difficulties such as signal delays and other practical problems, [5]. High-bandwidth sensors have been employed in PFC converter operations to lessen these issues. Although these sensors have a fairly high operating cost, over time they may reduce dependability and cause the converter to operate with poor dynamics, [6].

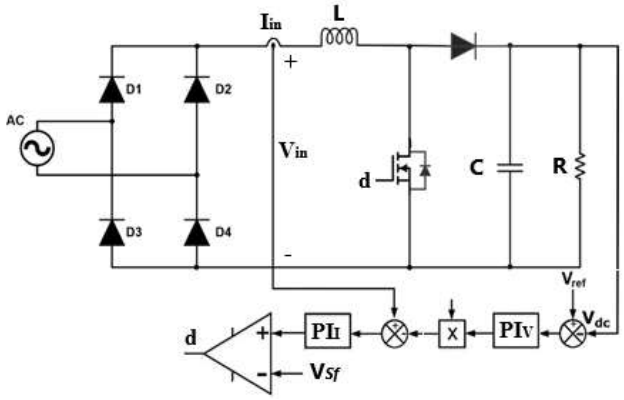

Fig. 1: Conventional boost PFC with a two-loop control system

Researchers have investigated many forms of sensor-less control strategies in PFC converters to increase their reliability and simplify control structures, hence lowering the cost of the entire system, [7]. The functioning of converters now requires the use of sensorless control techniques for input voltage, input current, and output voltage. The function of the sensor to be deleted must be determined by preparatory research before choosing one of these options. Because it directly contributes to the formation of the current reference signal, an exact mathematical representation must be created using the dependent variables indicated above in order to achieve the function that the deleted sensor was performing, [8], [9]. Additionally, it is feasible to estimate the DC link voltage by carrying out the necessary calculations on a microcontroller, DSP, or FPGA platform with digital signals and high efficiency with a PFC converter at extremely high frequency. In a number of distinct scholarly works, [10], [11], a detailed description of the various sensorless control methods that may be applied in single-phase PFC converters is provided.

With the use of input voltage and current data, stage 1 of this article (Design A) suggests a straightforward DC voltage sensor estimator, and stage 2 (Design B) proposes an SOI PID controller and the performances of both techniques are analyzed, and compared. To lessen the ripple content, a low-pass filter is employed, with a cutoff frequency that is twice the line frequency. Wide changes in load resistance can also be maintained by the developed controller.

The rest of this article is organized as follows, section 2 discusses the analysis and simulation of a digital estimator of the DC output voltage depending on the input voltage and input current. In section 3, the proposed SOI PID controller is analyzed, simulated and compared with the digital estimator controller. Section 4 gives the main contributions of the new controller with a discussion of the results and conclusions.

2 Analysis of a PFC Converter Controller

The analysis of the dynamic and transient response of the converter with the new proposed controller will be carried out in 2 stages as follows:

Stage 1: Analysis and simulation of design A of the converter with a digital controller which uses the input voltage and input current to estimate the DC output voltage. This piece of work is not novel but is carried out for comparison with the new controller at the same operating conditions.

Stage 2: Analysis and simulation of design B of the new proposed SOI PID controller at the same operating conditions as stage 1 and comparing the dynamic and transient responses of the two controllers with load variation.

2.1 Stage 1: Sensorless Digital Estimator (Design A)

In a PFC converter, several researchers have investigated the implementation of a controller without sensing the input current using a precise estimator, [12]. The current controller is the inner connection in the control structure. Therefore, the bandwidth required for the sensor must be large. It is difficult to use a large bandwidth estimator to accurately estimate the input inductor current because it has a low-frequency component, [13]. Consequently, the estimator may not be accurate or observable at all operating points, and sensor delays can compromise the stability and robustness of the control system, [14]. Therefore, eliminating the input current sensor is not a practical solution. Since the input voltage and current are dynamically linked, the

input voltage sensor is also irreplaceable, [15]. Thus, the DC output voltage sensor is the most cost-effective solution to eliminate among all these sensorless operations. Also, the DC output voltage estimator can improve the transient performance of the control technique by using two-loop cascade controllers for applications over 500W. The output DC linked voltage is regulated by the outer loop while maintaining a high power-quality input current is by the inner loop. Figure 2 shows the structure of a two-loop PFC converter controller. It uses input voltage and current sensors to sense the required parameters that are used for comparison and controller. A PI controller is appropriate because it has less influence on the converter due to abrupt changes in load and specific harmonic eliminations or reductions of the input current. To test the PI controller, the initial step creation using small signal analysis of the PFC converter is distinguished to analyze both off-state and on-state disorders. The final transfer functions of the system are $G_1(s)$ for input current and $G_2(s)$ for DC output voltage.

$$G_1(s) = \frac{I_L(s)}{d(s)} = \frac{V_{dc}}{L} \times \frac{s + 2(1-d)I_L/(C \times V_{dc})}{s^2 + \frac{1}{R \times C}s + (1-d)^2/(L \times C)} \quad (1)$$

$$G_2(s) = \frac{V_{dc}(s)}{d(s)} = \frac{I_L}{C} \times \frac{s - (1-d)V_{dc}/(L \times I_L)}{s^2 + \frac{1}{R \times C}s + (1-d)^2/(L \times C)} \quad (2)$$

where, V_{dc} is DC output voltage, I_L is inductor current, L is inductor, C is output capacitance, d is duty ratio, and R is load resistance.

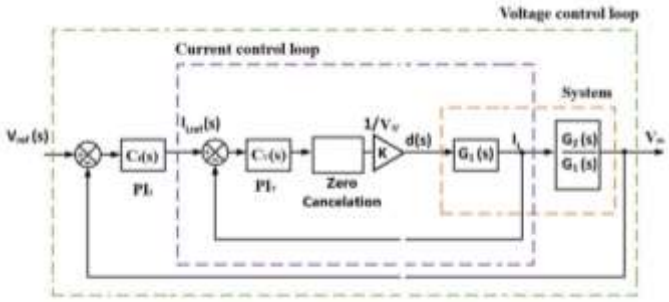

Fig. 2: Two loop control of a PFC converter

2.1.1 Initial Analysis Assumptions of the PFC Converters

The initial analysis of the PFC converters is based on a set of assumptions such as the input voltage is purely sinusoidal ($v_{ac} = V_m \sin \omega t$), the passive elements are ideal, the input inductor should be selected to the PFC converter always operates in the continuous mode, and the output capacitance should be large enough and connected across the load to reduce the contents of second-order harmonic ripple and then the total harmonic distortion (THD).

For continuous mode operation of a PFC converter:

$$v_{ac} = V_{dc} \times (1 - d) \quad (3)$$

when the switch, i.e. IGBT device, is turned-off, the output current is:

$$I_{in} = i_{in} \times (1 - d) = C\frac{dV_{dc}}{dt} + \frac{V_{dc}}{R} \quad (4)$$

Ideally, the input and output powers should be equal in any converter. Thus, we have:

$$v_{ac} \times i_{in} = V_{dc} \times I_{dc} \quad (5)$$

where, i_{in} is AC input current and I_{dc} is DC load current.

The input power is:

$$P_{in}(t) = v_{ac} \times i_{in} = V_m \sin \omega t \times I_m \sin \omega t = \frac{V_m \times I_m}{2}[1 - \cos(2\omega t)] = P_{rms}[1 - \cos(2\omega t)] \quad (6)$$

where, $P_{rms} = \frac{V_m \times I_m}{2}$ is the average input power.

If the input and output powers are equal, the DC output voltage sensed by the sensor has an average and ripple component at double the line frequency. The outer loop is the voltage control with slower dynamics while the inner loop is a fast-acting current. Choosing DC voltage sensor less control is easier to implement and thus reduces system cost. Also, the effect of the load resistance on the output DC voltage should not be reflected when estimating the output voltage, otherwise a change in the dynamics of the system will occur. In this work, Vdc is used as the expected output voltage reference, and the converter has the ideal characteristics. The output voltage as a function in the load is:

$\frac{V_{dc}^2}{R} = P_{in}(t)$, $\frac{2V_{dc}}{R}\Delta V_{dc} = \Delta P_{in}$, so that $R = 2 \times \frac{\Delta V_{dc}}{\Delta P_{in}} V_{dc}$

where, V_{dc} is the actual output voltage observed from the proposed estimator, ΔV_{dc} is the small change in the DC output voltage reference, and ΔP_{in} is the small change in the input power.

Also, $\Delta P_{in} = v_{ac}\Delta i_{in} + i_{in}\Delta v_{ac}$ (7)

In discrete time analysis and from Equations (3) & (4), we have:

$v_{ac} = V_{dc}^{*} \times (1-d)$; where, V_{dc}^{*} is the desired discrete output voltage reference.

$$i_{in} \times (1-d) = C\frac{dV_{dc}}{t_s} + \frac{V_{dc}}{R}$$

where, t_s is the sampling time period of the switching frequency device for PFC converter.

$$\text{Then, } \frac{v_{ac} \times i_{in}}{V_{dc}^{*}} = C\frac{dV_{dc}}{t_s} + \frac{V_{dc}}{R} \quad (8)$$

The final expression of ΔV_{dc}(DC output voltage estimated) is derived from Equations (7) & (8)

$$\Delta V_{dc} = \frac{P_{in} \times t_s}{C \times V_{dc}^{*}} + \frac{1}{C}\sqrt{\left(\frac{P_{in} \times t_s}{C \times V_{dc}^{*}}\right)^2 - 2Ct_s\Delta P_{in}} \quad (9)$$

The first term in (9) is the DC output voltage with constant parameters. The value of C has an inverse effect on the ripple in the DC output voltage. The ripple of DC output voltage is reduced when the size of capacitor is increased which leads to a higher cost of the system. Economically, a lower value of C which limits of THD to 5% is used to minimize the cost of the system for a specific power level. The output $V_{dc}$of the converter is obtained when the ΔV_{dc} inputs to a low pass filter (LPF) which acts as an integrator. This technique removes the effect of load and assessment block by Equation (9) to give ΔV_{dc}. The output signal result has a very small ripple when compared to the sensor control of the PFC converter.

2.1.2 Simulation results of design A

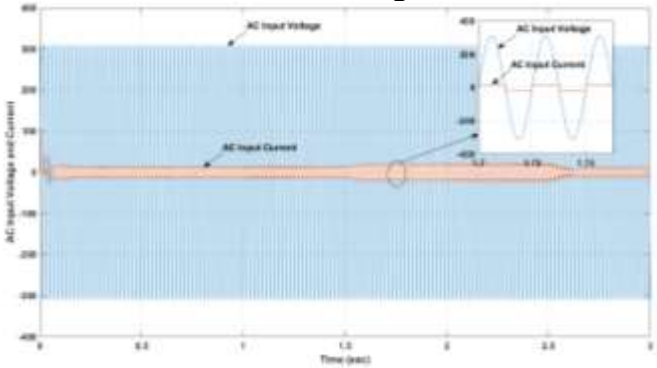

Fig. 3: AC input voltage and input current at transient period and steady state (design A)

Figure 3 shows the envelope of the AC input current during the transient period. The current has a maximum positive spike of 107A, a settling time of 70msec, and a maximum negative spike is -30A.

The zoomed area on Figure 3 shows the steady state waveforms of the AC input voltage and current with RMS values of 220V for input voltage and 20.625A input current at rated load.

Figure 4 indicates how the DC output voltage tracks the changes in the DC input voltage and currents due to the fact that, this method uses the value of input voltage and input current signals to estimate the output DC link voltage. The peak overshoot of the DC output voltage is 420V at startup with rated load and increases to 468.7V at light loading conditions.

In Figure 5, the voltage and current stresses on the switching element (IGBT) in transient and steady-state are shown. It can be seen that during the transient period the peak overshoot voltage across the IGBT is 421.5V at rated load, and increases to 468.5V at light load, while the transient peak current spike is 13A at rated load and increases to 17.25A at heavy load.

The zoomed areas of Figure 5 show the steady state voltage and current stresses of the IGBT at the heaviest load condition.

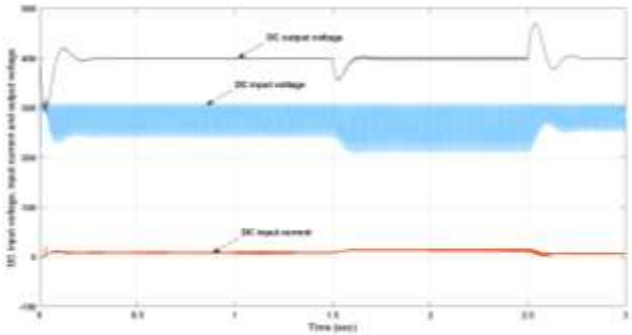

Fig. 4: Output voltage vs DC input voltage and current (design A).

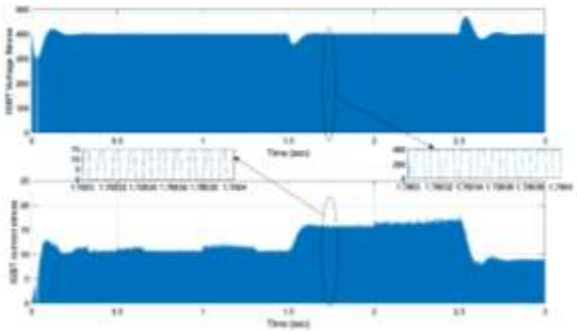

Fig. 5: Voltage and current stresses on the switching element in design A at transient period and steady state

The parameters of the converter together with the controller response at transient, steady state, and load variation instants are summarized for design A in Table 1 (Appendix).

In the next section, the digital output voltage estimator is replaced with the proposed simplified optimum controller, and the preceding analysis will be repeated and compared for the same circuit parameters and loading conditions.

3 Stage 2: Proposed Simplified Optimum Intelligent (SOI-PID) Controller (Design B)

3.1 Analysis and Design

The simple optimum SO-PID design formula proposed is based on the process transfer function to determine the optimum PID controller coefficient. Figure 6 illustrates a general 2nd order system with a controller deduced based on the optimum response depending on the process transfer function as the following equations, [16], [17]. Applying the general concept of Multi Degree Of Freedom (MDOF) controller can be applied to the proposed controller to make it a self-adaptive (Intelligent). This concept depends on using two controllers a fast controller (with a significant overshoot) as a wide-range controller and a slow controller (with no overshoot) as a fine-tuning controller. The two controllers derived from Simplified Optimum PID Controller with different gains, one of them is a high gain for the fast controller while the other gain is low for the slow controller. This previous procedure results in a Simplified Optimum Intelligent PID (SOI- PID) Controller.

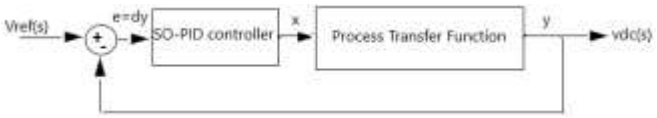

Fig. 6: Closed-loop of 2nd order process

Assuming the process transfer function is a common 2nd order process

$$\frac{y}{x} = \frac{k}{as^2+bs+c} \tag{10}$$

$$y(as^2 + bs + c) = kx \tag{11}$$

Substituting $s = \frac{dy}{dt}$ results the following differential equation:

$$a\frac{d^2y}{dt^2} + b\frac{dy}{dt} + cy = kx \tag{12}$$

In the above differential equation, substituting $\frac{dy}{dt} = \frac{\Delta y}{T}$:

$$a\frac{dy}{dt}\left(\frac{\Delta y}{T}\right) + b\frac{\Delta y}{T} + c\int \Delta y\, dt = kx \tag{13}$$

In the above differential equation, substituting $e = \Delta y$:

$$a\frac{dy}{dt}\left(\frac{e}{T}\right) + b\frac{e}{T} + c\int e\, dt = kx \tag{14}$$

Rearrange the above equation to match the PID controller equation.

$$x = \frac{b}{kT}e + \frac{c}{k}\int e\, dt + \frac{a}{kT}\frac{dy}{dt}(e) \tag{15}$$

Equaling coefficients of equation (15) with its corresponding next equation (16).

$$x = K_p e + K_i \int e\, dt + K_d \frac{dy}{dt}(e) \tag{16}$$

Results in the controller constant:

$$K_p = \frac{b}{kT}, K_i = \frac{c}{k}, K_d = \frac{a}{kT} \tag{17}$$

where T is chosen as a control program sampling time or multiple of the control program sampling time.

To apply SO-PID controller for a process of second order system presented by Equation 17

$$\frac{y}{x} = \frac{s+k}{as^2+bs+c} \tag{18}$$

The controller constants are designed for the transfer function:

$$\frac{y}{x} = \frac{1}{as^2+bs+c} \tag{19}$$

and add a pole to cancel the zero:

$$s + k = 0 \tag{20}$$

The controller detailed design of the PFC converter is made with MATLAB/SIMULINK software. By using a large signal mode, the plant transfer function is estimated with all of the necessary conditions.

3.2 Simulation Results of Design B

Figure 7 shows the AC side input voltage and input current at the transient period and steady state. The

effect of the new controller canceled the current overshoot at the transient period and reduced its settling time to 12.5msec compared to 70msec settling time of design A which means that the new controller of design B is 5.6 times faster than design A.

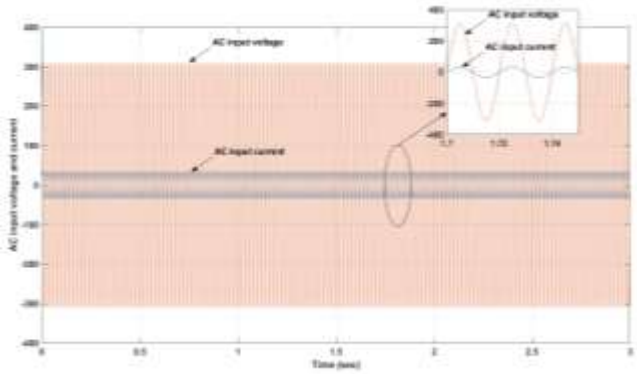

Fig. 7: AC input voltage and input current at transient period and steady state (design B)

The fast response and minimum overshoots of the proposed controller contribute to both input side and output side signals which can be obviously noted from Figure 8, which shows the comparison of the responses of the digital estimator controller and the simplified optimal controller at transient periods of the AC input current, and Figure 11, which compares the responses of both controllers during transient periods of the DC output voltage.

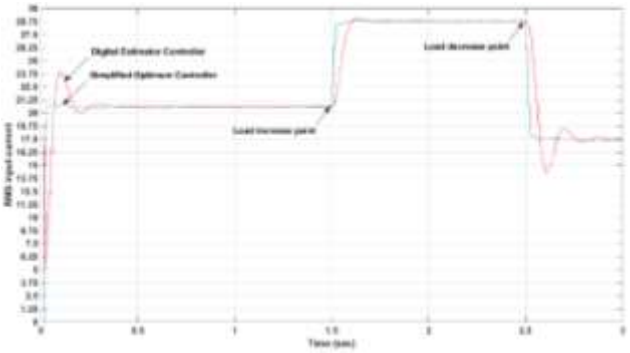

Fig. 8: RMS AC input current

In Figure 9, the DC output voltage is plotted against the DC side input voltage and current. It is obvious that the output voltage has a peak overshoot of 416.9V (4.23%) with no transient current spikes or voltage peaks in the DC input sides. The output voltage in this case is not affected by the change of input voltage and current which is a major advantage of the proposed technique.

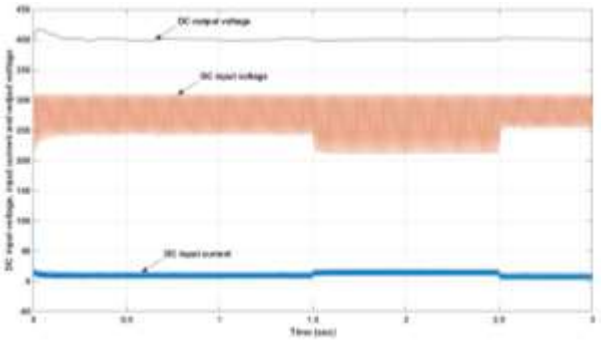

Fig. 9: Output voltage vs DC input voltage and input current (design B)

The settling time of the output response in the second case (design B) is 12msec compared with 76msec in the digital estimator case (design A).
Figure 10 shows the voltage and current stresses on the switching element of design B during transient period and steady state. The simulation results show a steady and stable voltage stress on the switching element even at load change instants, which is another advantage of the new controller that leads to a reduction of switching and conduction losses of the converter. The maximum positive voltage stress during the transient period is 419V and no negative stress exists. The transient peak current spike through the switch is 12A compared with 13A in design A. This improves the efficiency of the converter due to the reduction of switching losses and the power rating of the switching element which minimizes the cost of the hardware.

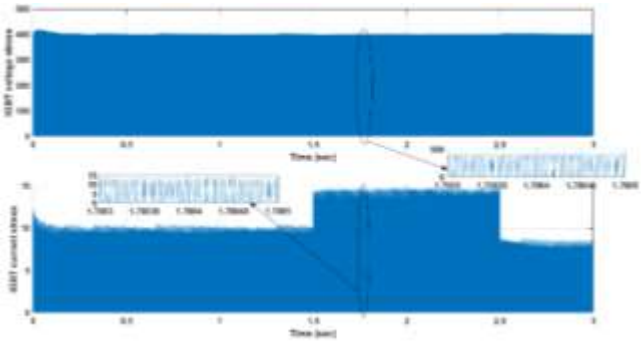

Fig. 10: Voltage and current stresses on switching element in design B at transient period and steady state

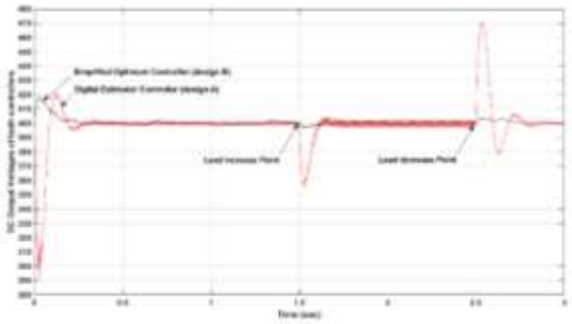

Fig. 11: Comparison of DC output voltage response for digital estimator and SOI PID controllers

The converter parameters and controller response at transient, steady state and load variation instants for design B are shown in Table 2 (Appendix).

The output responses of the DC output voltage for the two controllers (digital estimator and SOI PID controller) are shown in Figure 11. The comparison shows clearly several advantages of the proposed SOI PID controller which are; lower peak overshoot, lower rise time, and settling time, faster response to load variation with negligible overshoots and hence lower stress on the semiconductor switching element, and finally, lower voltage ripples on the output DC link.

The output voltage ripple is compared in Figure 12 for the two control techniques, this output ripple percentage can be calculated from Equation (21) as:

$$\Delta V_o\% = \frac{Higher\ Peak - Lower\ Peak}{Nominal\ Voltage} \times 100 \qquad (21)$$

From Figure 12, it can be found that the higher and lower peak voltages for the digital estimator controller (design A) are 402.2V and 396.7V respectively, which means a percentage output ripple voltage of 1.375%.

For the SOI PID controller (design B), the higher and lower peak voltages are 400.7V and 399.1V respectively, which means a percentage output ripple voltage of 0.4%. This final statement adds another advantage to the performance of the proposed controller over the conventional digital estimator controller. It has to be noted that this ripple content is calculated at the period of the heaviest load condition.

A final comprehensive comparison between the proposed SOI PID controller and the digital estimator controller as a counterpart is held in Table 3 (Appendix).

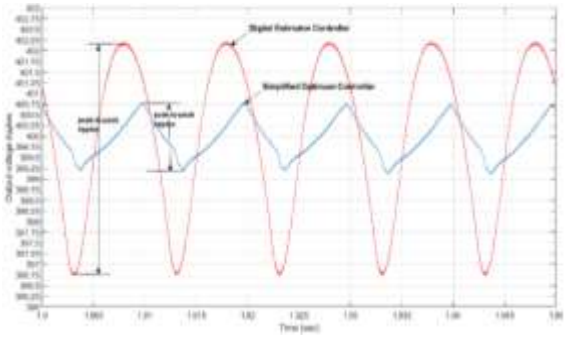

Fig. 12: DC Output voltage peak-to-peak ripples

4 Conclusions

Two different control techniques were designed, analyzed, and simulated. The first technique is a digital estimator to predict the output DC link voltage from the available input voltage and input current, which is widely discussed in the literature [18], [19], [20], [21], [22], while the second suggested technique uses the second-order transfer function of the converter (process model) to design the PID coefficients. The suggested Simplified Optimized (SOI-PID) controller has been proven to give lower rise time, lower peak overshoot, and lower settling time of the system response (output voltage and output current) besides the lower voltage and current stresses on the power electronic switching element at a wide range of load variation. These advantages improve the overall efficiency of the converter and reduce its capital cost.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- Mohamed I. Abu El-Sebah contributed by the new controller analysis and design and revising the final version.
- Abouelmaaty M. Aly contributed by modelling and simulation of design A, collecting resources, editing the draft version and revising the final version.
- E. S. Elwakil contributed by modeling and - simulation of design B, commenting on simulation results, setting comparison tables and revising the final version.
- Fathy A. Syam contributed by collecting resources, modeling and simulation, editing and revising the final version.

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APPENDIX

Table 1. Transient and state steady-state parameters of AC and DC input signals of Design A

Parameter / Signal	Steady-state value	Max Spike	Settling time	Response time to load variation
AC input voltage	220V (RMS)	none	N/A	N/A
AC input current	20.625A (RMS)	107A	70msec	15msec
DC input voltage	277V (average)	309.4V	20msec	100msec
DC input current	10.5A (average)	25.25A	72msec	83msec
DC output voltage	400V (average)	420V	76msec	74msec
IGBT voltage	400V (average)	421.5V	137.9msec	74msec
IGBT current	5A (average)	13A	140msec	80msec

Table 2. Transient and steady-state parameters of AC and DC input signals of Design B

Parameter / Signal	Steady-state value	Max Spike	Settling time	Response time to load variation		
AC input voltage	220V (RMS)	none	N/A	N/A		
AC input current	20.625A (RMS)	77.5A	31.5msec	32msec		
DC input voltage	277V (average)	347V	12.5msec	12msec		
DC input current	12.5A (average)	109A	12msec	12msec		
DC output voltage	400V (average)	416.9V	12msec	12msec		
IGBT voltage	400V (average)	418V	32msec	34msec		
IGBT current			5A (average)	12A	32msec	20msec

Table 3. Quantitative Comparison between the proposed controller and other techniques

Control Technique	Efficiency	Power Factor	Regulation	THD	Complexity	Response Time
Proposed SOI-PID	96-97%	0.99	0.4%	1.1 – 2.4 %	Very Low	Very Fast
Average Current Mode	95-97%	>0.99	3-8%	5-10 %	Moderate to High	Moderate
Peak Current Mode	94-96%	0.95-0.98	4-10%	5-15 %	Moderate	Fast
Hysteresis Control	94-96%	>0.99	0.5-2%	5-10 %	Low to Moderate	Very Fast
Sliding Mode	95-97%	>0.99	1-3%	<5 %	High	Fast
Digital PID Control	95-97%	>0.99	1-5%	<5 %	High	Fast to Moderate