An Improved Conventional Diode-Clamped Multilevel Inverter Using Non-Zero Triangular- Based Unipolar Modulation Scheme

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Abstract: - This paper presents an improved conventional diode-clamped multilevel inverter using non-zero triangular-based unipolar modulation scheme. The proposed scheme is meant to reduce the number of carrier waves, minimize the circuits of modulation scheme and obtain stabilized output voltage waveforms. Non-zero triangular-based unipolar modulation scheme is actualized by using two zero-free triangular wave carriers and two modulating sinewaves for line-to- line five level output voltage waveforms in single phase full bridge diode-clamped multilevel inverter unlike conventional multicarrier sinusoidal pulse width modulation that uses four triangular waves and one modulating sinewave for the same inverter type. The proposed system also used microcontroller in the combinational of its wave signals in order to generate the appropriate triggering signals for switching the power semiconductor switches. The proposed system has the following features: (i) It produces two distinct triggering trains (W1 and W2) meant to reduce the low and high harmonics unlike conventional modulation techniques (ii) All its carrier waves operate in continuous current mode which makes it unique from other multicarrier and other related modulation schemes (iii) it has low component counts. The proposed scheme on the conventional diode-clamped inverter produced the following results: voltage and current with total harmonic distortions of 0.4547%, stabilized 400V output voltage and 20A output current, probability results at each level of voltage and current occurrences are 0.10, 0.25, 0.25, 0.75 and 0.90; power output of 80kW, low component counts of modulation circuit scheme and experimental prototype.

Key-Words: - Improved, modulation, non-zero triangular, unipolar

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1 Introduction

Multilevel DC-to-AC converter is an inverter with different levels of output voltages which share the input supply voltage/s depending on the stability of the system and the kind of circuit configurations. Under stabilized operating conditions, the output voltages of the multilevel inverter (MLI) share the input voltage equally and vice versa. A lot of researches have been ongoing on multilevel inverter due to its attractive features of high power eminence, great voltage handling capability, little switching power losses and reduced EMI

Multilevel inverters have various types ranging from the conventional topologies such as diode-clamped multilevel inverter, flying capacitor multilevel inverter and cascaded multilevel inverter [1]-[11] to different improved topological circuits like Hybrid MLI, modular multilevel inverters, optimized cascaded multilevel inverter etc.) [12]-[18]. The three conventional multilevel inverters have intrinsic imbalance voltage levels which is observable in the waveforms of the input capacitors and the loads beyond 0.1second [already seen in 2] without adding any extra circuitries for removing the imbalances. The concept of additional circuits on the conventional types is to compensate those voltage drops so as to improve the quality of the output waveforms as can be seen in [19]. Multilevel inverters (MLIs) have many applications such as in high power applications, medium power applications, industrial machine drive, tractions, renewable based power generation, etc [20] - [21].

A lot of modulation schemes on multilevel inverters have been done by many researchers in the past and published online with diverse merits and demerits. Some of those schemes are: in-phase disposition pulse width modulation (IPDPWM), phase

opposition disposition PWM (PODPWM), alternate phase disposition PWM(APDPWM), phase shift PWM, space vector modulation scheme, modified space vector modulation techniques, optimized selective harmonic elimination scheme, etc [22]-[24].

In this research work, a 5 level line-to-line output voltage based diode-clamped multilevel inverter is simulated and implemented using non-zero triangular-based unipolar modulation scheme (NZTBUMS). NZTBUMS is a modified class of multicarrier PWM scheme. It is different from multicarrier PWM scheme in the sense that (i) the carrier waveforms are not touching zero axis therefore operating in continuous current mode, (ii) it has reduced number of carrier waveforms, (iii) it has reduced total harmonic distortions (iv) It has lower signal component counts (v) It produces two distinct trains of firing signals unlike conventional multicarrier modulation techniques.

2 Methodology

The materials that are used in this research are the insulated gate bipolar transistors, IGBTs, clamping diodes, resistor load and inductive load, capacitors, connecting wires and DC source for power circuit. These materials are used to build the power circuit topology as shown in Fig.1. MatLab modelling and implementation methods are adopted in this research. Fig.1 consists of single source, Vs, two input capacitors, four clamping diodes, eight IGBTs, thirteen defined nodes with thirty two branches (b_{11}….b_{32}) and load point. In furtherance to that, it has two legs that are phase shifted at 180 degrees.

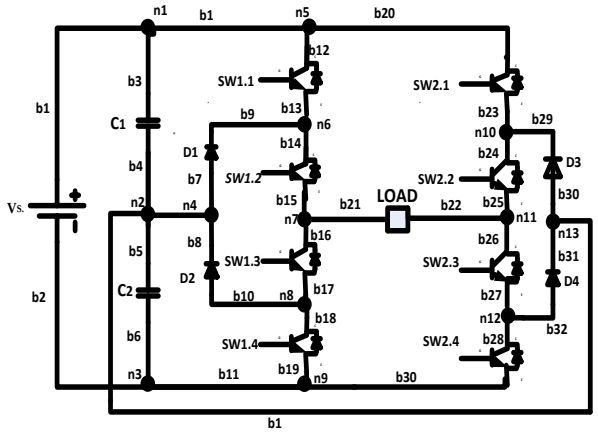

Fig. 1: Convectional Diode Clamped Inverter [25]

So, for a complete cycle operation of Fig.1, it experiences both positive and negative half cycles. During the positive half cycle, *vo*=Vs *and vo*= Vs/2. And during the negative half cycle, *vo*=-Vs *and vo*=- Vs/2. *vo*=0V is produced when it is changing from positive half cycle to negative half cycle and vice versa. This shows that five output voltage levels (i.e Vs , Vs/2, 0, Vs , Vs/2) are generated in Fig.1 for every cycle of its operation across the load point.

3 Non-Zero Triangular-Based Unipolar Modulation Scheme

Non-zero triangular- based unipolar modulation scheme (NZTBUMS) is modulation technique meant for producing triggering signals for switching the power circuit in Fig.1. The NZTBUMS is made of two carrier signals (triangular signals), Vc.1, Vc.2 and two reference (modulating) signals Vr.1, Vr.2. The Vc.1 and Vc.2 are free from zero voltages while Vr.1 and Vr.2 are phase shifted by 180^{o}to each other. They are represented mathematically as in eq.s (1), (2), (3) and (4)

$$\mathbf{V}_{c.1}=\begin{bmatrix} 0 & \frac{1}{4f} & \frac{1}{2f} & \frac{3}{4f} & \frac{1}{f} \\ Vp & 2Vp & 3Vp & 2Vp & Vp \end{bmatrix} \quad (1)$$

$$\mathbf{V}_{c.2}=\begin{bmatrix} 0 & \frac{1}{4f} & \frac{1}{2f} & \frac{3}{4f} & \frac{1}{f} \\ -3Vp & -2Vp & -Vp & -2Vp & -3Vp \end{bmatrix} \quad (2)$$

Where f and V_p represent the switching of carrier frequency and amplitude voltage of the carrier. The Vr.1 and Vr.2 are expressed as in eq.s (3) and (4) [26]

$$\mathbf{V}_{r.1}=Vm\left[\cos\frac{\pi}{2}\cos\theta+\sin\frac{\pi}{2}\sin\theta\right] \quad (3)$$

$$\mathbf{V}_{r.1}=Vm\left[\cos\frac{\pi}{2}\cos\theta-\sin\frac{\pi}{2}\sin\theta\right] \quad (4)$$

V_m and θ are the peak voltage of the modulating signal and the phase angle.

The switching operations of Fig.1, NZTBUMS is illustrated from eq.5 to eq.12. During the positive half cycle, eq.5 to eq.8 are carried out.

$$\begin{matrix} S_{w1.1} \\ S_{w1.2} \end{matrix}=\begin{cases} 1 \\ 1 \end{cases} \text{ if } V_{r.1}>V_{c.1} \text{ and phase of } V_{r.1} \text{ is equal to } 0 \quad (5)$$

Consequently, after processing eq.5, the next line of action is eq.6

$$\begin{matrix} S_{w1.1} \\ S_{w1.2} \end{matrix}=\begin{cases} 1 \\ 0 \end{cases} \text{ else if } V_{r.1}<V_{c.1} \text{ and } V_{r.1}>V_{c.2} \quad (6)$$

$$S_{w1.3} = \overline{S_{w1.1}} \quad (7)$$

$$S_{w1.4} = \overline{S_{w1.2}} \quad (8)$$

During the negative half cycle, eq.9 to eq.12 are being processed for switching
the Fig.1, leg2.

$$\begin{matrix} S_{w2.1} \\ S_{w2.2} \end{matrix} = \begin{cases} 1 \\ 1 \end{cases} \text{ if } V_{r.2} > V_{c.1} \text{ and } \text{phase of } V_{r.2} \text{ is equal to } \pi \quad (9)$$

$$\begin{matrix} S_{w2.1} \\ S_{w2.2} \end{matrix} = \begin{cases} 1 \\ 0 \end{cases} \text{ else if } V_{r.2} < V_{c.1} \text{ and } V_{r.2} > V_{c.2} \quad (10)$$

$$S_{w2.3} = \overline{S_{w2.1}} \quad (11)$$

$$S_{w2.4} = \overline{S_{w2.2}} \quad (12)$$

The circuit diagram for implementing the Vr.1, Vr.2 Vc.2 and Vc.2 is illustrated Fig.2. It consists of triangular generator, level shifter, sinewave generator, microcontroller (ATmega328p) and drivers. The carriers and modulating signals in Fig.2 are generated using one TL084 and resistor-capacitor-zener diode combination.

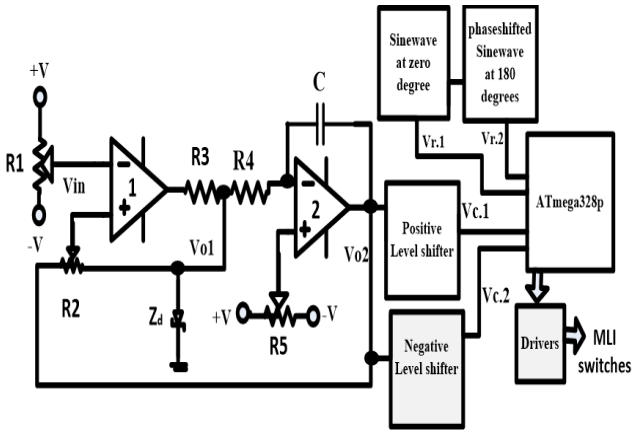

Fig. 2: Non-zero triangular- based unipolar modulation scheme topology

Fig. 2 displayed Non-zero triangular- based unipolar modulation scheme topology. The practical frequency of the carrier of proposed system is determined using the concept of transfer function [27]-[28]. The transfer function, T_s of the system is expressed as in eq.13.

$$T_s = \frac{V_{o2}}{V_{in}} \quad (13)$$

V_{in}, the input voltage at operational amplifier, Op Amp, **1**, V_{o2}, output voltage of the Op Amp.2.
But the output voltage of the operational amplifier 1, V_{o1} with respect to resistances R2 and R3 and voltage V_{in}, of Fig. 2, is expressed as:

$$V_{o1} = \frac{V_{in} R_3}{R_2} \quad (14)$$

And this V_{o1}, is equal to the input voltage of Op Amp, **2**
Besides, taking into consideration, the second Op.Amp.**2** of Fig.2, the transfer function of the integrator becomes:

$$\frac{V_{o2}}{V_{o1}} = \frac{1}{1 + jR_4\omega C} \quad (15)$$

When the expression in eq.14 is inserted into eq.15, then the eq.16 emerges as:

$$\left|\frac{V_{o2}}{V_{in}}\right| = \frac{1}{\sqrt{1 + (\mathrm{R}_4\omega C)^2}} * \frac{R_3}{R_2} \quad (16)$$

Assuming R_2=R_3, the face of eq. 16 becomes:

$$\left|\frac{V_{o2}}{V_{in}}\right| = \frac{1}{\sqrt{1 + (\mathrm{R}_4\omega C)^2}} \quad (17)$$

In order to get the carrier frequency *f*, the magnitude of eq.17 is set equal to $1/\sqrt{2}$, to which is the cut-off frequency transfer, according to the author already seen in [28], there emerges eq.18 as.

$$\frac{1}{\sqrt{1 + (\mathrm{R}_4\omega C)^2}} = \frac{1}{\sqrt{2}} \quad (18)$$

The circular and switching frequencies of Fig.2 are deduced in eq.19 and 20

$$\omega = \frac{1}{R_4 C} \quad \text{(rad/s)} \quad (19)$$

$$f = \frac{1}{2\pi R_4 C} \text{ (Hz)} \quad (20)$$

It can be noticed that R_4 is the only resistor that specifically adjusts the frequency of the carriers
Then, the output voltage of the triangular wave circuit and the level shifter voltages are expressed in:

$$V_{c.1} = \frac{[V_{o2} - a]}{k} \quad (21)$$

$$V_{c.2} = \frac{-[V_{o2} + b]}{k} \quad (22)$$

Where "**a**" and "**b**" are the positive and negative offset voltages while "k" is the gain factor which ensures that analog entries into Atmega328p are accommodated. The boundary conditions of the offset voltages with respect to amplitude voltage of

the carriers, V_p, are $0 < a \leq V_p$ and $0 > -b \geq -V_p$.

4 MatLab Model, Simulation Results and Discussion

Fig.3 displayed the MatLab/ Simulink model of the power circuit and the proposed modulation technique. In addition that, it showed that under resistive load, the total distortions of both output current and voltage is 0.4575%.

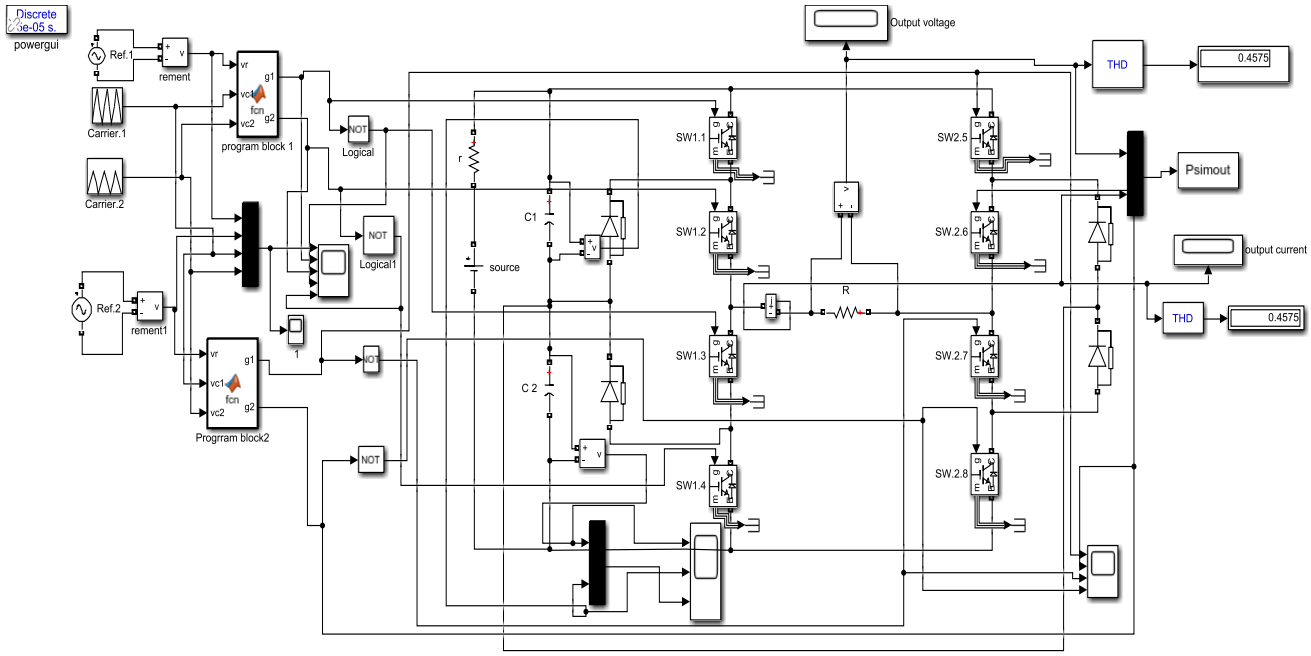

Fig. 3: MatLab Models of the MLI power circuit and it proposed scheme

The Non-zero triangular- based unipolar modulation scheme waveforms are shown in Fig.4. It is made of two carrier waves (Vc.1 and Vc.2) of the same magnitudes but at different positions as well as two modulating signals of the equal amplitudes but are phase shifted at 180° from each other. And they have already been mathematically represented in eq.1-4. It is noticed that NZTBUMS has only two carrier and two reference signals making the whole NZTBUMS total signals to be four signals for switching Fig.1 unlike conventional multicarrier pulse width modulated schemes that have five signals and above for switching a similar topology as in Fig.2 . It is observed that Fig.4 showed the comparison between the two zero-free carrier waves of eqs.3 and 4 with the two modulating signals of eqs.1 and 2.

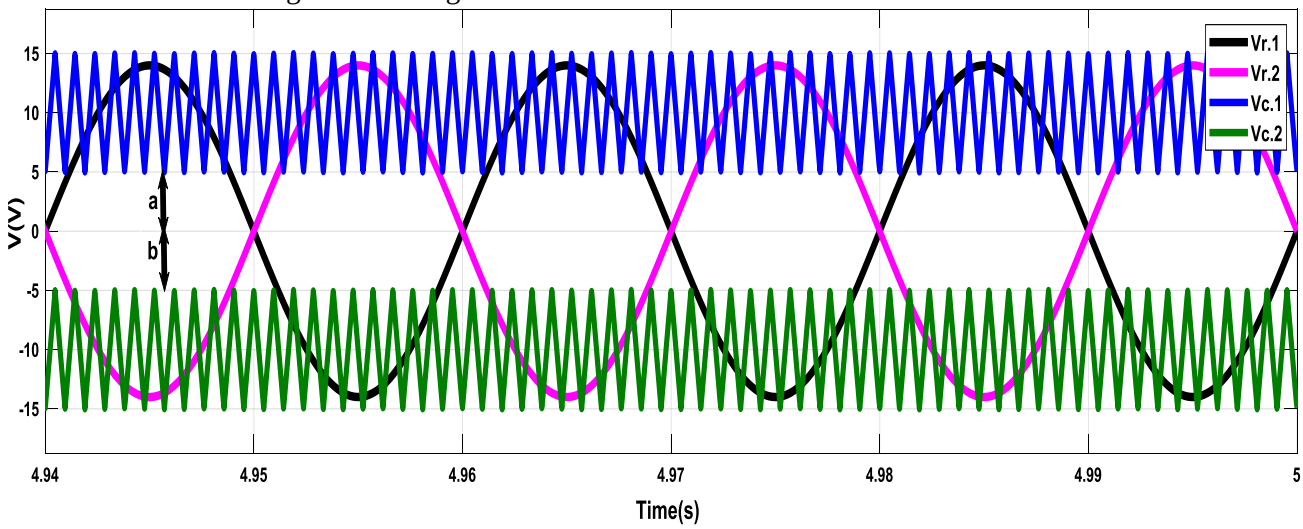

Fig. 4: Simulated waveforms of proposed scheme non-zero triangular- based unipolar modulation scheme

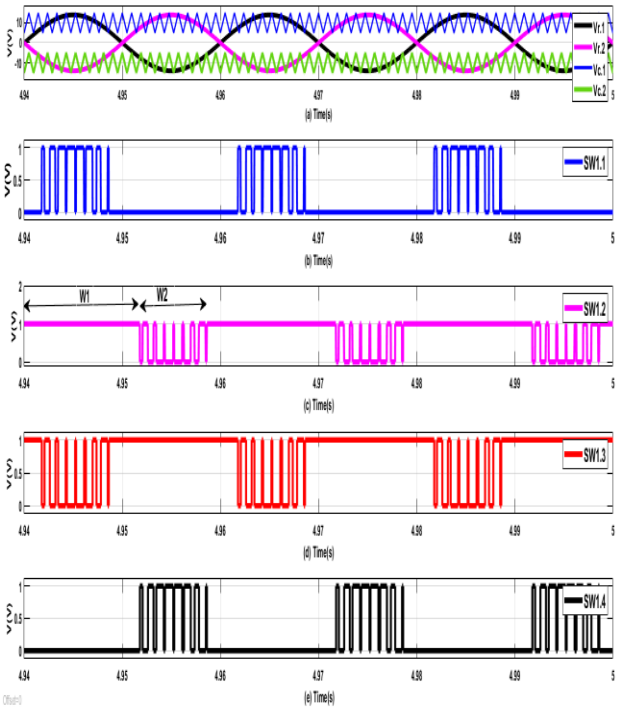

Fig. 5: Simulated Waveforms of proposed scheme (NZTBUMS) and it switching signals for Leg.1

The firing signals for the second leg in Fig.1 are represented in Fig.6e, 6f, 6g and 6h. It is observed that Fig.6g is complementing Fig.6e while Fig.6h is a complement of Fig.6f. They possess similar characteristics like Fig.5

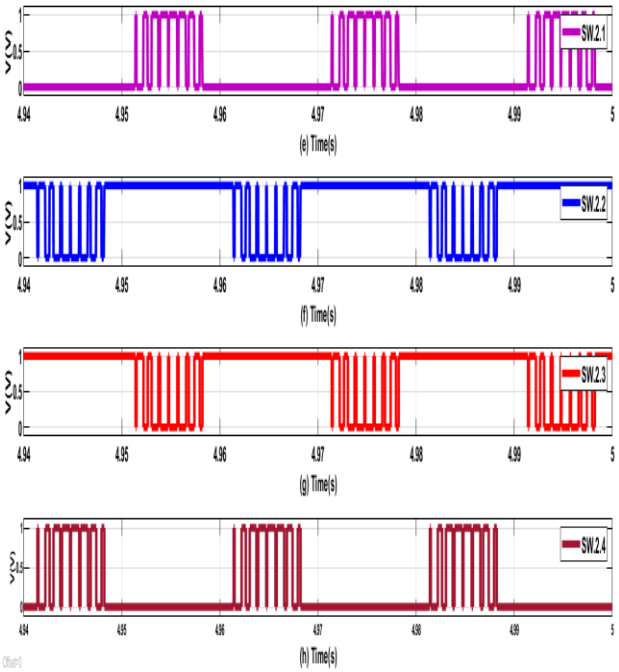

Fig. 6: Simulated Waveforms of proposed scheme (NZTBUMS) switching signals for Leg.2

Fig.7 signifies balanced input capacitor voltage under NZTBUMS. It is evident that Fig.7a and Fig.7b have equal 200V across C1 and C2 throughout the span of 5 seconds without changing. Fig.7c also showed where the V.C1 and V.C2 are plotted together. And it clear that they And it clear that they have the same voltage magnitudes at time interval of same 5 seconds.

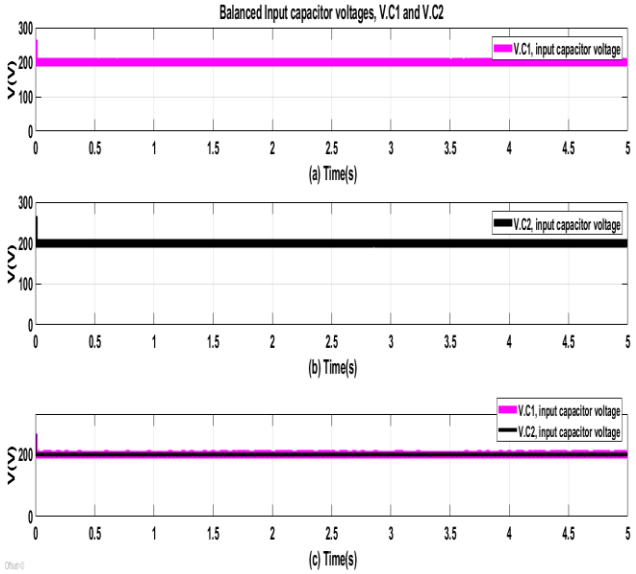

Fig. 7: Balanced input capacitor voltages using NZTBUMS

The output voltage waveform across the resistive load of Fig. 1 is shown in Fig.8. It has stabilized five line-to-line output voltage levels with peak voltage of 400V at $4.85 \leq t \leq 5 seconds$. It is noticed that there is no voltage drops beyond 0.1second using NZTBUMS, which cannot be released with other convention scheme without using extra compensating circuitries. Even beyond seconds, the quality of voltage waveforms remain the shape.

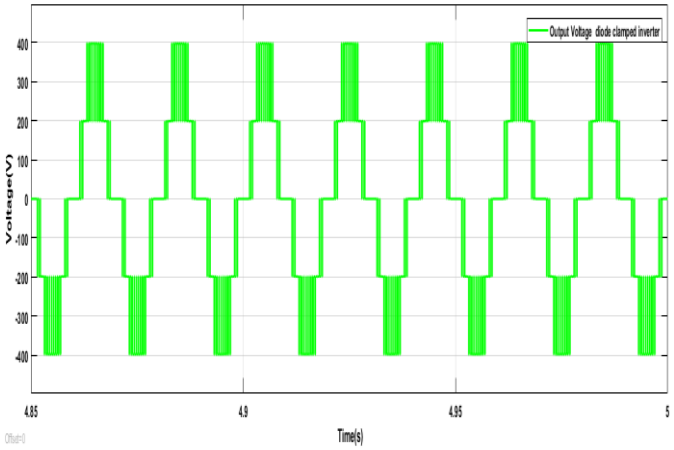

Fig. 8: 5-level line-to-line output voltage waveform of the diode-clamped multilevel inverter

The spectral characteristics of output voltage is shown in Fig.9. It indicated that at fundamental frequency of 50Hz and maximum voltage of 400V, the system output voltage has the total harmonic distortion (THD) of 0.4575%. And the THD value corresponded to the value already shown in Fig.3

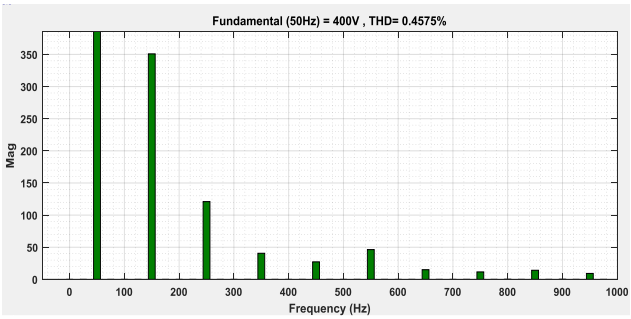

Fig. 9: Spectral analysis of total harmonic distortion of output voltage of the diode-clamped MLI

Fig.10 represented the output current wave shape of the MLI under resistive load. It mimics Fig.8 except that it has lower amplitude. The peak current value is 20A. The power output of the MLI in this research when the peak value of Fig.8 is multiplied by the maximum value of Fig.10 is 8kW.

Fig.11 depicted the spectral analysis of total harmonic distortion of output current of the MLI. It is observed that it has THD of 0.4575% like voltage. This showed that both voltage and current under the resistive load are in phase.

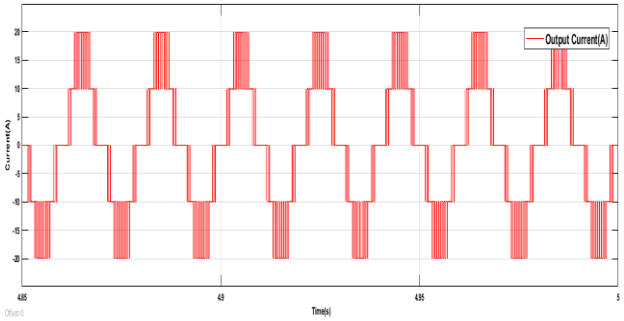

Fig. 10: 5-level line-to-line output current waveform of the multilevel inverter

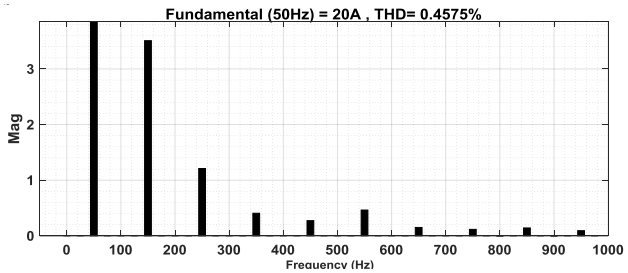

Fig. 11: Spectral analysis of total harmonic distortion of output current of the MLI

The statistical probabilistic analysis of both current and voltage excursions are displayed in Fig.12. The levels that spanned from -20A to +20A along the horizontal axes represent the current output statistical analysis. In Fig.12, the level 1, 2, 3, 4 and level 5, counting from the negative half cycle to positive half cycle, have the probabilities of 0.1, 0.25, 0.25, 0.75 and 0.9. Similarly, the levels that covered from -400V to +400v along the horizontal axes represent the voltage output numerical analysis. It is also showed that level 1, 2, 3, 4 and level 5, counting from the negative half cycle to positive half cycle, have the same probabilities of 0.1, 0.25, 0.25, 0.75 and 0.9. This implies that the current and voltage under restive load are in phase

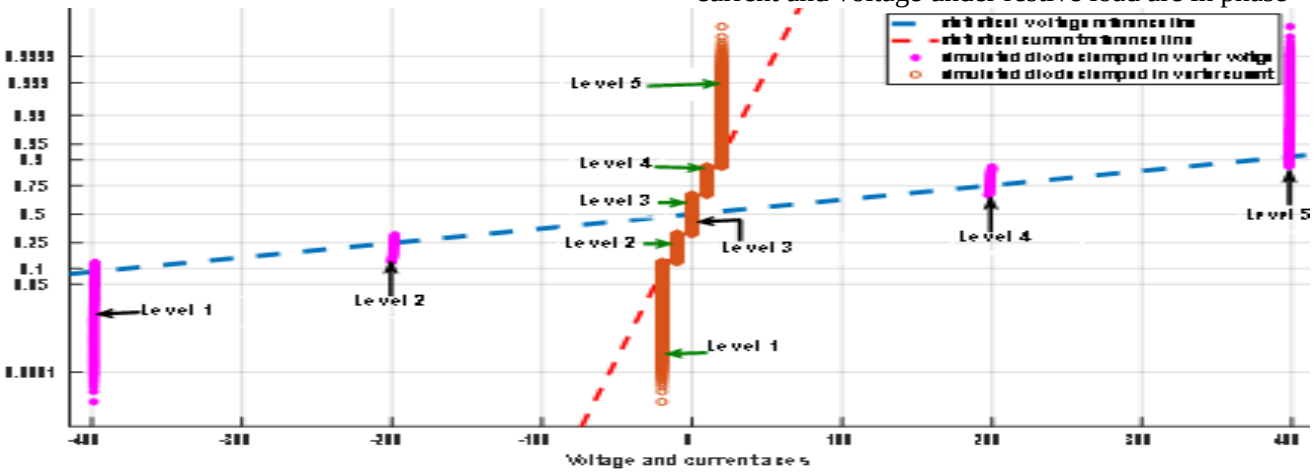

Fig. 12: Statistical analysis of voltage and current waveforms of the diode clamped multilevel inverter based on the proposed scheme

Fig.13 illustrated 3-D plot of voltage and current waveforms of the MLI with respect to data points. It designated that the minimum and maximum voltage of the MLI across the load are -400V and 400V

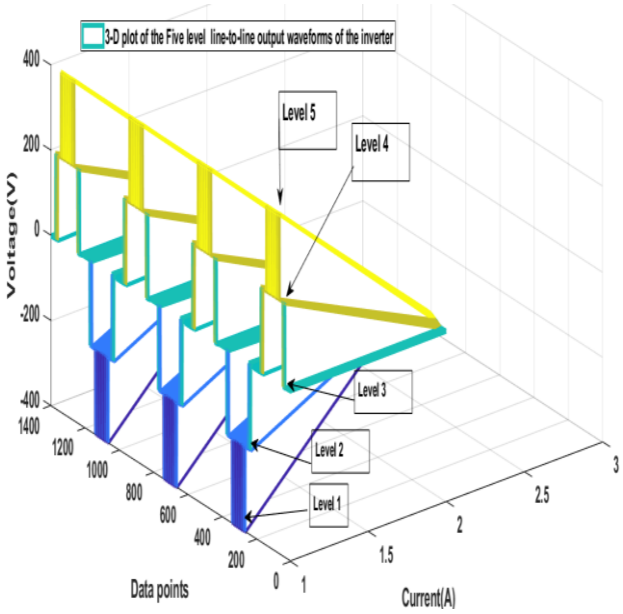

Fig. 13: 3-D plot of voltage and current waveforms of the MLI with respect to data point

5 Experimental Results and Discussion

The experimental result waveforms of the proposed scheme and its experimental set-up are shown in Fig.14-21. The experimented analog oscilloscopic display of the two modulating sinewaves in Fig.14 has already been expressed in eq. 3 and eq.4 and simulated in Fig.4. This implies that they resemble each other

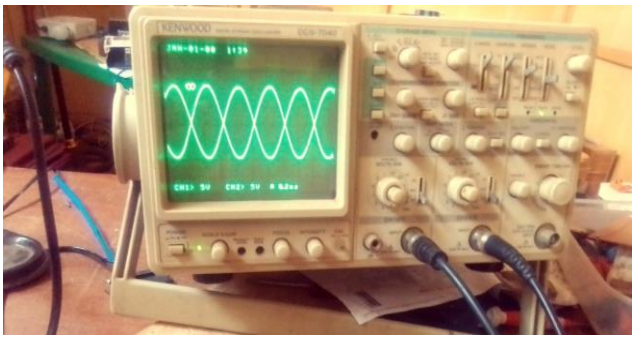

Fig. 14: Experimented waveforms of two modulating reference voltages

Fig.15 showed implemented two zero-free carrier waves. Those carrier waves have been mathematically shown in eq.1 and 2, simulated in part of Fig. 4 and practically shown in Fig.15. In order to show the gapping between the Vc.1 and Vc.2 as well as the practical comparison with the reference signals, Fig.16 and 17 emerged.

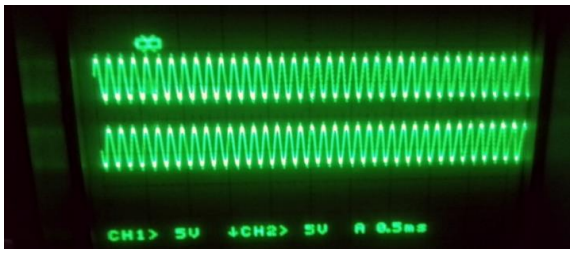

Fig. 15: Experimented waveforms of carrier voltages

In Fig.16, the positive zero-free carrier wave was compared with the modulating sinewave to generate the triggering pulses. The comparison between the signals has been shown in eq.5, simulated as part of Fig.4 and shown in experimented form in analog oscilloscope in Fig.16. It is observed that the zero-free positive triangular wave is above the sinewave in order to avoid over modulation.

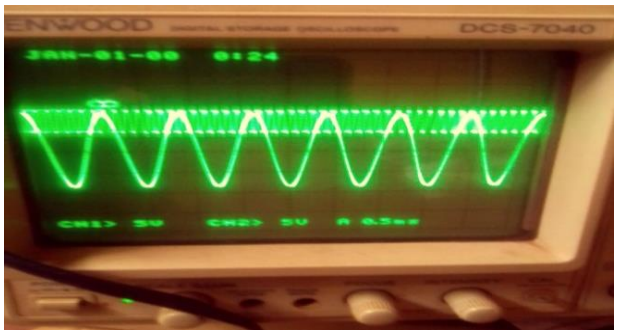

Fig. 16: Experimented waveforms of modulating voltage and positive carrier wave form

A zero-free negative carrier wave was compared with the 180^{o} phase shifted reference signal in Fig.17. The MatLab/Simulink simulated form of it, has been shown in part of Fig.4 and its arithmetic expression was deduced in eq.9

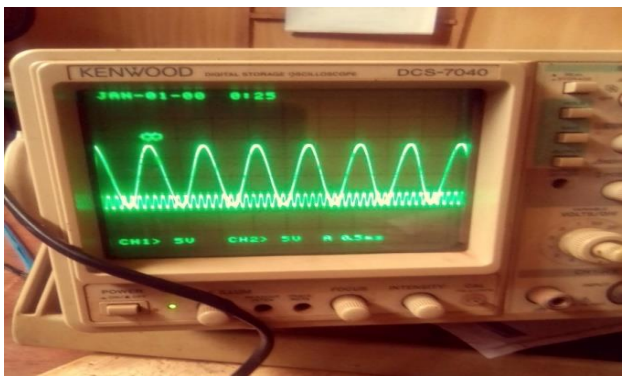

Fig. 17: Experimented waveforms of modulating voltage and Negative carrier waveform.

The triggering pulses were generated when the comparative results of Fig.16 and 17 were further processed by Atmega328p and drivers (TLP 250 and VO3120). Fig.18 showed generated triggering pulses for switching SW1.1 and SW.13 obtained from the output of the driver's circuit. It is observed that they are complementing each other. And also, they have two distinctive regions which reduce both low and high harmonic distortions as already seen in simulated results of Fig.5.1 and Fig.5.2

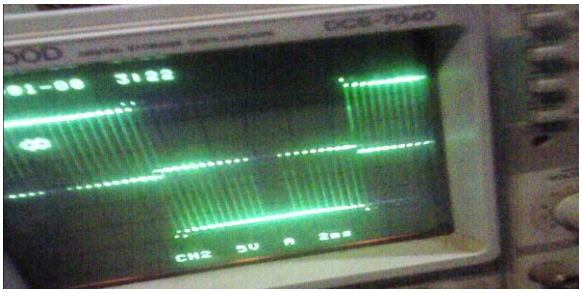

Fig. 18 Experimented waveforms of triggering pulse-width modulated signals

A five level line-to –line output voltage across a resistive load is shown in Fig.19. It is realized that there is no voltage drop at each level of excursion. This show that there is a stabilized output voltage using NZTBUMS. It is noticed that it resembles the wave form in Fig.7

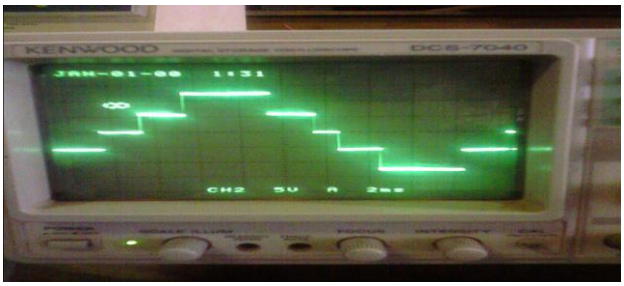

Fig. 19: Experimented waveforms of 5-level line-to-line Output voltage of the MLI

Fig.20 illustrated an experimented un-energized prototype of the proposed scheme and power MLI.

Fig. 20: Experimented Un-energized Laboratory prototype

Complete experimented and energized prototype of the proposed scheme and diode-clamped MLI power circuits were practically shown in in Fig.21. It can be observed that it consists of power supply unit for NZTBUMS, NZTBUMS section, Atemega328p, drivers, MLI section, battery section, load light, analog oscilloscopic display and protective unit. It also indicated that NZTBUMS occupies small space with low component counts as well as realizable for switching diode-clamped multilevel inverter used in generation five level line-to-line output voltage.

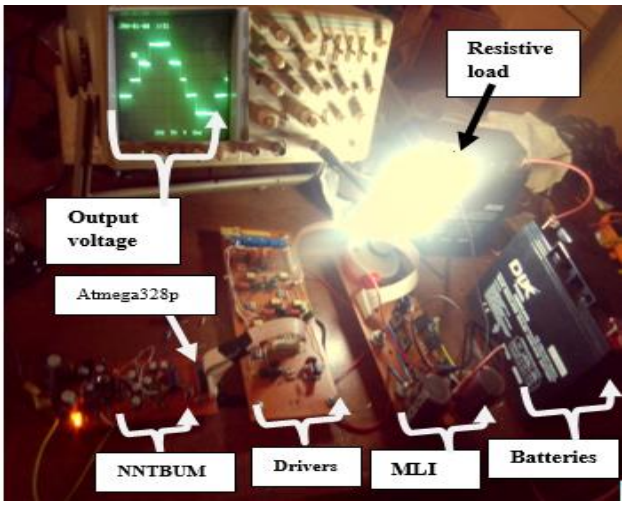

Fig. 21: Experimented energized prototype of the proposed scheme and power circuit

6 Conclusion

An improved conventional diode-clamped multilevel inverter using non-zero triangular-based unipolar modulation scheme has been analyzed, modelled, simulated in MatLab/Simulink software 2018 and pragmatically implemented in Laboratory of Industrial Electronics, Power Devices and New Energy Systems. The proposed modulation system scheme and the output waveforms of diode-clamped MLI have been showed on two channel analog oscilloscope. It was observed that the simulation results and the practical waveforms resembled one another very closely. Therefore, the experimental prototype validates the simulated results of the proposed system.

It was also noticed that the NZTBUMS occupied small space and has less number of carrier signals unlike the conventional modulation schemes, hence, leading to low component counts and better performance.

The results produced by the proposed scheme on switching diode-clamped MLI are: voltage and

current with total harmonic distortions of 0.4547%, stabilized 400V output voltage and 20A output current, probability results at each five levels of voltage and current occurrences corresponded to 0.10, 0.25, 0.25, 0.75 and 0.90; and power output of 80kW. The research work also presented that the statistical plot of voltage and current is another way of showing that under resistive load, the voltage and current waveforms are in phase.

Future research:
NZTBUMS will be in future research, applied in higher diode-clamped multilevel inverters and other hybrid multilevel inverters to determine their performance characteristics.

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References:
[1] R. Bensraj and S.P NataragaN, *multicarrier trapezoidal PWM strategies for single phase five cascaded Inverter*, Journal of Engineering and Science, Vol.5, N0 4, Jan. 2010 pp. 400-411.

[2] Candidus.U. Eya, O. Crescent, J. M. Ukwejeh, *Solar- powered five level output voltage of dc-to-AC converter using simplified capacitor voltage-controlled scheme*, **IEEE** PES/IAS Power Africa, Abj, Nigeria, 2019. pp. 1-6, DOI: 10.1109/PowerAfrica46609.2019.9078670.

[3] M. H. Rashid, *Power Electronics Hand book*. 3rd Ed. Butterworth-Heinemann, 30 Corporate Drive, suite 400. Burlington, MA 01803, USA, 2011.

[4] Marcel U. Agu, Principles of Power Electronics Circuits, UNN Press, Nigeria, 2019.

[5] Djamila Cherifi, Yahia Miloud and Mohamed Mostefai, *Performance of Neutral Point Clamped Five Level Inverter Using Space Vector Modulation Control Fed by DPC-VF-SVM Rectifier*, **Wseas** Transactions on Power Systems, Vol. 16, 2021, pp.275-287,DOI:10.37394/232016.2021.16.28

[6] Han, Y., X. He, C. Tan, J. Cheng, and R. Zhao, *Multilevel circuit topologies based on the switched capacitor converter and diode-clamped converter, **IEEE** Transaction*. Power Electron, Vol. 26, No. 8, 2011, pp.2127–2136

[7] Dargahi, V. S, A.K and Corzine, K, *Analytical Determination of Conduction Power Losses for Active Neutral Point Clamped Multi-Level Converter*, in Proceeding, **IEEE** Appl. Power Electron. Conferences, 2016, pp. 720-727. https://doi.org/10.1109/APEC.2016.7467951

[8] M. Saeedifard, H. Nikkhajoei, R. Iravani and A. Bakhshai, *A Space Vector Modulation Approach For A Multi- Module HVDC Converter System, **IEEE** Transactions on Power Delivery*, Vol.22, No.3, PP.1643-1654, July, 2007.

[9] Amirnaser Yazdani and Reza Iravani, *Voltage-Sourced Converters In Power Systems Modeling, Control, and Applications*, **IEEE** Press, A John **Willey** and Sons Inc., Hoboken, New Jersey Published simultaneously in Canada, 2010.

[10] J. M Rao Malla and S.Ganesh Malla**,** *Five Level Parallel Inverter for DTC – SVM of Induction Motor*, **Wseas** Transactions on Power systems pp:273-286.

[11] C.R. Balamurugan, S.P. Natarajan, R. Bensraj and T.S. Anandhi, *Hybrid Carrier PWM Strategies for Three Phase H-bridge Multilevel Inverter*, **Wseas** Transactions on Power systems, 2016, pp:90-99.

[12] Shunji Shi, X. Wang and S. Zheng and Fei Xia2, A New Diode-Clamped Multilevel Inverter for Capacitor Voltage Balancing, Progress In Electro. Research M, Vol. 52, 2016, pp.181–190.

[13] Candidus U. Eya, Ayodeji O. S and Stephen Ejiofor O, *High Performance DC-to-AC Converter Using Snubber-less H-Bridge Power Switches and an Improved DC-to-DC Converter*, International Journal of Circuits, Systems and Signal Processing, , Vol.15, 2021. pp. 315-333.

[14] J. Ebrahimi, E. Babaei, G. B. Gharehpetian , *A new multilevel inverter topology with reduced*

number of power electronic compon., **IEEE** Trans. Ind. Electr., vol. 59, N0.2 Feb 2012, pp. 655-667.

[15] B. S. Muhammad, H. Ammar, I. A. Mian, *A New Multilevel DC-AC Converter Topology for Grid-Connected Photovoltaic Systems*, Hindawi, International Journal of Photo-energy,2018, pp: 1-9,

[16] R. P. Sridhar, K. Georgios, G. A. Vassilios, *Hybrid seven-level cascaded active neutral-point-clamped-based multilevel converter under SHE-PWM*, **IEEE** Transactions on Industrial Electronics, 60(11), 2013, pp. 4794-4804.

[17] T.Sunitha and T.Annamalai, *A New 23 Level Cascaded Multilevel Inverter with Optimum Structure*, Conference, 4th International Conference on Electrical Energy Systems (ICEES), 2018, pp.320-326. DOI: 10.1109/ICEES.2018.8443220

[18] Omeje, C. O , Nnadi, Damian., Odeh, C. I , Eya, C. U, Oti, Stephen E, *Analysis of a three phase capacitor voltage balanced hybrid multi-level inverter with a three phase RL-load*, International Journal of Engineering & Technology, 9(1) 2020, PP.133-148.

[19] Rodríguez, J, Bernet, S, Wu, B. Pontt, J.O. and Kouro, S, *Multilevel voltage-source-converter top.s for industrial medium voltage drives*, **IEEE** Transaction. Ind. Electronics. Vol.54, 2007 pp.2930–2945.

[20] A. Jidin, N. R. N. Idris, A. H. M. Yatim, T. Sutikno and M. E. Elbuluk, *An optimized-switching strategy for quick dynamic torque control in DTC hysteresis based induction machines*, ***IEEE*** *Transaction*. Industrial Electron, vol. 58, no. 8, pp. 3391–3400, 2011.

[21] M.S Rajaan and R. Seyezhazi, *Comparative Study of Multilevel PWM Techniques for a Modular Multilevel Inverter*, International Journal of Engineering and Technology, Vol.5, Dec, Jan, 2014.

[22] Jani Rushshiraj G and Prof . P.N Kapil, Analysis of different Modulation Techniques for Multilevel Inverter,"Computer Science, **IEEE** 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES) March 2016. DOI:10.1109/ICEEOT.2016.7755254.

[23] C.O. Omeje, C.I. Odeh, D.B. Nnadi, M.U. Agu, E.S. Obe, *Space Vector Pulse Width Modulation of A Multi-Level Diode Clamped Converter With Experimental Verification*, Nigerian Journal of Technology, Vol. 30, No. 2, June 2011.

[24] T. Kamal, S.Z. Hassan, S. Z. Naqvi and Imranullah, *Development of Improved Diode Clamped Multilevel Inverter Using Optimized Selective Harmonic Elimination Technique*, Emerging Trends in Electrical, Electronics & Instrumentation Engineering: An international Journal (EEIEJ), Vol. 1, No. 3, August 2014.

[25] M. H. Rashid, *Power Electronics Circuits, Devices and App*, 3rd Ed P. Hall India, 2004

[26] Candidus U. Eya, Ayodeji Olalekan Salau and Stephen Ejiofor Oti, *Constant and wireless controlled DC-to-AC based boost differential converter with a sensor-less changeover system*, Int J Syst Assur Eng Manag , 2021 doi.org/10.1007/s13198-021-01451-x

[27] Charles K. Alexender and Math N.O Sadiku, "*Fundamentals of Electric Circuits*, 4th Edition, McGraw-Hill Education, 2009.

[28] D. Roy Choudrhury, *Modern Control Engineering*, Prentice-Hall of India Private Limited, New Dehi-110 001, 2006

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