

Design and Implementation of High Speed and Low Power 12-bit SAR ADC using 22nm FinFET

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Abstract: Successive Approximation Register (SAR) Analog to Digital Converter (ADC) architecture comprises of sub modules such as comparator, Digital to Analog Converter and SAR logic. Each of these modules imposes challenges as the signal makes transition from analog to digital and vice-versa. Design strategies for optimum design of circuits considering 22nm FinFET technology meeting area, timing, power requirements and ADC metrics is presented in this work. Operational Transconductance Amplifier (OTA) based comparator, 12-bit two stage segmented resistive string DAC architecture and low power SAR logic is designed and integrated to form the ADC architecture with maximum sampling rate of 1 GS/s. Circuit schematic is captured in Cadence environment with optimum geometrical parameters and performance metrics of the proposed ADC is evaluated in MATLAB environment. Differential Non Linearity and Integral Non Linearity metrics for the 12-bit ADC is limited to +1.15/-1 LSB and +1.22/-0.69 LSB respectively. ENOB of 10.1663 with SNR of 62.9613 dB is achieved for the designed ADC measured for conversion of input signal of 100 MHz with 20dB noise. ADC with sampling frequency upto 1 GSps is designed in this work with low power dissipation less than 10 mW.

Key Words: SAR ADC, 22nm FinFET, Low Power, High Speed, Folded Resistive String, Operational Transconductance Amplifier.

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1. Introduction

The links between analog world of transducers and digital world of signal processing and data handling are Analog to digital converters(ADC) and Digital to analog converters(DAC).The A/D interface to reside on the same silicon with large DSP or digital circuit is due to increasing trend of integration level of integrated circuits. Scaling in transistor geometries have resulted in low voltage references for operation of digital circuits. ADCs that are interfaced with DSPs blocks also needs to operate at low voltages. Among the most popular Nyquist rate ADCs SAR ADCs are important because of high speed conversion and low voltage operation. Compared with other types of ADC, SAR ADCs exhibit the best energy efficiency for medium to high speed, moderate resolution and low power applications. Aili Wang et al.[1] have designed a 10-bit SAR register ADC with SNDR of 59.59 dB and power dissipation limited to 41.3 μ W operating at maximum

frequency of 50 MS/s using 14 nm SOI FinFET technology. The number of capacitors in the ADC is reduced using segmented architecture. Aligned switching with Skip (ASS) logic is used to save power dissipation. The SAR logic is based on VCM-based MCS Scheme which saves power dissipation further by 85%. Dual mode power is used to further reduce power dissipation. Lukas Kull et al.[2]presented an 8-bit Time-interleaved ADC that is designed to operate in the 24-72-GS/s. The SNDR at low frequency is 39 dB and 30 dB at Nyquist frequency. The Time-interleaved ADC uses 64 asynchronous SAR ADCs to perform the conversion. 14-nm CMOS FinFET technology is used in the design that requires 0.15 mm² area. James Hudner et al.[3] in their work, proposed SAR ADC that operates at 56GS/s and is based on time interleaved logic using 16nm FinFET technology. The power dissipation is limited to 475 mW. Sung-En Hsiehet al.[4] presenteda 11-bit SARADC that

uses semi resting DAC and cascaded input comparator. The designed ADC operating at 600-kS/s with 0.3 V supply voltage requires 187 nW of power dissipation. The SFDR is 73 dB at 9.46 bits. Keisuke Okuno et al.[5] in their work reported on 8-bit SAR ADC using 16 nm FinFET. The time interleaved ADC is designed to operate at 800 MS/s with ENOB of 6.53 bits. The results of designed ADC are compared with several other ADCs demonstrating superiority in performances. Ashish Joshi et al.[6] have designed ADC using 45nm FinFET models based on SAR logic that is designed to operate at 909 kS/s with 9 μ W of power dissipation. The ADC uses switch capacitor DAC and opamp based comparator circuit. Ewout Martens et al., [7] have designed ADC based on SAR logic using 16nm CMOS FinFET models that operates at 300 MS/s with ENOB of 11.2 bit. The power dissipation is 3.6 mW with 76 dB harmonic distortion. Zhiliang Zheng et al.,[8] presented a new technique for error cancellation in SAR ADCs. In this technique, the conversion time is increased by 50% to cancel the first order capacitor mismatch error, where typically 100% additional conversion time is needed compared to the ideal operation. Gilbert Promitzer [9] presented a paper on non calibrating SAR ADC with fully differential switched capacitor for low power with 12 bit resolution. The power consumption is reduced because of cancellation of the VCM buffer and by implementing self timed comparator. To achieve lower power consumption and higher sampling rate the resolution was improved from 10 bit to 12 bit. Eric Fogleman et al.,[10] presented a technique to reduce in band noise of DAC block in ADC architecture. Using a second order 33-level tree structured mismatch shaping DAC an audio ADC Delta-Sigma modulator is designed. The prototype modulator is implemented in a standard

0.5 - 3.3V single-poly CMOS fabrication process. All 12 of the fabricated prototypes achieve a 100dB peak signal-to noise and distortion ratio (SINAD) and 102dB dynamic range over a 10–20 kHz measurement bandwidth. John McNeill et al.,[11] presented the “Split ADC” architecture. The “Split ADC” architecture uses two independent and identical ADCs to sample the same input, V_{in} . The two independent outputs are averaged to produce the ADC output code. The difference of the two outputs provide information for the background

calibration process. Mi-rim Kim et al.,[12] presented a 12-bit SAR ADC with hybrid RC DAC. The hybrid RC DAC is employed to reduce the size and improve energy efficiency by reducing the total number of capacitors. The prototype ADC fabricated in a 180 nm CMOS and occupies 0.25 mm² active die area. The measured DNL and INL are +0.47/-0.48 LSB and +0.75/-0.76 LSB respectively. The ADC shows the maximum SNDR of 64.2 dB and SFDR of 80.4 dB with a 2.8V Supply consuming 1.16mW. Dragisa Milovanovic et al.,[13] presented second order sigma-delta modulator in CMOS 0.35 μ m technology for audio applications. In this they presented a technique to improve the swing, dynamic range and stability analysis of the second order sigma-delta modulator by scaling the gain of the integrators. The area occupied by this design is 0.57 mm². Oguz Altun et al.,[14] presented the multi rate multi bit sigma-delta modulator for low power implementation in 90 nm for wireless application. This design achieves 71.4 dB SNDR in 200 kHz GSM band and dissipates 1.1 mA of total current from a 1.5 V Supply. Victor Aberg[15] in his master's thesis in Embedded Electronic system have presented a design of SAR ADC using 28 nm FD-SOI CMOS technology that comprises of scaled Capacitive DAC. The ADC has been designed to operate at 800 MS/s with SNDR of 38.4 dB and consumes power less than 1.1 mW.

In this work a 12-bit SAR ADC is designed and implemented for high speed and low power using 22 nm FinFET technology. This paper is organized as follows: Section 2 describes SAR ADC architecture. Section 3 provides design of SAR ADC. Section 4 presents FinFET and Section 5 presents Design of SAR Logic Block which includes power estimation, DAC design and Comparator design. Section 6 describes the implementation of SAR logic block, DAC and Comparator. Section 7 presents Results and Discussion. Section 8 concludes the paper.

2. SAR ADC

The block diagram of SAR ADC is as shown in Figure 1. In a Successive Approximation Register Analog to Digital converter, the input signal V_{in} is sampled at the beginning of each conversion cycle. The process of conversion starts by comparing the input signal V_{in} and the half reference voltage $V_{ref}/2$ to determine the MSB of V_{in} and also determines the search

region for the second MSB. The binary search algorithm is allowed to approximate the actual V_{in} , and the reference voltage is used for the MSB will be divided by 2. The result is added or subtracted from the previous reference voltage which delimitates the new binary search regions.

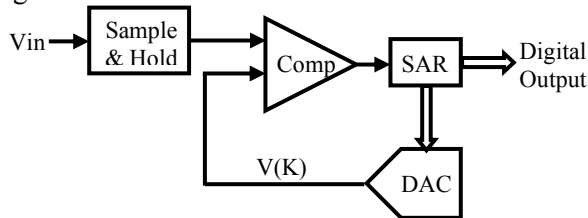


Fig-1. Block diagram of the SAR A/D converter[8]

Reference voltage updated and V_{in} , each comparison between them generates N-bits of SAR ADC and one bit of V_{in} which needs N Comparisons.

3. Design of SAR ADC

In this work SAR ADC is designed and implemented. The design is divided into sub blocks like DAC, comparator, SAR logic. The schematic of the sub blocks is designed using Virtuoso schematic editor. The simulations for the individual blocks were carried out using ELDO simulation tool. Integration of the sub blocks was done using virtuoso schematic editor. The specifications for SARADC (Table 1) is identified considering the reference design [16].

Table-1. Design specifications of SAR ADC

Resolution	12-bit
Technology	22 nm
Clock Rate	1GHz
Area	<1mm ²
Power Supply	1.8V
Operating Current	1mA
Input Range(V_{in})	0.2V-1.4V
Power Dissipation	<10 mW
INL	+/- 2 LSB
DNL	+/- 2 LSB
SNR (dB)	64 dB
SNDR (dB)	60 dB
SFDR (dB)	72 dB
ENOB	9.5

Several factors are considered for ADC design. The ratio in between the maximum input signal level and the minimum detectable input signal that the modulator can handle is called the Dynamic Range(DR).The ratio in power between the input sine wave and the noise of the converter from DC to Nyquist rate[15] is called

Signal to Noise Ratio(SNR). SNR is expressed in decibels and the equation is given in (1).

$$SNR = 10 \log \frac{P_{signal}}{P_{noise}} \dots \dots \dots (1)$$

The ratio of the signal power to the total noise and harmonic power at the output is called the Signal to Noise Plus Distortion Ratio(SNDR)[15].Harmonic content is present in SNDR which is not there in SNR, Otherwise they are similar. Distortion is not important for small signal levels. As the signal level increases and distortion degrades SNDR will be less than SNR. Equation of SNDR is given in (2).

$$SNDR = 10 \log \frac{P_{signal}}{P_{noise} + P_{distortion}} \dots \dots \dots (2)$$

The ratio of the power value of the input sine wave with a frequency $f(IN)$ to the power value of the peak spur observed in the frequency domain is called Spurious Free Dynamic Range(SFDR)[15].The ratio between the sampling frequency f_s and the Nyquist rate $f(IN)$ is called the Over Sampling Ratio(OSR). Since $f(IN) = 2fB$, the over sampling ratio equation is given in (3).

$$OSR = \frac{fS}{2fB} \dots \dots \dots (3)$$

Due to the periodical charge/discharge of load capacitances we get dynamic power dissipation and it is shown in equation (4).

$$P = \alpha \times VDD^2 \times Cs \times fN \times OSR \dots \dots \dots (4)$$

Where C_s is sampling capacitor, fN is system Nyquist rate, OSR is over sampling ratio and α is the average change of the voltage on the sampling capacitor. Static power dissipation P_{stat} is computed considering the current flow during static state of the circuit that is considered as leakage current and the power P_{stat} is given as in equation (5).

$$P_{stat} = VDD \times I_{stat} = VDD \times gm \frac{C_s}{C_i} V_s \dots (5)$$

The power dissipation in ADC is either due to higher sampling frequency or due to the power dissipation due to charging and discharging of the capacitors. Based on the factors that constitute power dissipation in ADC it is required to design the sub systems in ADC with low power strategies.

4. FinFET

Double Gate FinFET device shown in Figure 2 (a) and its characteristics demonstrating the increased current flow in the channel by controlling with two gate voltage is presented

in [17]. Small signal model for the DG FET is presented in Figure 2(b). C_{gd} , C_{gs} and C_{ds} are the parasitics in FinFET that limits the device

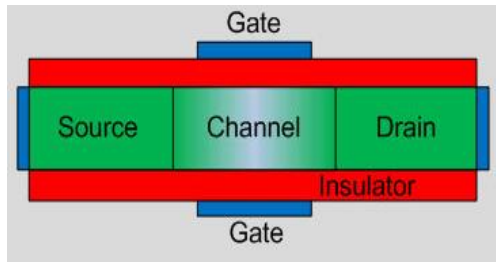


Fig-2. FinFET[17]

Fig-2(a). FinFET device structure of DGFET [17]

operation at high frequencies and R_{gd} , R_{gs} , R_{ds} and R_{sub} limits the device for low power operations.

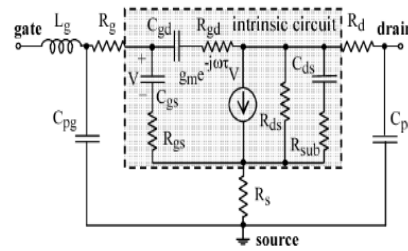


Fig-2 (b). FinFET Device Small signal model [17]

Predictive Technology Model (PTM) parameters for FinFET is presented in Table-2 and the corresponding model files are considered for design of OTA and OTA based comparator. Considering structural and electrical parameters of FinFET device modeling is carried out for analysis of input and output characteristics. The theoretical and practical mismatches are identified based on simulation results and the appropriate geometry settings for FinFET are identified for maximum frequency of operation and low power dissipation [18].

Table-2. FinFET Device Parameters

Parameter	Value
Channel length	22 nm
Oxide thickness 1	2.5 nm
Oxide thickness 2	2.5 nm
Gate length	22 nm
Source/drain extension length	50 nm
Gate to source/drain overlap	2 nm
Work function	4.6 eV
Source/Drain doping	$1 \times 10^{19} \text{cm}^{-3}$
Dielectric constant of channel	11.7
dielectric constant of insulator	3.9
Bandgap	1.12 eV
Affinity of channel material	4.05 eV
Mobility of electrons	$1400 \text{cm}^2/\text{Vs}$
saturation velocity	$1.07 \times 10^7 \text{cm/s}$

The building blocks of SAR ADC are designed using FinFETs and the design procedures are discussed in detail.

5. Design of SAR logic block

It is required to turn ON/OFF ADC reference current source switches, depending on comparator output at every clock till the end of conversion and generate the ADC data output. This logic is implemented in RTL. Block diagram of the SAR logic block is shown in the Figure-3.

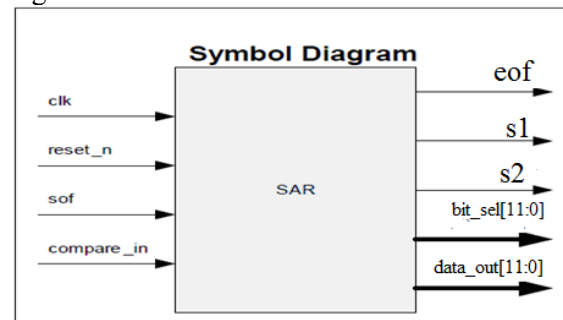


Fig-3. Symbol of SAR logic block

All the flip-flops in this module will be reset asynchronously when $reset_n$ is active, the entire module works on the positive edge of clock(clk). In reset deactivate condition, the module monitors Start of Function (SOF) signal. On detecting the transition on SOF signal from low to high, the conversion process starts and continues for 14 cycles. During the conversion phase, depending on the output of the comparator, for every clock cycle of comparison (from 2nd to 13th) a 12-bit register (Digital Output) is updated. At the end of 14th cycle, an End of Function (EOF) signal is set, and the 12-bit register values are latched on to the $data_out<11 : 0>$ (output) bus. During the next clock cycle (15th cycle), the **SOF** and **EOF** signals are reset. The logic output of SAR is interfaced with the DAC input using buffer modules and to transfer the SAR output to the output pins of ADC module.

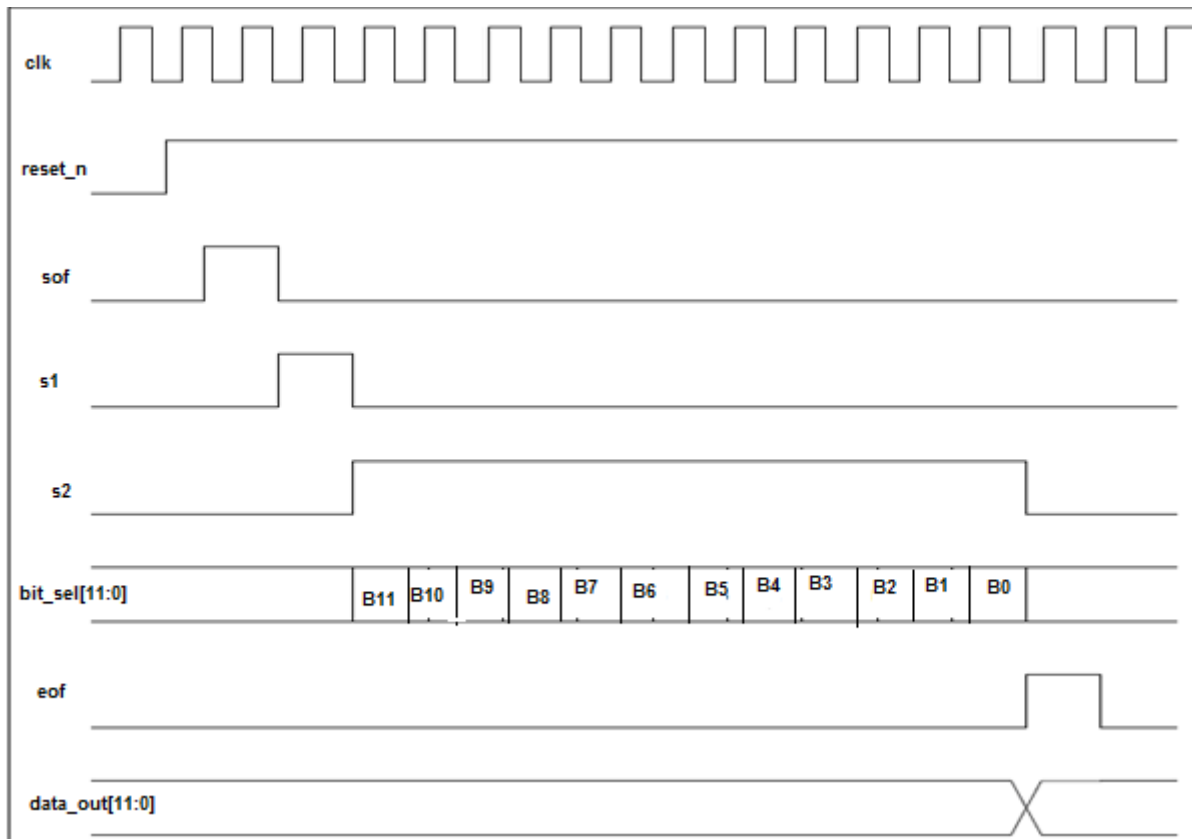


Fig-4. Timing diagram used for SAR logic

All the flip-flops in this module will be reset asynchronously when *reset_n* is active. The entire module works on the positive edge of clock *clk*. The timing diagram determined to design the SAR logic block is shown in Figure 4. In reset deactivate condition, the module monitors *sof* signal, the conversion process starts on detecting the transition on *sof* signal from low to high. The input of the SAR logic is the output of the comparator which generates *Vcmp* out as in Eq. (6),

$$V_{cmp}(\text{compare_in}) = \begin{cases} 0, & V_{dac} < V_{in} \\ 1, & V_{dac} \geq V_{in} \end{cases} \dots(6)$$

Considering the output of comparator (*compare_in*), the conversion logic is as follows:

- 1st clock cycle: The *s1* signal is set to 1 and *bit_sel[11 : 0]* is set to 0×00
- 2nd clock cycle: The *s1* signal is cleared, *s2* signal is set to 1 and set *bit_sel[11]* to 1 if *compare_in* is 1
- 3rd clock cycle: Retain the *bit_sel[11]* as 1 if *compare_in* is 0, else clear *bit_sel[11]* and set *bit_sel[10]* to 1
- and this process is continued upto 14th cycle

- 14th clock cycle: Retain the *bit_sel[0]* as 1 if *compare_in* is 0, else clear *bit_sel[6]*, clear signal *s2*, set signal *eof* and register the *bit_sel[11:0]* into ADC output *data_out[11 : 0]*
- 15th clock cycle: Clear *eof* and monitor of *sof* and start from 1st cycle.

The current bias for ADC design required are $1i$, $2i$, $4i$, $8i$ and $16i$ units that need to be derived from the current references. The reference current is designed using current mirrors from which all other current bias is derived. To produce the desired output current, the current source transistor and its cascaded neighbour needs to be biased and is designed using current mirrors.

5.1 Power estimation

The total power consumption can be estimated as given in equation (7).

$$P_{total} = \text{total number of current cells} * I_{ref} * V_{dd} \dots(7)$$

In this design, V_{dd} of 1.8 V is selected and therefore, it is necessary to minimize the total current in the design to reduce the total power consumption. There are three building blocks in ADC with DAC requiring higher current references. Comparator and SAR logic is set to operate at maximum current of $50 \mu A$ and DAC is set to operate at maximum of $100 \mu A$, the

total current required by the ADC is 200 μ A. For analysis of transistor matching Pelgrom's paper [19] has become the standard source and his formula for the standard deviation of saturation current for identically sized devices was used for the design. Mismatch causes time independent random variations in physical quantities of identically designed devices, which means each current source in the matrix generates a current that varies slightly from the desired current I_{ref} . To see that random variations do not degrade the performance of the circuit below its specifications, the current sources have to be designed. The formulas are given in equations (8) and (9).

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_{TO})}{(V_{GS} - V_{TO})^2} + \frac{\sigma^2(\beta)}{\beta^2} \dots\dots(8)$$

$$\text{where } \sigma^2(V_{TO}) = \frac{A_{VTO}^2}{WL} \text{ and } \frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} \dots\dots(9)$$

The dependant area parameters are A_{VTO} and A_β . Note that variation with spacing is neglected. The expressions for W^2 and L^2 are

derived from equations (8) and (9). W^2 and L^2 are used to design the width and length of the transistors of the biasing circuit.

$$W^2 = \frac{2I_{LSB}}{\mu * Cox * \left(\frac{\sigma I}{I}\right)^2} \left(\frac{A^2\beta}{(V_{GS} - V_T)^2} + \frac{4A_{VT}^2}{(V_{GS} - V_T)^2} \right) \dots(10)$$

$$L^2 = \frac{\mu * Cox}{2I_{LSB} * \left(\frac{\sigma I}{I}\right)^2} \left(A_\beta^2 * (V_{GS} - V_T)^2 + 4A_{VT}^2 \right) \dots(11)$$

5.2 DAC Design

In this work a new architecture for Digital to Analog (DAC) is proposed, designed, modelled and evaluated for its performance [20]. The proposed 12-bit DAC block diagram is shown in Figure 5. The DAC structure is split into two groups of 6-bits. The first stage generates V_{out1} corresponding to 6 MSBs and the second stage generates V_{out2} for 6 LSBs. The output of two-stage DAC V_{out1} and V_{out2} are accumulated in the adder circuit to generate the final analog output V_{OUT} .

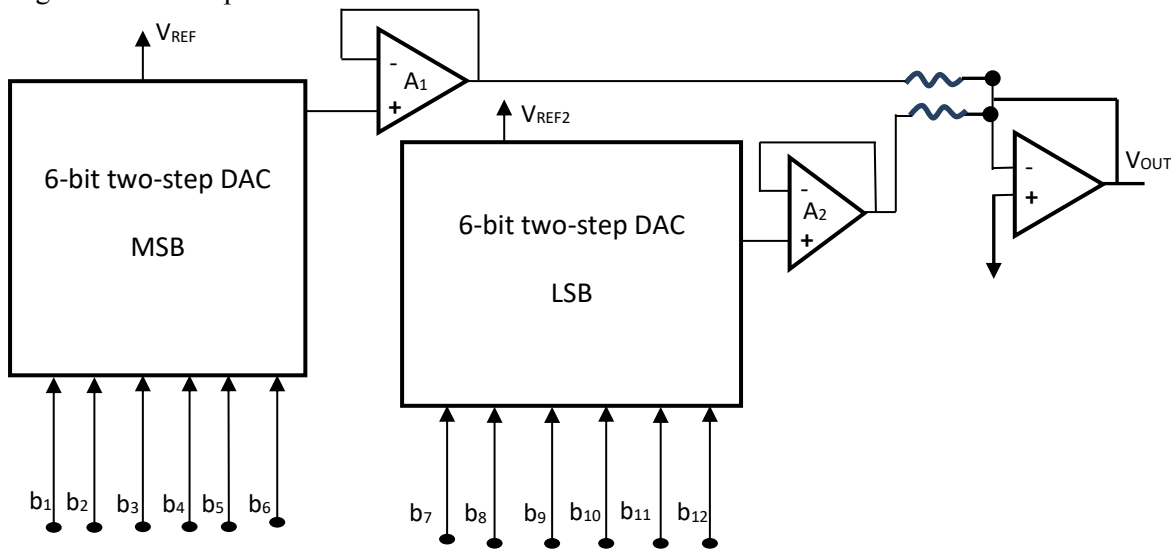


Fig-5. Proposed 12-bit DAC structure[20]

The 12-bit DAC is designed using two stages of 6-bit DAC [20]. Each of the 6-bit DAC consists of two step voltage divider type DAC and folded resistive string network. Device mismatches and area optimization is achieved with folded resistive string approach. Also, improvement in resolution is achieved with coarse and fine voltage generation logic from the two step voltage divider method. Schematic capture is carried out using Cadence tool. From the simulation studies, it is observed that the designed DAC has a maximum operating Bandwidth of 100 MHz and the gain at 3 dB is

41.86 dB. The power dissipation of designed DAC has been calculated at 4.33 mW and hence suitable for high speed ADC. The INL and DNL of the DAC design has been calculated as +0.034 V to -0.001 V and +0.06 V to -0.05 V. The performance is accomplished with a design area of 450 μ m².

5.3 Comparator design

Comparator which is another sub block of SAR ADC circuits is designed using Operation Transconductance Amplifier (OTA) [18]. The OTA circuit is realized using eleven transistors

as shown in Figure6. The transistors F1 and F2 are the differential pair and forms the transconductance cell that converts the input voltage V_{in}^+ and V_{in}^- (differential input voltages) to current. The differential current output (I_{out}) of the differential pair is converted to single ended current at the output by using the current mirrors F3 to F8, F10 and F11. F9 transistor is used to bias the differential pair and is used as current sink circuit. The cut-off frequency of the OTA is decided by setting the appropriate bias current and the load capacitance of the OTA. The transconductance gain g_m of the OTA is controlled by setting the current that enters the transistor F9 and the gate voltage V_b is appropriately set. Design of OTA is primarily identifying the transistor geometries such that the simulation results are matching the hand calculations. Design methodology based on g_m/I_D method is the most popular approach that identifies the transistor geometries based on data sheets and simulation results. In this method of design of OTA circuits based on datasheet several design variables that were required for the design were assumed without clear rules. The design specifications meeting input range, common mode rejection and noise parameters were not considered in this approach. Even the channel length variations with regard to g_m/I_D were not considered in the design process.

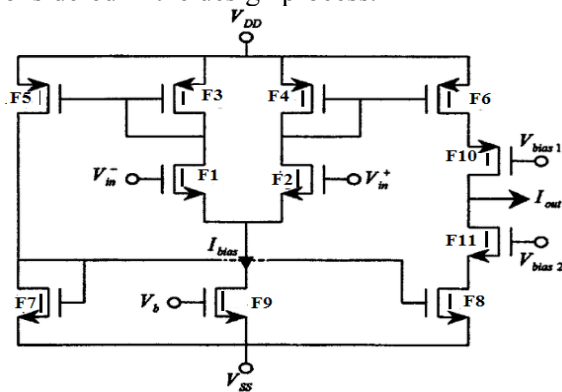


Fig-6. OTA based comparator

The OTA is designed using FinFET transistors and the comparator circuit is designed integrating the sub circuits with OTA. The building blocks of the comparator design such as input level shifter, differential pair with cascode stage and class AB amplifier for output swing are designed and integrated. The gain of the comparator is 103dB, with phase margin of 65° , CMRR of 76 dB and output swing from rail to rail of 0 to 1.8 V is achieved. The circuit provides unity gain bandwidth of 5 GHz and DC Open Loop voltage gain of 90 dB.

6. Implementation

The SAR ADC primarily consists of 3 main blocks. SAR Logic Block, a resistive string folded segmented DAC and OTA based Comparator with Offset- Cancellation feature.

6.1 The SAR Logic Block Implementation

SAR logic design is presented in terms of Finite State Machine (FSM) and is illustrated for its logic function as in Table 3. Each conversion requires 14 clock cycles with the first clock being reset mode and in this mode all outputs are set to zero. From the 1st clock to 13th clock data is converted sequentially and the SAR output is generated. In the 14th clock cycle the data generated is stored in the output register for conversion to analog data by the DAC circuit.

Table-3. SAR logic conversion table using FSM

Cycle	Sample	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Comp.
0	1	0	0	0	0	0	0	0	0	0	0	0	0	-
1	0	1	0	0	0	0	0	0	0	0	0	0	0	a11
2	0	a11	1	0	0	0	0	0	0	0	0	0	0	a10
3	0	a11	a10	1	0	0	0	0	0	0	0	0	0	a9
4	0	a11	a10	a9	1	0	0	0	0	0	0	0	0	a8
5	0	a11	a10	a9	a8	1	0	0	0	0	0	0	0	a7
6	0	a11	a10	a9	a8	a7	1	0	0	0	0	0	0	a6
7	0	a11	a10	a9	a8	a7	a6	1	0	0	0	0	0	a5
8	0	a11	a10	a9	a8	a7	a6	a5	1	0	0	0	0	a4
9	0	a11	a10	a9	a8	a7	a6	a5	a4	1	0	0	0	a3
10	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	1	0	0	a2
11	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	1	0	a1
12	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	0	a0
13	0	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1	a0	-

Figure 7 presents the SAR logic circuit diagram using D-flip flops. The SAR logic is realized using ring counter and a code register. In the first clock i.e., clock zero all the outputs of D-

flip flop are reset to zero. In the first clock the MSB bit is set to logic '1' and this logic data is shifted through the shift registers.

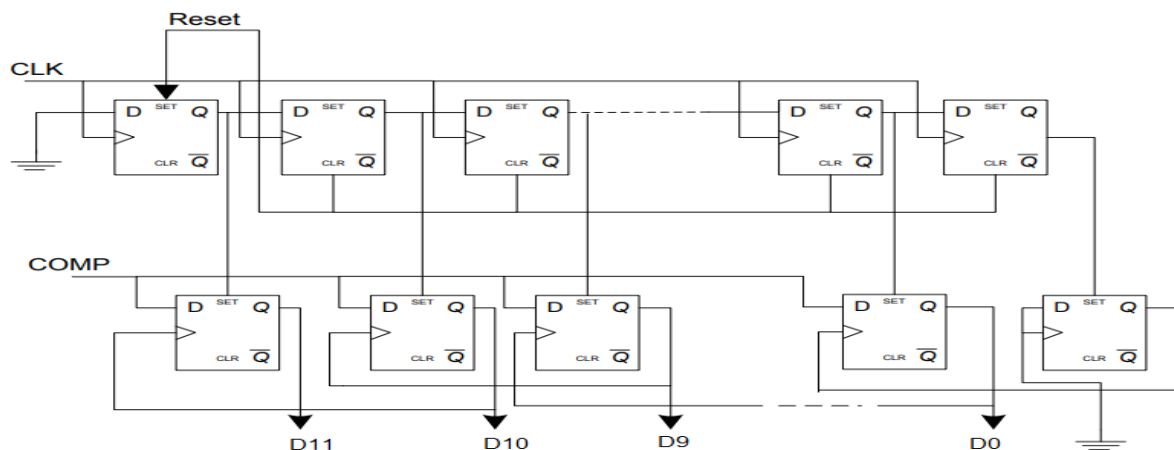


Fig-7. SAR logic realized using ring counter and code register

The Verilog code is developed for SAR logic and is verified for its functionality in Cadence environment and the verified code is synthesized to generate the netlist. The netlist is imported into Virtuoso schematic environment and is integrated with analog block of ADC structure.

6.2 DAC Implementation

The Digital to Analog (DAC) converter is basically Current-Steering Mode - Segmented architecture. The current sources are designed as $1i$, $2i$, $4i$, $8i$ and $31*16i$. The virtuoso schematic is as shown in Figure 8.

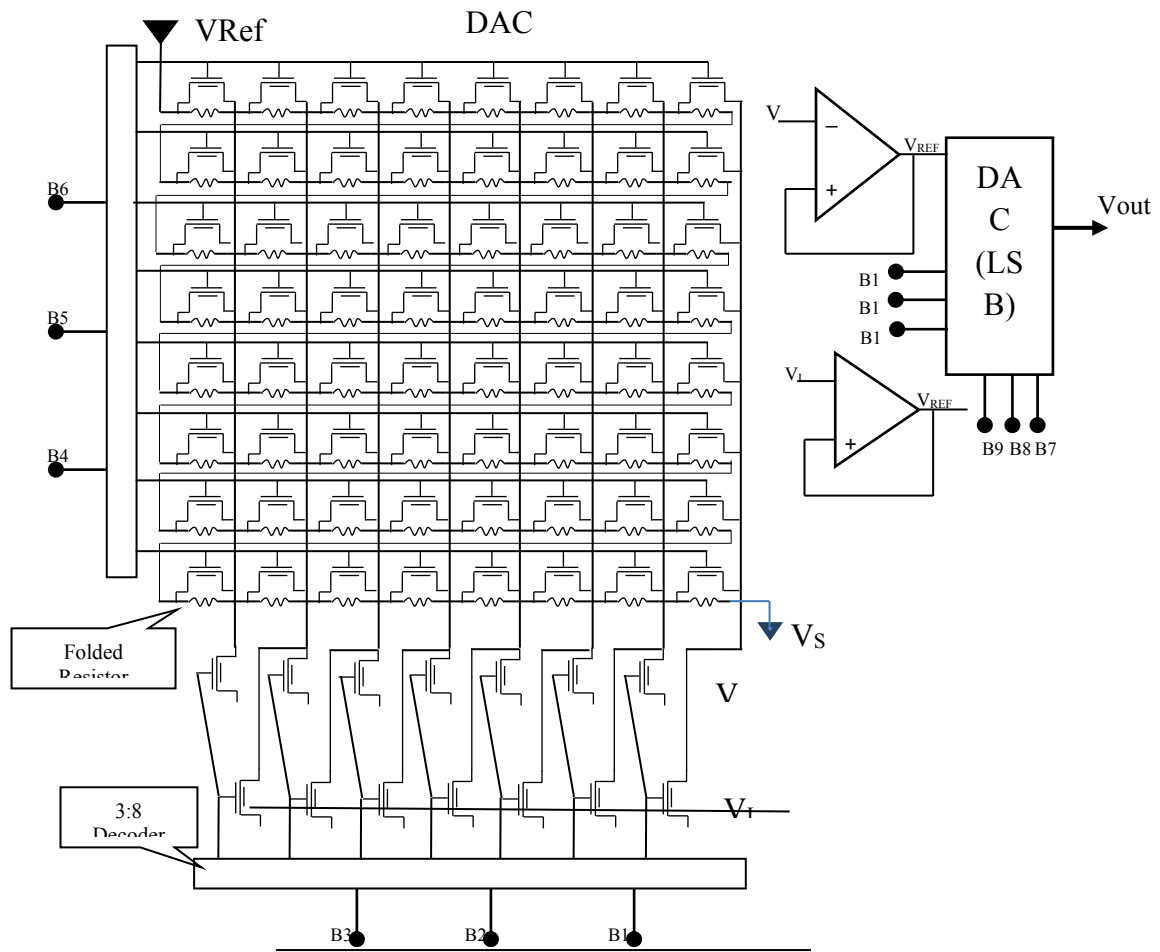


Fig-8. Virtuoso opus schematic of DAC block

The designed 12-bit DAC has to work according to its functionality. Once the netlist of spice is generated the simulations results are produced using ELDO, then add all the required input voltages such as input bits and bias voltage. The input reference currents were also provided. The power supply is given as 1.8V.

Comparator schematic captured in Virtuoso is presented in Figure 9. The OTA circuit is presented in Figure 9(a) and Figure 9(b) presents the OTA used as comparator. The simulation of the comparator was done with a test case where a PWL signal was provided as the Analog input to the comparator. The circuit is operated at 1.8V and 1 GHz clock frequency.

6.3 OTA Based Comparator Implementation

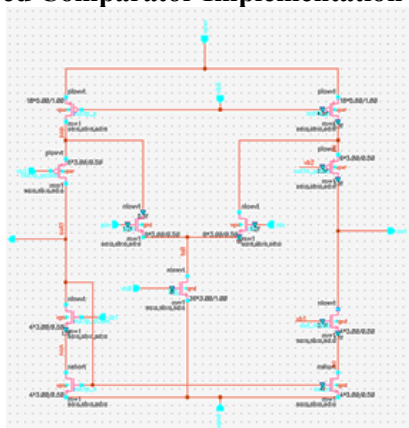


Fig. 9 Comparator schematic
Fig-9(a).OTA sub circuit

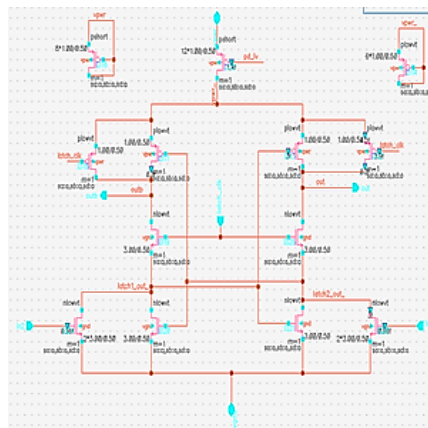


Fig-9(b). OTA as comparator

7. Results & Discussion

Figure 10 presents the simulation result of SAR ADC where it shows 6-bit (MSB) digital output such as B12, B11, B10, B9, B8, B7 along with its analog input (analog_in) and DAC output (DAC Out). An input signal of frequency of 100 MHz is considered in this test case and the amplitude of the signal is set between 0 to 2 V.

12-bit ADC operating at sampling frequency of 1 GHz, the 6 LSB bits will have very fast switching process and hence MSB bits are captured and presented for verification. An input signal of 10 kHz is considered as input and the voltage level is between 0 to 2 V is sampled at 100 MHz. The digital output of ADC is captured considering the 6 LSB bits to check for logic correctness of the ADC.

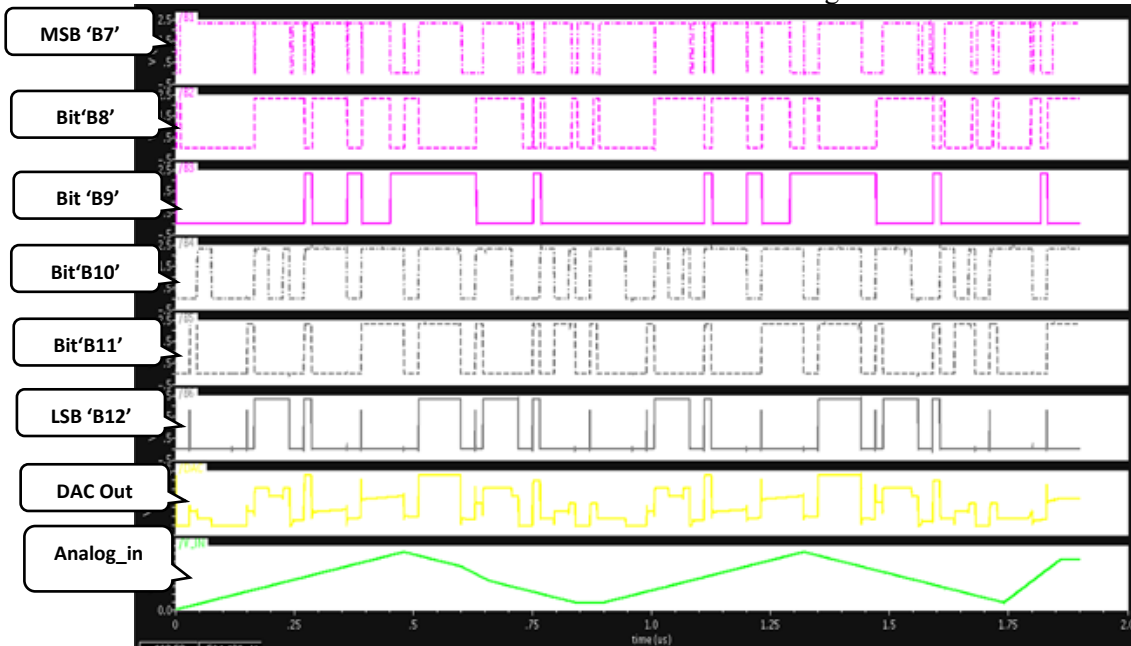


Fig-10. Simulation result of SAR ADC (LSB 6-bits)

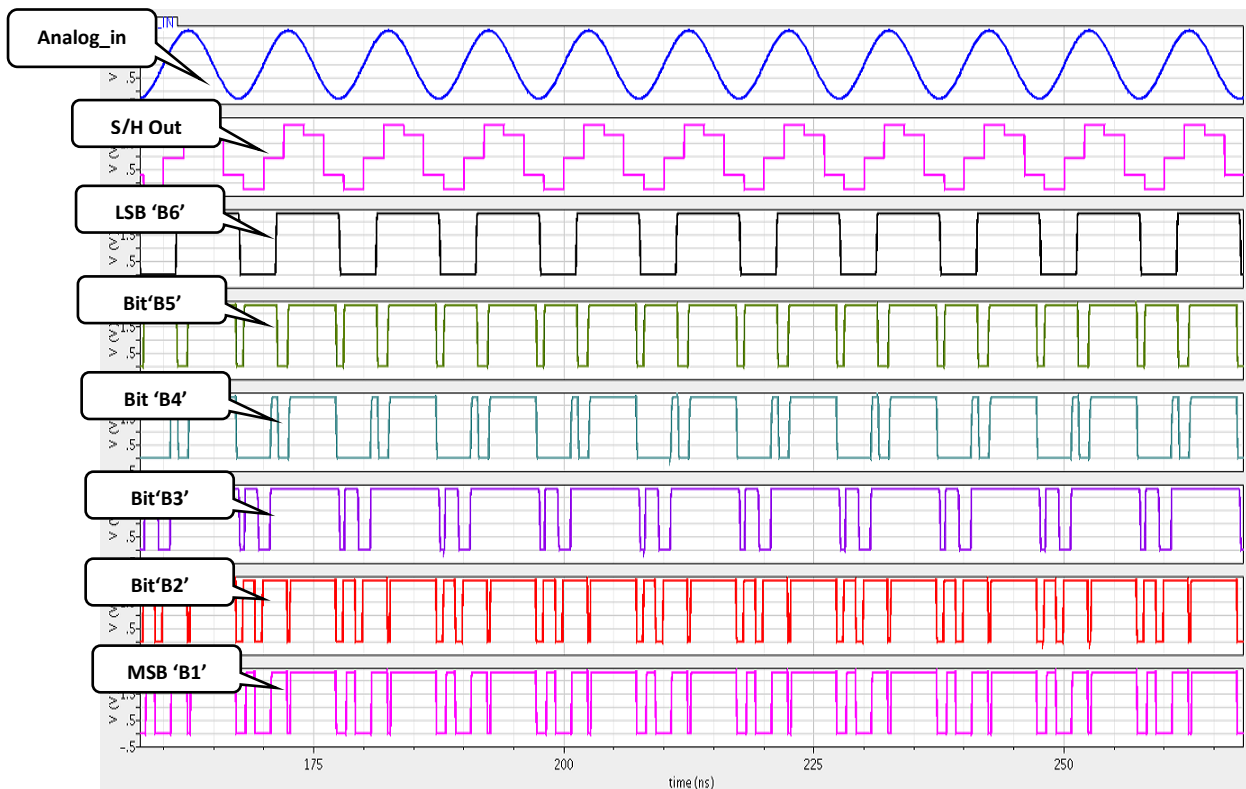


Fig-11. Simulation results of SAR ADC (MSB 6-bits)

Figure 11 illustrates about the simulation result of SAR ADC 6-bit (LSB) where the results obtained for analog input (analog_in), digital to analog converter output (DAC Out), and digital output bits such as B6, B5, B4, B3, B2, B1. From this simulation result, it is observed that the output of all the digital bits has been high when analog input voltage is equal to its reference voltage or equal to V_{DD} voltage. The power dissipation simulations were done on the extracted layout net list including parasitic resistance and capacitance of the

power buses, nets used for signal routing using ELDO simulator. The power supply is 1.8V. Figure 12 illustrates the active current across multiple cycles. The power dissipation results are inclusive of SAR Logic block. The maximum switching current is captured from the SAR logic switching states and it is observed that the maximum switching current of 0.1806 mA occurs whenever the MSB bits is activated. Considering the maximum switching current, the average power dissipation is computed.

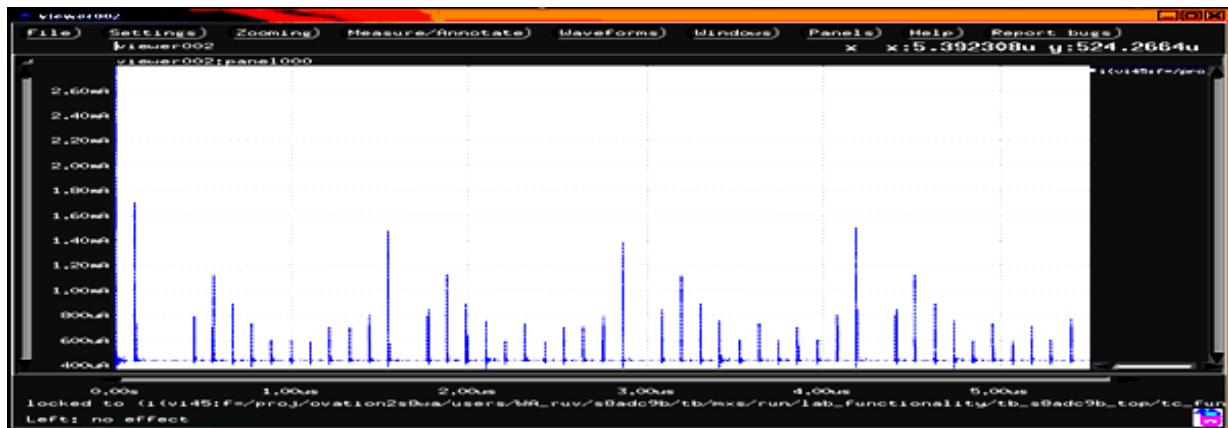


Fig-12.Active current plots of ADC

7.1 ADC metrics

Input signal with maximum frequency of 100 MHz is sampled at 1 GHz sampling frequency with amplitude of 2 V. The input signal is added with random noise and multiple harmonics that occur in the band 10-40 kHz, 10-40 MHz and

70-100 MHz. The noise power is also varied to estimate the ADC metrics. Figure 13 presents the input data with noise and harmonics. Figure 14 presents the FFT spectrum of input data with noise and harmonics.

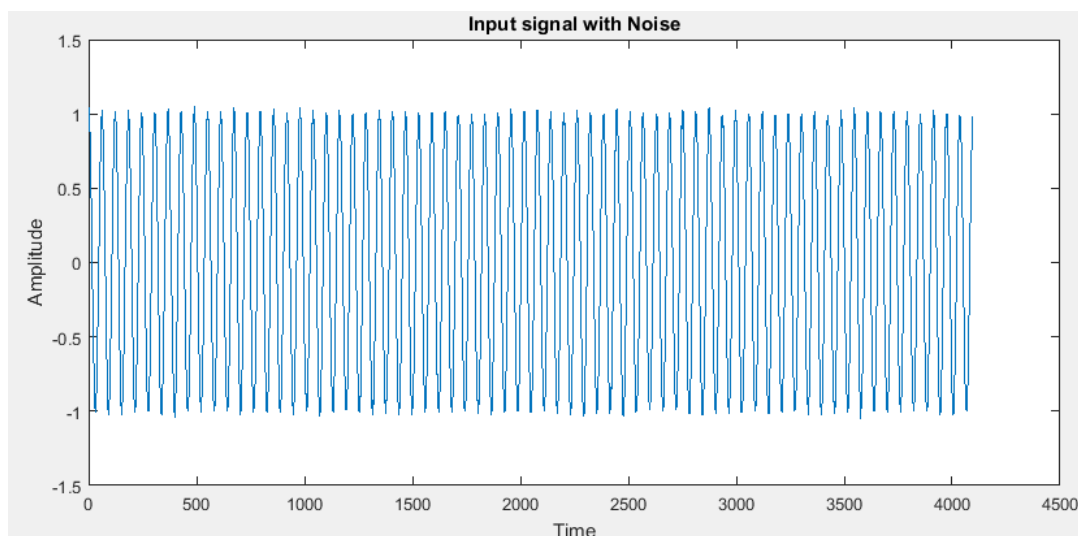


Fig-13. Input data with 20dB noise and with 3rd order harmonics

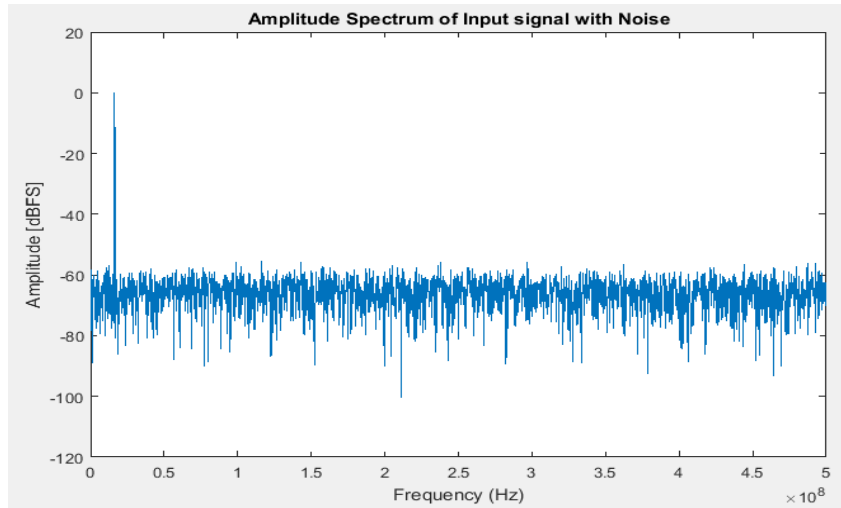


Fig-14. Frequency spectrum of input data

The ADC schematic is simulated in Virtuoso environment and the corresponding outputs are imported into MATLAB environment to compute ADC metrics such as ENOB, SNDR, SFDR and SNR. Figure 15 presents the ADC metrics plot for input signal of 1.2V with higher

noise power defined in the range of 40 to 50 dB. The ADC metrics are ENOB = 4.8449, SNDR = 30.9261, SFDR = 55.6228, SNR = 30.9261.

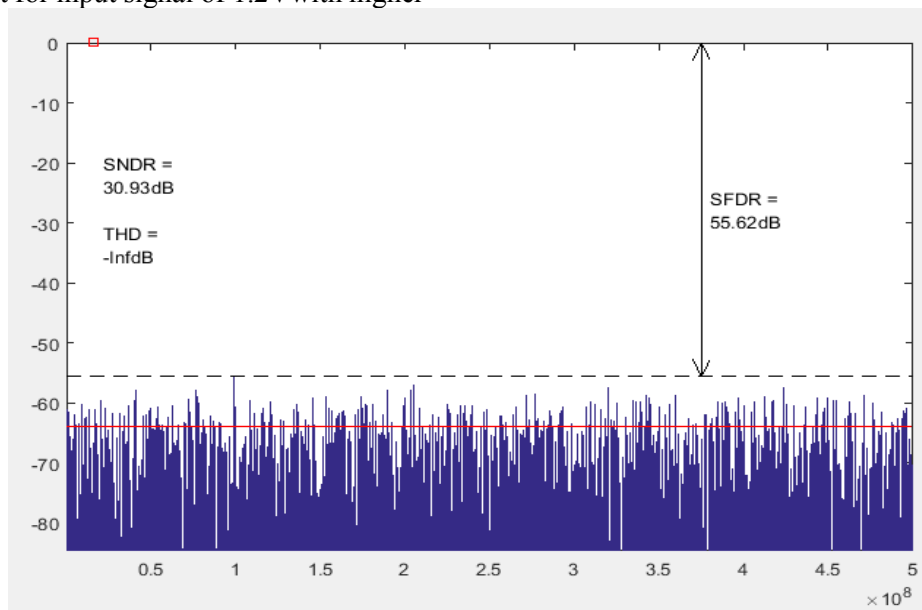


Fig-15. ADC metrics with noise power in 40 – 50 dB harmonics in 10 kHz to 40 kHz

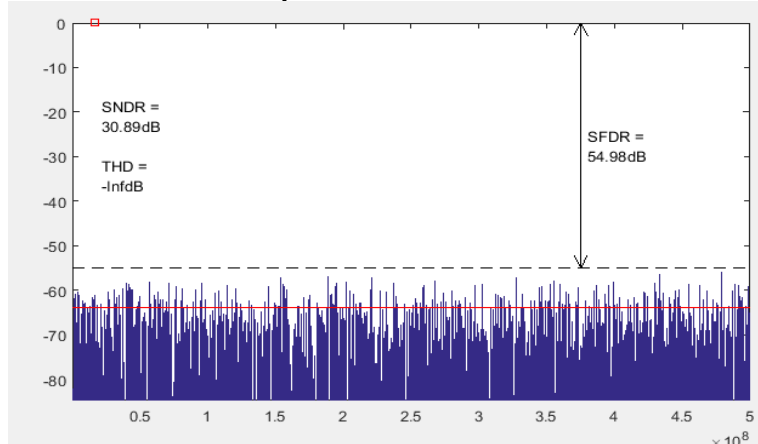


Fig.-16. ADC metrics with noise power in 40 – 50 dB harmonics in 10 MHz to 40 MHz

The frequency spectrum depicting ADC metrics is presented in Figure 16. ADC metrics are ENOB = 4.8392, SNDR = 30.8923, SFDR

= 54.9778, SNR = 30.8923 for noise power in 40-50 dB and harmonics in 10 MHz – 40 MHz range.

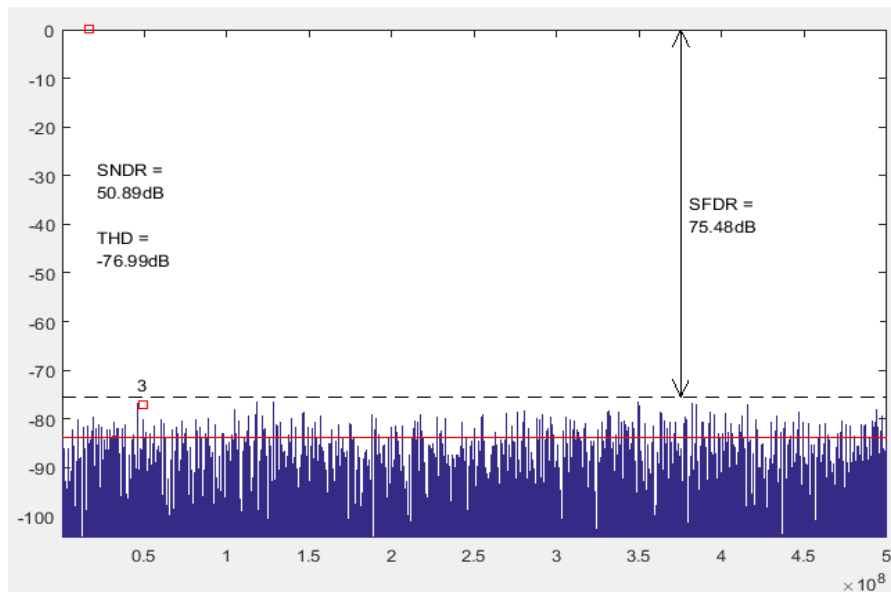


Fig. 17 ADC metrics with noise power in 10 – 20 dB harmonics in 10 MHz to 40 MHz

The frequency spectrum depicting ADC Metrics is presented in Figure 17 for noise power in 10-20dB and harmonics in 10 MHz to

40 MHz range. ADC Metrics are ENOB = 8.1610, SNDR=50.8893, SFDR = 75.4777 and SNR = 50.8999.

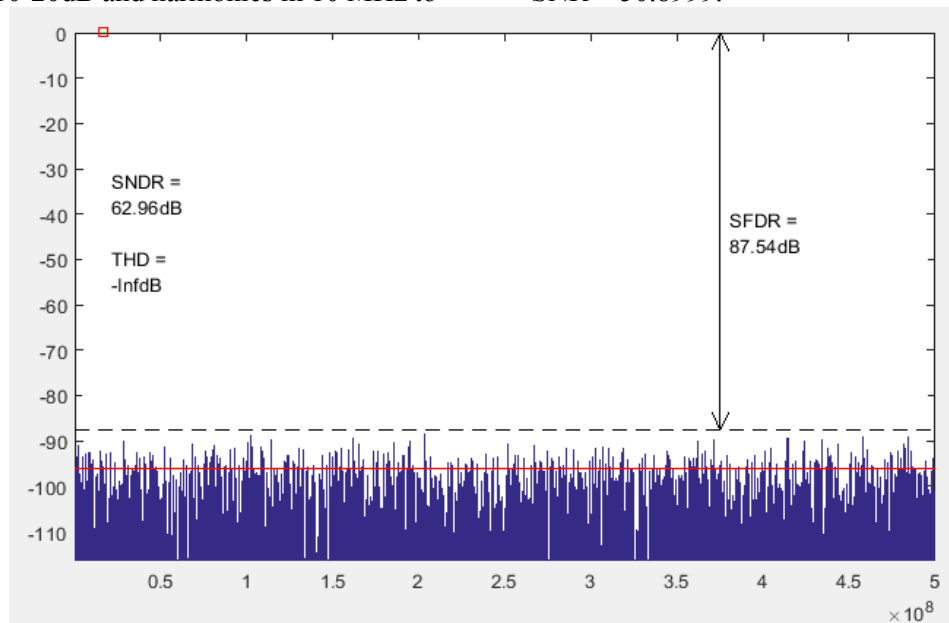


Fig. 18 ADC metrics with noise power in 10-20 dB harmonics in 70 MHz to 100 MHz

The frequency spectrum depicting ADC metrics with noise power in 10 dB, harmonics in 70 MHz to 100 MHz is presented in Figure 18. ADC metrics are ENOB=10.1663, SNDR=62.96 dB, SFDR = 87.54 dB and SNR=62.9613 dB. It is observed from the measurement results that the change in

harmonics intensity for the ADC operating at 70MHz to 100MHz band width resulted in improvement in ENOB, SNDR and SNR. The highest INL error measured is +1.22/-0.69 LSB. Figure 19 presents the DNL and INL measurements for 12-bit ADC.

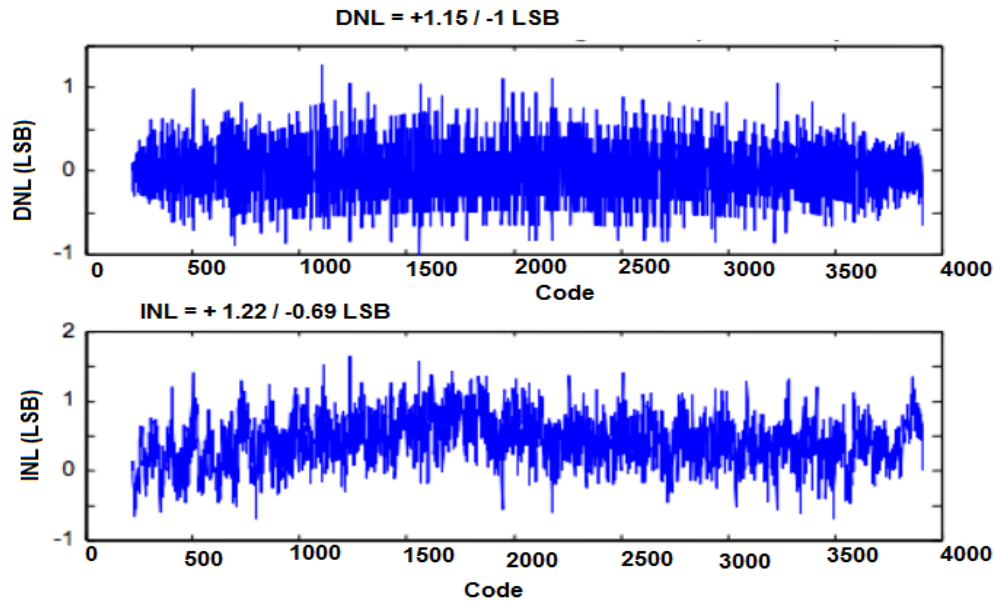


Fig-19. DNL and INL measurements for 12-bit ADC

Table 4-Comparison table

Parameters	Existing Design[16]	Proposed Design performance parameter and its values
Resolution	12-bits	12-bits
Technology	40 nm	22nm
Clock frequency	200 MHz	1 GHz
Power Supply	1.2 V	1.8 V
Operating Current	15 mA	1 mA
Input voltage range	-	0.2 V-1.4 V
Power Dissipation	8 mW	7 mW
INL	1 LSB/-1.2 LSB	+1.22/-0.69 LSB
DNL	0.7 LSB/-0.3 LSB	+1.15/-1LSB
SNR (dB)	-	62.9613
SNDR (dB)	-	62.96
SFDR (dB)	67.9	87.54
ENOB	9.85	10.1663
Novelty in Proposed Design	-	OTA Comparator Two Step DAC

8. Conclusion

This work involved in designing a FinFET based 12-bit SAR ADC for suitable for high speed and low power applications. The design consists of sub blocks like DAC, comparator, SAR logic. The OTA based comparator is designed to achieve gain of 100 dB with phase margin of 65° and UGB of 5 GHz. DAC circuit designed using two stage folded resistive structure which can operate at maximum frequency of 10 GHz with power dissipation of less than 4 mW. Also, DAC performs the conversion of data with minimum noise measured considering INL and DNL of +0.034

V to -0.001 V and +0.06 V to -0.05 V respectively. Thermometric decoder and shift registers based SAR logic is used along with and FSM based approach which reduces glitch in the SAR output. The sub blocks are integrated to achieve SAR ADC and its performance is analysed considering noise sources and harmonics. From the results obtained the ADC structure is able to work at 1GSps with effective conversion metrics suitable for high speed and low power applications.

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