Implementation of Neural network based I cos ϕ Controller for DSTATCOM in Three Phase Four Wire Distribution System under Varying Source and Load Conditions for Power Quality Improvement

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Abstract: - The application of power semiconductor devices in the area of power electronics and power system are the key factors which kindle the power quality problems particularly the harmonics, burden of reactive power and neutral current due to unbalance. The above citied power quality problems are predominant due to wide usage of 1-ϕ / 3-ϕ , linear and nonlinear loads which are fed from three phase four wire (3P4W) distribution system. The performance of the 3P4W distribution system can be enriched by mitigating the above mentioned problems with proper selection of a power quality compensator and control strategy. In this paper, DSTATCOM is chosen as power quality compensator which comprises of a three phase three leg Voltage source converter (VSC), a single phase active power filter (APF) and a DC bus capacitor. The proposed neural network based control strategy generates the reference supply current, so as to make the source supply only the real fundamental load current component (I cos ϕ, in which "I" refers the fundamental load current magnitude and cos ϕ refers the load displacement power factor). The DSTATCOM with neural network based control strategy mitigates harmonics, compensates reactive part of load current, ensures balanced and sinusoidal source current from the supply mains that are nearly in phase with the supply voltage even though there is an unbalance in the three phase load currents and source voltage conditions, compensates neutral current even under unbalanced linear and non-linear load conditions in 3P4W distribution systems. Artificial Neural Network (ANN) controller is also executed to keep up the voltage of the capacitor at the reference value under varying load and source conditions. The DSTATCOM performance is validated under unbalanced, linear/nonlinear loads for all possible conditions of the source like balanced, unbalanced, balanced/distorted and unbalanced/distorted source voltage conditions. The propounded neural network based control algorithm for DSTATCOM presented in this paper is simulated using MATLAB software. The simulation results prove the efficacy of the proposed neural network based control strategy under varying source and load conditions.

Key-Words: - Neural network, DSTATCOM, Neutral current mitigation, Three phase four wire distribution system, unbalanced and/or distorted source, Power quality.

1 Introduction

The proliferation use of various types of 1-ϕ/3-ϕ, linear and non-linear loads like rectifier, inverters, choppers, solid state controllers etc., create several power quality issues such as burden of reactive power, distorted current and voltage waveforms which have high harmonic content[1-4]. Most of the commercial, official, residential, and IT industry buildings are operated on 3P4W system which are unbalanced linear and non-linear load conditions. These loads are the cause for the enormous flow of neutral current having both fundamental and harmonic currents that create overload on neutral conductor. This makes the distribution system to have low power factor, poor voltage regulation, malfunctioning of consumer equipment, overheating of conductor, and thereby reduces the efficiency of the system with deterioration in the life of the equipment [5-12].The customer power device (CPDs) is a generic name used to denote a group of devices that are employed for the mitigation of the power quality problems in the distribution system [3]. The series connection of CPD with the load is termed as Dynamic voltage restorer (DVR) which is used to solve and suppress the problems related to source voltage. The DSTATCOM is a CPD which is connected across the load to solve and suppress the problems related to current by operating in current control mode. The power quality problems related to both voltage and current are solved by Unified Power Quality Conditioner (UPQC) which is the combination of both DVR and DSTATCOM [13]. In literature survey, it is reported that different topologies of DSTATCOM are under investigation for the compensation of neutral current in 3P4W distribution system along with mitigation of power quality problems related to source current they are i) 4legVSC ii) 3 single phase VSC iii) 3 leg VSC with split capacitor iv) 3 leg VSC with any of the transformer connections like T-connection, zig-zag, hexagonal and star-delta transformers [14, 15]. Even though these transformers mitigate neutral current effectively, the efficacy depends upon its impedance, transformer position and the condition of source voltage. Most of the researchers prefer the four leg VSC topology as a better option for the mitigation of neutral current compared to other methodologies, even though the control strategy is complex with more number of switching devices [16-30].

The DSTATCOM performance relies on the control strategy implemented for the generation of reference current. The selection of control strategy is based on the accuracy and filter response time with minimal number of calculation steps [31]. In order to fulfil this requirement many control strategies are developed and proposed by various researchers. They are instantaneous reactive power theory (IRP) [12, 32], power balance theory [33], synchronous reference frame theory (SRF) [16] etc. In the mitigation of harmonics in 3P4W system under unbalanced and/or distorted voltage source condition, the IRP theory control strategy is inaccurate in calculating the load harmonic currents and reference supply currents [25,32], SRF theory requires separate control strategy for UPF (unity power factor) and ZVR (zero voltage regulation) operations [24]. However the proposed neural network based I cosϕ algorithm is considered superior than all other control strategies for 3P4W system, due to reduced computational steps in making the source to supply only the real fundamental load current component with more accuracy.

To accomplish the function of power quality compensator, a novel neural network based control algorithm for 3P4W DSTATCOM is proposed in this paper. MOSFET based four limb VSC with a DC capacitor is the topology implemented for DSTATCOM where the fourth limb is used to mitigate excessive neutral current with separate neural network control strategy. The proposed neural network based I cosϕ control approach is implemented for the estimation of reference current which is utilized for the generation of gate pulse for the DSTATCOM and makes the source to supply only the real part of the fundamental load current under all possible utility voltage source conditions. Separate ANN controllers are also proposed to mitigate the neutral current under unbalanced load conditions and to regulate the voltage of DC bus capacitor under varying source and load conditions. The following are the features of ANN based control strategy of DSTATCOM:

i) Balanced and sinusoidal source current from the supply mains that are nearly in phase with the supply voltage, even under unbalanced linear and non-linear load conditions.

ii) Reduction in the %THD of source current in 3P4W distribution system thus making the source current sinusoidal even under varying source and load conditions.

iii) Compensation of reactive power.

iv)Regulation of DC bus capacitor voltage under varying load and source conditions.

v) Recompense of neutral current under unbalanced load conditions.

2 System configuration of DSTATCOM

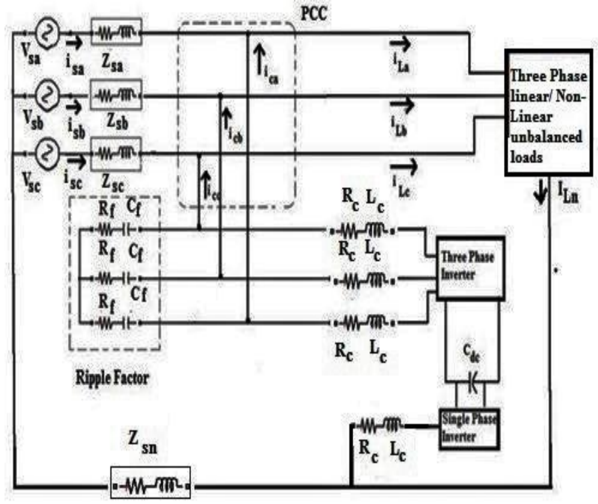


Fig.1. Schematic power circuit diagram of 3P3W DSTATCOM and single phase inverter connected to 3P4W distribution system.

Fig.1 depicts the power circuit diagram of a DSTATCOM with three phase three leg MOSFET based VSC and single phase inverter with a DC capacitor performing as energy buffer, connected to the 3P4W distribution network. Realization of 3P4W wire supply system is made by star connection of 3ϕ voltage source with a neutral point. The impedance of the three phase lines are represented as Zsa, Zsb, Zsc and Zsn corresponds to the impedance of the neutral conductor. R_c and L_c

corresponds to the coupling resistor and inductor of the DSTATCOM. In the schematic diagram, 3P4W DSTATCOM, ripple filter and different types of loads are shunted at the point of common coupling [PCC] [24, 32]. The DSTATCOM with four leg VSC fired by appropriate gating pulses generates compensating currents and injects into the distribution system. Therefore the DSTATCOM makes the source to supply only active part of load current, ensuring reduction in the % THD of source current, compensating reactive part of the load current, ensuring balanced and sinusoidal source current from the supply mains even under unbalance in the three phase load currents, performing voltage regulation during varying load and source conditions[25]. Hysteresis based current control method is proposed for the generation of gate pulses. The mitigation of neutral current under unbalanced load conditions is accomplished by the fourth limb of DSTATCOM. The switching transients and ripples present in the PCC are filtered out by series connection of capacitor C_f and resistor R_f.

3 Proposed control strategy of DSTATCOM

The proposed control algorithm is simple to implement in practical applications and involves minimum number of computational steps even when the supply voltage is distorted and/or unbalanced with unbalanced non-linear loads. The extraction of harmonic and reactive currents are deduced by sensing the source voltages (V_{sa},V_{sb},V_{sc}), the DC bus capacitor voltage and load currents (I_{La},I_{Lb},I_{Lc}) of the DSTATCOM. Consecutively Neural network based control algorithm is implemented for the extraction of reference currents in 3P3W DSTATCOM. Three different ANN controllers are proposed in this algorithm to serve the following purposes.

i) To extract the magnitude of fundamental current and to introduce a shift in phase by + 90°.

ii) To extract the fundamental component of phase voltage under distorted and/or unbalanced source voltage conditions.

iii) To extract the power loss in the inverter and interfacing inductor, thereby keep up the DC bus capacitor voltage to its reference value by compensating the power loss.

The proposed neural network control strategy makes the source current and supply side voltage waveforms nearly sinusoidal under any electrical disturbances. The block diagram depicted in Fig.2 is the model of proposed neural network control scheme. The following are the steps involved in the control strategy of DSTATCOM:

i) Application of ANN controllers for the generation of reference source current signal by maintaining the DC voltage across capacitor constant and implementation of hysteresis current control for the generation of gate pulses.

ii) Application of ANN controller for single phase APF for mitigation of neutral current under unbalanced load conditions.

3.1 Generation of reference current signals

The balanced three phase instantaneous source voltage can be expressed as

$$v_a = V_m sin\omega t$$
$$v_b = V_m \sin(\omega t - 120°)$$
$$v_c = V_m sin(\omega t + 120°) \quad (1)$$

Let us assume that the above mentioned balanced three – phase source is connected to an unbalanced 3P4W non-linear load. The harmonics and reactive component of unbalanced load current can be expressed as:

$$i_{La} = I_{La1}\sin(\omega t - \phi_a) + \sum_{n=2}^{\infty} I_{Lan}\sin(n\omega t - \phi_{an})$$
$$= Real(i_{La1}) + Imaginary(i_{La1}) + harmonic\ currents$$

$$i_{Lb} = I_{Lb1}\sin(\omega t - 120° - \phi_b) + \sum_{n=2}^{\infty} I_{Lbn}\sin(n(\omega t - 120°) - \phi_{bn})$$

$$= Real(i_{Lb1}) + Imaginary(i_{Lb1}) + harmonic\ currents$$

$$i_{Lc} = I_{Lc1}\sin(\omega t + 120° - \phi_c) + \sum_{n=2}^{\infty} I_{Lcn}\sin(n(\omega t + 120°) - \phi_{cn})$$

$$= Real(i_{Lc1}) + Imaginary(i_{Lc1}) + harmonic\ currents \quad (2)$$

Where

ϕ_a, ϕ_b, ϕ_c - fundamental source current phase angles for phases a,b,c.

$\phi_{an}, \phi_{bn}, \phi_{cn}$ – n^{th} harmonic current phase angles for phases a,b,c.

$I_{La1}, I_{Lb1}, I_{Lc1}$ - magnitudes of fundamental source current for phases a,b,c.

$I_{Lan}, I_{Lbn}, I_{Lcn}$ -magnitudes of nth harmonic currents for phases a,b,c.

For each phase the calculation of the magnitude of real part of fundamental load current is performed as follows

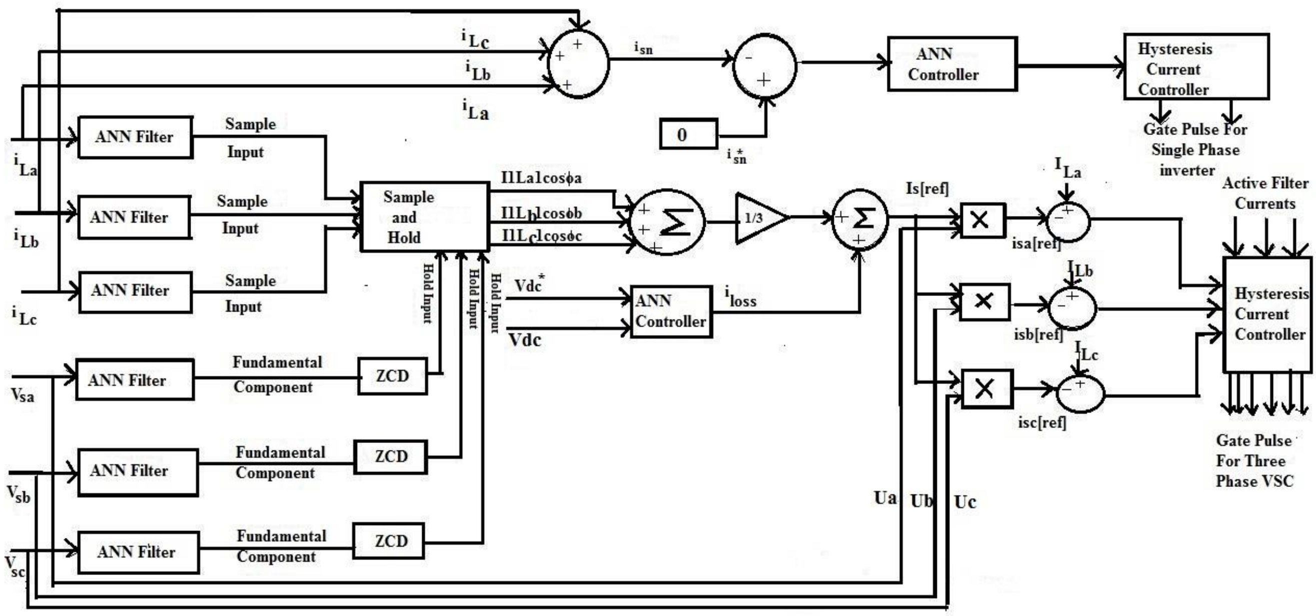


Fig.2 Block diagram of the neural network based I cos ϕ control scheme for DSTATCOM in 3P4W system.

$$|Real(I_{La1})| = |I_{La}|cos\phi_a$$
$$|Real(I_{Lb1})| = |I_{Lb}|cos\phi_b$$
$$|Real(I_{Lc1})| = |I_{Lc}|cos\phi_c \quad (3)$$

In the above equations, $|I_L|.cos\phi$ is the magnitude of the corresponding fundamental load current which depicts the real part of the fundamental load current. The $|I_L|.cos\phi$ is calculated by sensing the load current magnitude with a phase shift of +90° at the zero crossing point of the negative cycle of the phase voltage. In the conventional controller it is achieved by connecting a second – order low pass filter where the cut-off frequency is 50Hz which calculates the fundamental load current with an inherent phase shift of +90° [31]. In this paper the above mentioned calculation is performed by neural network block. An ANN filter is used to extract the fundamental component of phase voltage which is fed as input (I/P) to the Zero crossing detector (ZCD). The calculation of the zero crossing point of the negative cycle of the fundamental component of the phase voltage is performed by the ZCD. The output (O/P) pulse of the ZCD is fed as an (I/P) to the hold circuit. The phase shifted fundamental current is calculated using another ANN block and is fed as an I/P to sample circuit. The (O/P) of the sample and hold circuit is considered as the amplitude $|I_L|.cos\phi$ which is the real part of the fundamental load current.

The reference source current magnitudes of the three phases are calculated by finding out the average value of the amplitude of the real part of the fundamental load current.

$$|I_s\,(ref)| = \frac{|Real(I_{La1})| + |Real(I_{Lb1})| + |Real(I_{Lc1})|}{3}$$

$$= \frac{|I_{La}|cos\phi_a + |I_{Lb}|cos\phi_b + |I_{Lc}|cos\phi_c}{3} \quad (4)$$

In the MATLAB simulation the above mentioned equation is implemented by connecting a summer of gain 1/3.Equation (4) ensures balanced and sinusoidal source current from the supply mains that are nearly in phase with the supply voltage under all varying conditions of source and load.

The reference source current for three phases is calculated as follows:

$$i_{sa}\,(ref) = |I_s\,(ref)| \times U_a = |I_s\,(ref)|sin\omega t$$
$$i_{sb}\,(ref) = |I_s\,(ref)| \times U_b = |I_s\,(ref)|\sin(\omega t - 120°)$$
$$i_{sc}\,(ref) = |I_s\,(ref)| \times U_c = |I_s\,(ref)|\sin(\omega t + 120°) \quad (5)$$

In the above equations U_a, U_b, U_c are the templates which represent the phase voltage of three phases with unit magnitude.

$$U_a = 1\sin\omega t$$
$$U_b = 1\sin(\omega t - 120°)$$
$$U_c = 1\sin(\omega t + 120°) \quad (6)$$

For a balanced/pure sinusoidal waveform the 3-ϕ source voltages are considered as templates for generating sine waves with unit magnitude which are in phase with source voltages. If the 3ϕ source voltages are distorted/unbalanced, the fundamental component of the source voltage is deduced with the aid of an ANN block and the output of the ANN block is considered as template to generate unit amplitude sine wave. The extraction of variation of voltage in the DC capacitor gives the information about loss of power (p_{loss}) in the inverter and the coupling inductor. In order to keep the voltage across the capacitor constant and to meet out the power loss (p_{loss}) for each phase, the corresponding current component (i_{loss}) is deduced by an ANN controller and is summed to the real part of the fundamental load current component in each phase represented in equation (4).

The reference source current is compared with corresponding load current in order to calculate the reference compensation current and the equation is as follows:

$$i_a(comp) = i_{La} - i_{Sa}(ref)$$
$$i_b(comp) = i_{Lb} - i_{Sb}(ref)$$
$$i_c(comp) = i_{Lc} - i_{Sc}(ref) \quad (7)$$

The respective compensation current and actual filter current are fed as input to hysteresis controller which generates gate pulses for the 3P3W DSTATCOM.

The expanded form of equation (7) is expressed as

$$i_a\,(comp) = [Real(i_{La1}) + Imaginary(i_{La1}) + harmonic\ currents] - [i_{sa}\,(ref)]$$

$$i_b\,(comp) = [Real(i_{Lb1}) + Imaginary(i_{Lb1}) + harmonic\ currents] - [i_{sb}\,(ref)]$$

$$i_c\,(comp) = [Real(i_{Lc1}) + Imaginary(i_{Lc1}) + harmonic\ currents] - [i_{sc}\,(ref)] \quad (8)$$

If the load current of a distribution system is assumed to be balanced, then the real value of the load current will be equal to the corresponding reference source current which makes the reference compensation current to have the value, which is the sum of harmonic and imaginary part of load current for the corresponding phase.

$$i_a\,(comp) = [Imaginary(i_{La1}) + harmonic\ currents]$$

$$i_b\,(comp) = [Imaginary(i_{Lb1}) + harmonic\ currents]$$

$$i_c\,(comp) = [Imaginary(i_{Lc1}) + harmonic\ currents] \quad (9)$$

3.2 ANN based Reference current generation for neutral current mitigation

The ANN based control strategy for neutral current mitigation is modeled as block diagram and depicted in Fig.3. The load currents of the three phases are sensed and summed up using a summer. The summed up value i_{sn} is compared with i_{sn}* which is zero. The difference between the compared values is fed as an input to the ANN controller which generates the reference current signal for the single phase APF. The output of the ANN controller is fed as input to the hysteresis current controller which generates the gate pulses for the single phase APF.

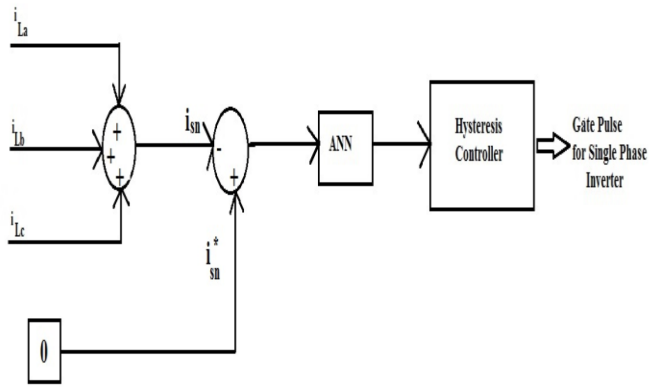


Fig.3.Single phase APF control strategy

4. MATLAB based model for ANN control strategy of DSTATCOM

A MATLAB based model developed with the implementation of PSB toolboxes and Simulink software for 3P4W DSTATCOM is depicted in Fig.4.The roles of ANN controllers implemented in control strategy are as follows:

i) Three ANN controllers for phases a,b,c for the extraction of amplitude of fundamental load current with shift in phase by +90°.

ii) Three ANN controllers for phases a,b,c for the extraction of fundamental component of phase voltage under distorted and unbalanced voltage source condition.

iii) An ANN controller for the extraction of power loss (p_{loss}) component in inverter and coupling inductor in order to meet out the losses, thereby maintaining the voltage across the DC bus capacitor.

iv)An ANN controller for the generation of reference neutral current for 1-ϕ APF which mitigates the neutral current under unbalanced load conditions.

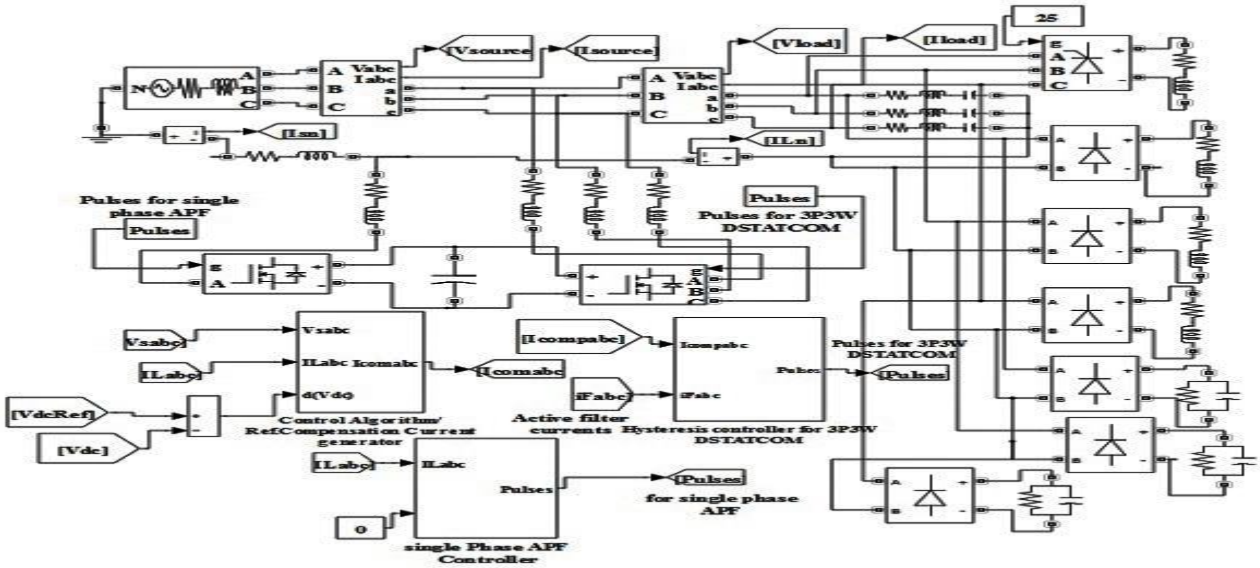


Fig.4. MATLAB/Simulink model of the neural network based I Cos ϕ DSTATCOM

5 Neural coding for creation of neural network block

The primary requirements for better performance of the DSTATCOM are i) Dynamic response of the controller should be high. ii) Reference signal should be processed at a faster rate. iii) Signals should be sensed with high accuracy. The performance of conventional controller is not satisfactory under nonlinear load condition with variation in parameters. But ANN controller fulfils the above mentioned requirements by maintaining the system stability. ANN is rapidly flourishing in the discipline of power electronics. This consists of elements that operate in parallel.

5.1 Proposed ANN architecture

The proposed Back propagation neural network architecture for ANN filter constitute an input layer, hidden layer and output layer. The input vector is fed to the input layer, and then transmitted to the consecutive hidden layer and eventually to the output layer through weighted connections. The operation of each neuron in the hidden and output layer is to take the sum of weighted inputs and to transfer the result via a non-linear activation function. The number of input vectors to the input layer is accounted by the problem and the output of the problem decides the number of neurons in the output layer. The problem specified decides the size and the number of hidden layers between the input and output layers. Initially by varying the number of neurons in the hidden layer, the optimum combination is decided based on the performance error and training period. Fig.5 depicts the flow chart of ANN modeling.

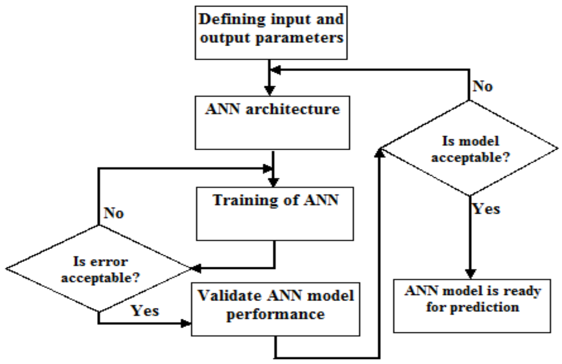


Fig.5. Flow chart of ANN modelling

Lavenberg-Marquardt (LM) back propagation training algorithm 'trainlm' is found suitable for the specified problem, considering MSE for the L index values under varying source and load conditions, training time and overall accuracy[34-35]. The details of ANN architecture of the proposed neural network controllers are listed in Table 1.

In this paper, the following neural coding is implemented for normalization, training and generation of neural network block for i_{loss} component.

```
[pn,ps]=mapminmax(p);
[tn,ts]=mapminmax(t);
net=newff(pn,tn,500,{'tansig','tansig','purelin'},'trainlm');
net=init(net);
net.trainParam.show=70;
net.trainParam.lr=.07;
net.trainParam.mc =0.95;
net.trainParam.epochs=500;
net.trainParam.goals=1e-6;
[net,tr]=train(net,pn,tn);
a=sim(net,pn);
gensim(net,-1);
[m,b,r]=postreg(a,t)
```

Table 1 ANN Parameters for training in MATLAB

Parameter	Values							
	ANN Filter							
	i_{La}	i_{Lb}	i_{Lc}	V_{Sa}	V_{Sb}	V_{Sc}	i_{loss}	i_{Sn}
No of Training data	300	300	300	400	400	400	500	350
No of Testing data	50	50	50	70	70	70	100	40
No of neurons in input layer	1	1	1	1	1	1	2	2
No of neurons in hidden layer	20	20	20	17	17	17	24	14
No of neurons in output layer	1	1	1	1	1	1	1	1
Training function	LM Algorithm (trainlm)							
Performance function	Mean squared error (MSE)							
Activation function (input /hidden/output)	tansig/ tansig/ purelin							
Maximum epochs	380	340	360	420	410	440	500	300
Learning rate	0.05	0.05	0.05	0.04	0.04	0.04	0.07	0.06
Performance goal	$1e^{-6}$							
Normalized range	-1 to 1							
Testing accuracy in %	99.4	98.93	98.5	99.1	99.39	99.12	99.21	98.72

6 Simulation results and discussions

The validation of performance of the proposed neural network control is adjudged using MATLAB/Simulink software. Appendix A list out the details of system parameters. The performance of the propounded scheme for THD reduction, balancing of load, reactive power compensation and mitigation of neutral current is analyzed for varying load and source conditions. The simulations are also carried out using conventional controller for all the varying source and load conditions. The performance of the DSTATCOM with conventional controller is compared with that of neural network control strategy in Tables 4, 5, 6 and 7. The performance of the propounded DSTATCOM with ANN control strategy is analyzed for the following load conditions.

i) Linear unbalanced load. ii)Non-linear load[Three 1-ϕ bridge rectifiers with RL load (i.e., R and L are in series)].iii)Non-linear load [Three 1-ϕ bridge rectifiers with RC load (i.e., R and C are in parallel)].iv)Non-linear load [3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load].v)Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Linear unbalanced load.vi)Non-linear load [Three 1-ϕ bridge rectifiers with RC load] + Linear unbalanced load. vii) Non-linear load [3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load] + linear unbalanced load. viii)Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Non-linear load [Three 1-ϕ bridge rectifiers with RC load].ix)Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Non-linear load [3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load].x)Non-linear load [Three 1-ϕ bridge rectifiers with RC load] + Non-linear load [3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load].xi)Linear unbalanced load + Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Non-linear load [Three 1-ϕ bridge rectifiers with RC load].xii)Linear unbalanced load + Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Non-linear load [3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load].xiii)Linear unbalanced load + Non-linear load [Three 1-ϕ bridge rectifiers with RC load] + Non-linear load [3-ϕ phase controlled bridge rectifier fired at $\alpha = 25°$ with RL load].xiv)Linear unbalanced load + Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Non-linear load [Three 1-ϕ bridge rectifiers with RC load] + Non-linear load[3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load].

The DSTATCOM with neural network control strategy is simulated for the above fourteen varying load conditions with the following four different utility conditions of source voltage:

Case A: Ideal voltage source condition.
Case B: Unbalanced sinusoidal voltage source condition.[Magnitude unbalance of 50% sag in phase a,b,c and Phase unbalance of 20°,-120°,120°]
Case C: Balanced [no unbalance in magnitude and phase] and distorted voltage source condition [i.e., 15% of 3rd harmonic and 18% of 5th harmonic are injected into the source].
Case D: Unbalanced [Magnitude unbalance of 50% sag in phase a,b,c and Phase unbalance of 20°, -120°, 120°] and distorted voltage source condition [i.e., 15% of 3rd harmonic and 18% of 5th harmonic are injected into the source].Details of various source voltage conditions are tabulated in Table 2.

The performance of the DSTATCOM with neural network control strategy is analysed and tabulated for all the fourteen types of loads with the four cases of voltage source condition in Table 4, 5, 6 and 7. Due to limitation in the number of pages, the waveforms are shown only for case xiv of load condition with all the four cases of voltage source.

Case xiv: Linear unbalanced load + Non-linear load [Three 1-ϕ bridge rectifiers with RL load] + Non-linear load [Three 1-ϕ bridge rectifiers with RC load] + Non-linear load [3-ϕ controlled bridge rectifier fired at $\alpha = 25°$ with RL load].

In all the load conditions, the 3-ϕ unbalanced load is changed to 2-ϕ load at time 0.25s and consecutively to 1-ϕ load at 0.3s. Again the load is made as 2-ϕ at time 0.35s and consecutively to 3-ϕ load at 0.4s. Details of variation of load with respect to time are tabulated in Table 3.

6.1 Case A. Performance of DSTATCOM under ideal voltage source condition

The DSTATCOM dynamic performance for the above mentioned source condition is depicted in Fig.6. The propounded neural network control algorithm reduces the THD of the compensated source current to 0.79%, 0.71%, 0.68% for phases a, b, c whereas the load current THD are 11.23%, 11.80%, 11.93% respectively. The THD of the compensated supply current is within 5% which is the benchmark value of IEEE-519 recommendation.

6.2 Case B. Performance under unbalanced voltage source condition

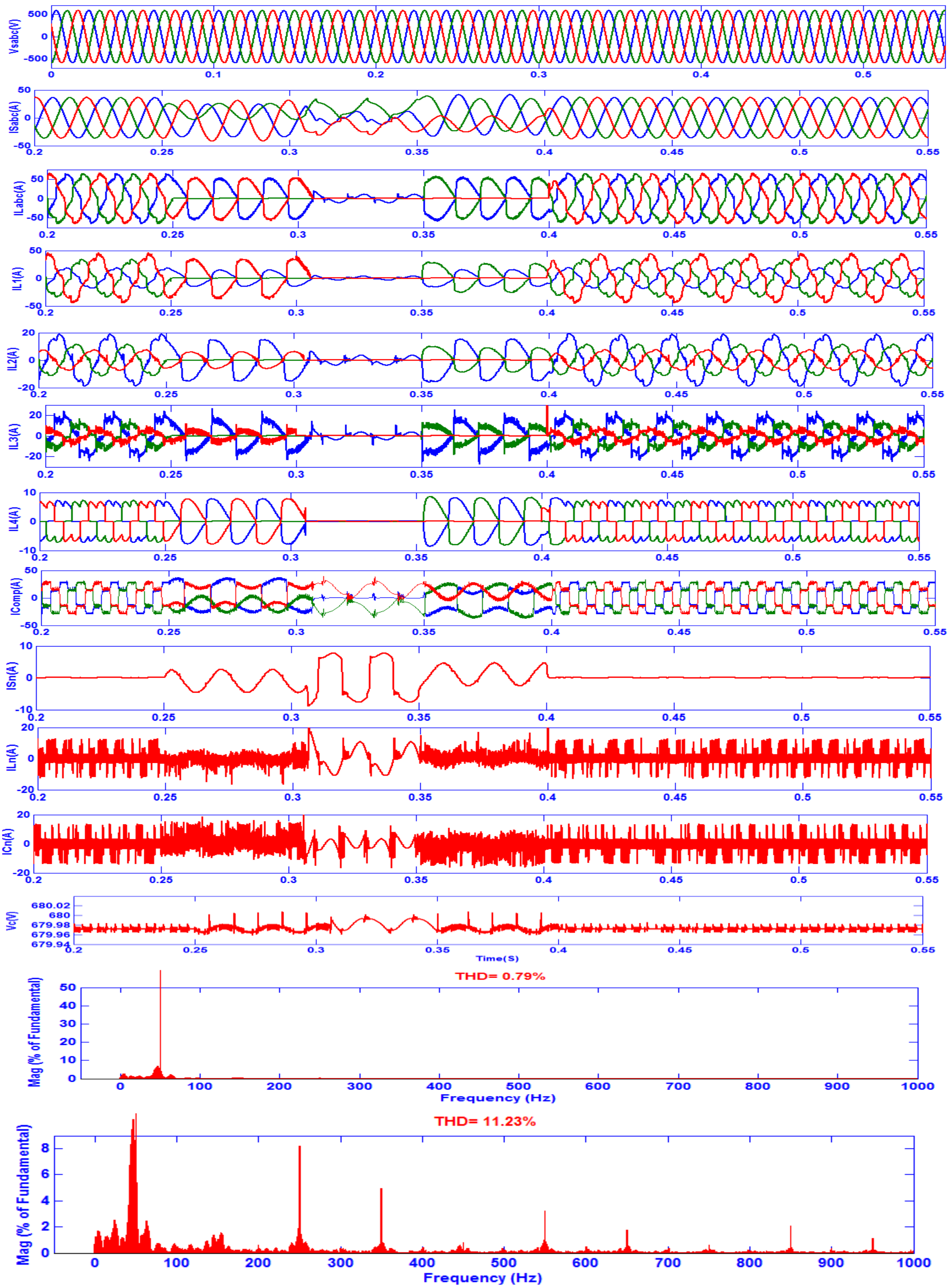
In many practical applications, the possibility of occurrence of unbalanced source voltage is more, which may cause a zero-sequence voltage in the distribution system. To study the effect of unbalance in DSTATCOM a magnitude unbalance of 50% sag is made to occur in phases a,b,c for the time period between t=0.25s and 0.45s and phase unbalance of 20°,-120°, 120° for the entire time period. The DSTATCOM dynamic performance for the above mentioned source condition is shown in Fig.7. The propounded neural network control algorithm reduces the THD of the compensated source current to 0.59%, 0.47%, 0.50% for phases a, b, c whereas the load current THD are 11.24%,11.47%,11.72% respectively. The THD of the compensated source current is within 5% which is the benchmark value of IEEE-519 recommendation.

6.3 Case C. Performance under balanced and distorted voltage source condition

The frequency of occurrence of distorted source voltage condition is likely to be more in many practical applications, which may cause a zero-sequence voltage in the distribution system. To study the impact of distorted source voltage condition in DSTATCOM, 15% of 3rd harmonic and 18% of 5th harmonic are injected into the source for a time period of 0.35s to 0.5s. The DSTATCOM dynamic performance for the above mentioned source condition is shown in Fig.8. The propounded neural network control algorithm reduces the THD of the compensated source current to 0.63%, 0.81%, and 0.82% for phases a, b, c whereas the load current THD are 10.94%, 11.82%, and 11.96% respectively. The THD of the compensated source current is within 5% which is the benchmark value of IEEE-519 recommendation.

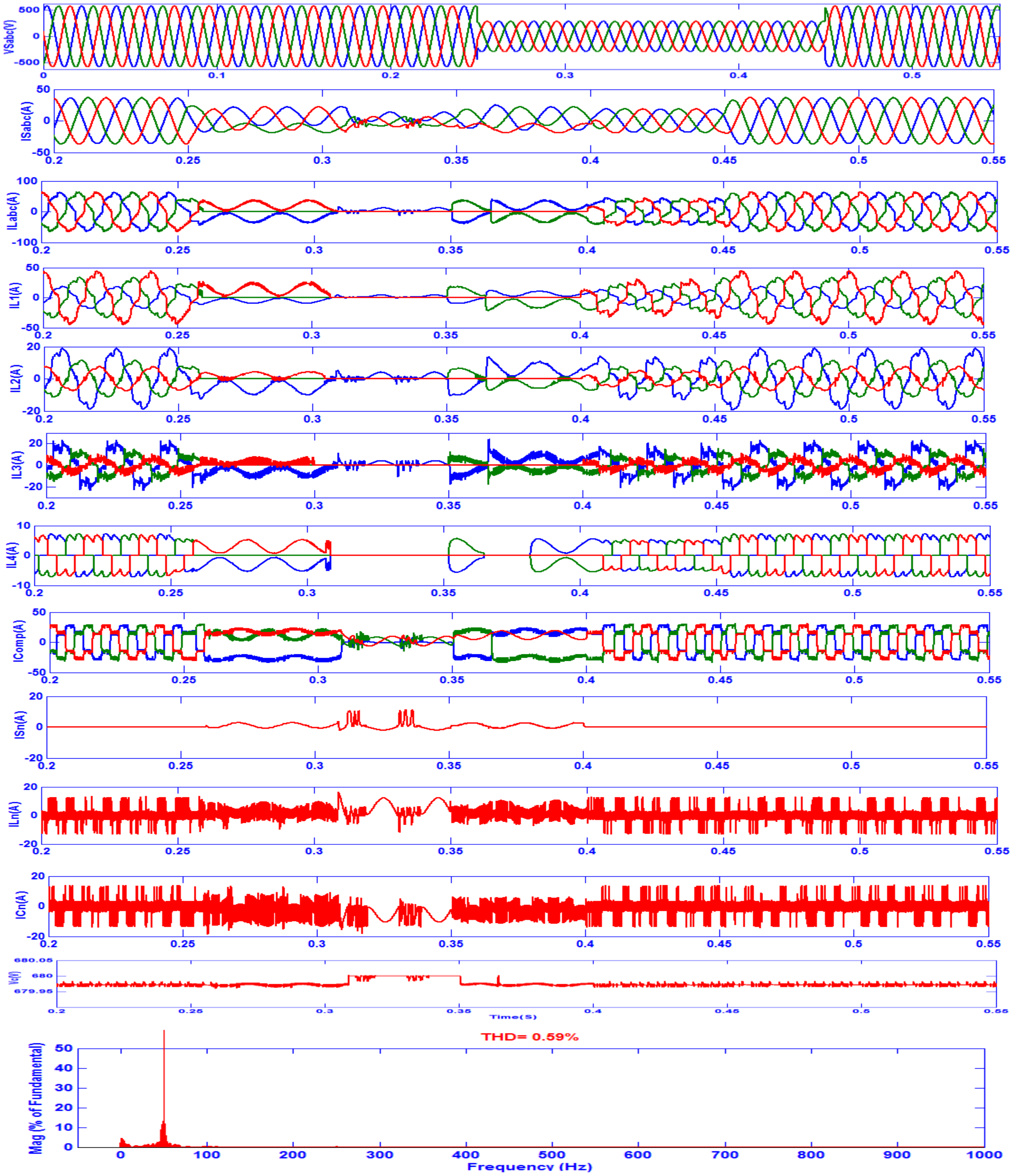
6.4 Case D. Performance under unbalanced and distorted voltage source condition

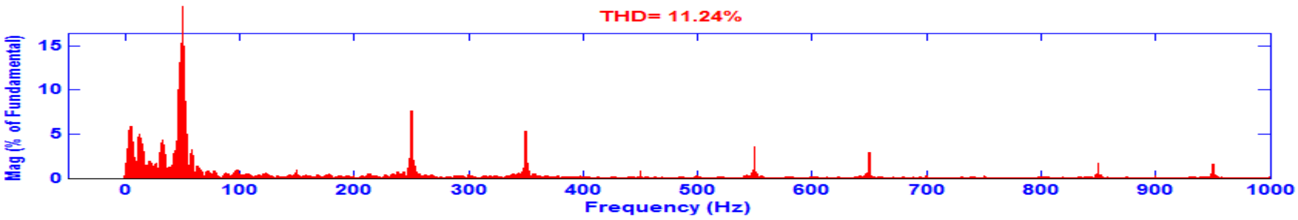
When the source voltage is distorted and also unbalanced, the magnitude of zero sequence voltage is very high and the impact on the load is also critical. To study the impact of distorted and unbalanced voltage source conditions in DSTATCOM, a magnitude unbalance of 50% sag is made to occur in phases a,b,c for the time period between t=0.25s to 0.45s and phase unbalance of 20°,-120°,120° for the entire time period along with 15% of 3rd harmonic and 18% of 5th harmonic is injected into the source for a time period of 0.35s to 0.5s. The DSTATCOM dynamic performance for the above mentioned source condition is shown in Fig.9 The propounded neural network control algorithm reduces the THD of the compensated source current to 1.14%, 1.03%, 1.01% for phases a,b,c whereas the load current THD are 10.90%,11.07%,11.27% respectively.



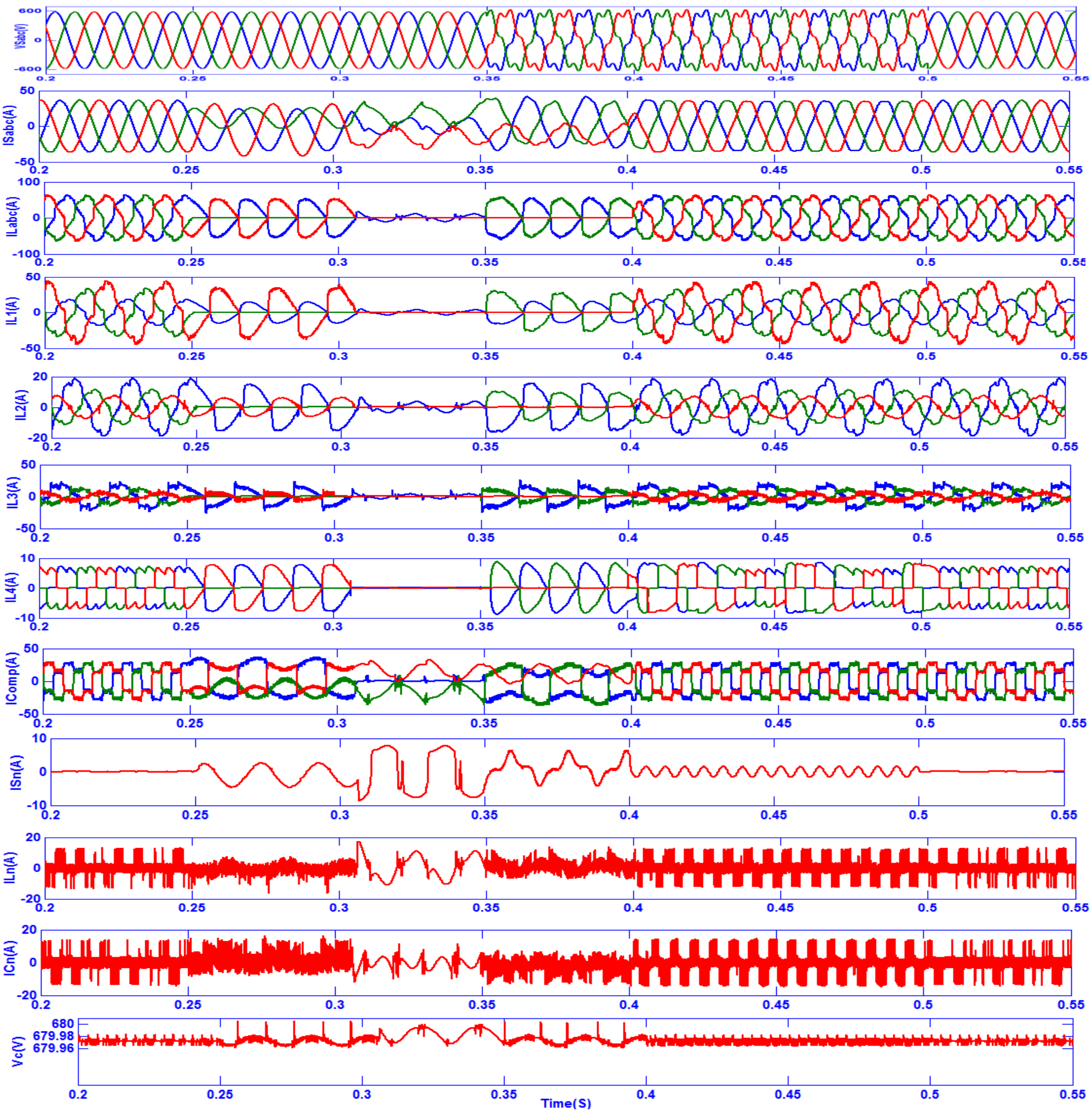
Performance under ideal voltage source condition for load case xiv. Traces of Fig.6. i) ideal voltage source(Vsabc) ii) 3-φ source currents (Isabc) iii) 3-φ load currents (ILabc) iv) load current of linear load (IL1)

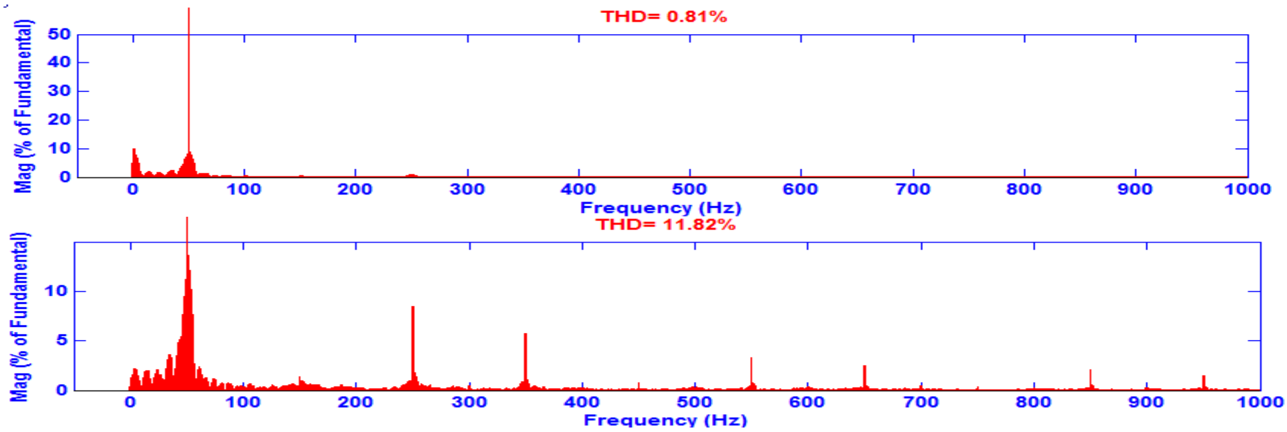
v) load current of three 1-φ bridge rectifiers with RL load (IL2) vi) load current of three 1-φ bridge rectifiers with RC load (IL3) vii) load current of three phase controlled bridge rectifier fired at $\alpha = 25°$ with RL load (IL4) viii) compensator current of 3P3W DSTATCOM (Icomp) ix) source neutral current (Isn) x)load neutral current (ILn) xi)compensator neutral current of single phase APF (ICn) xii)DC bus voltage of DSTATCOM (Vc) xiii)Harmonic spectrum of compensated source current for phase a xiv)Harmonic spectrum of load current for phase a.



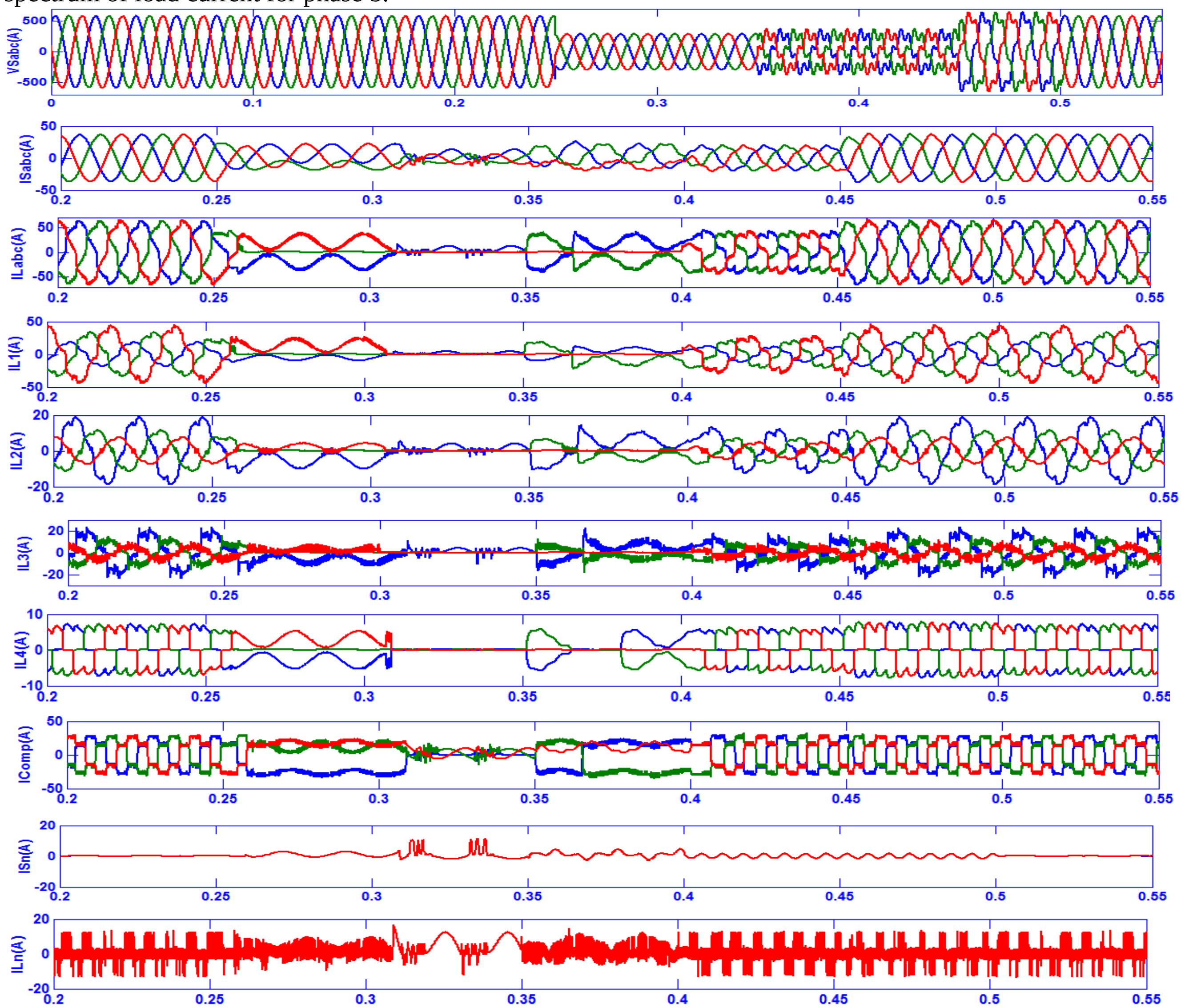


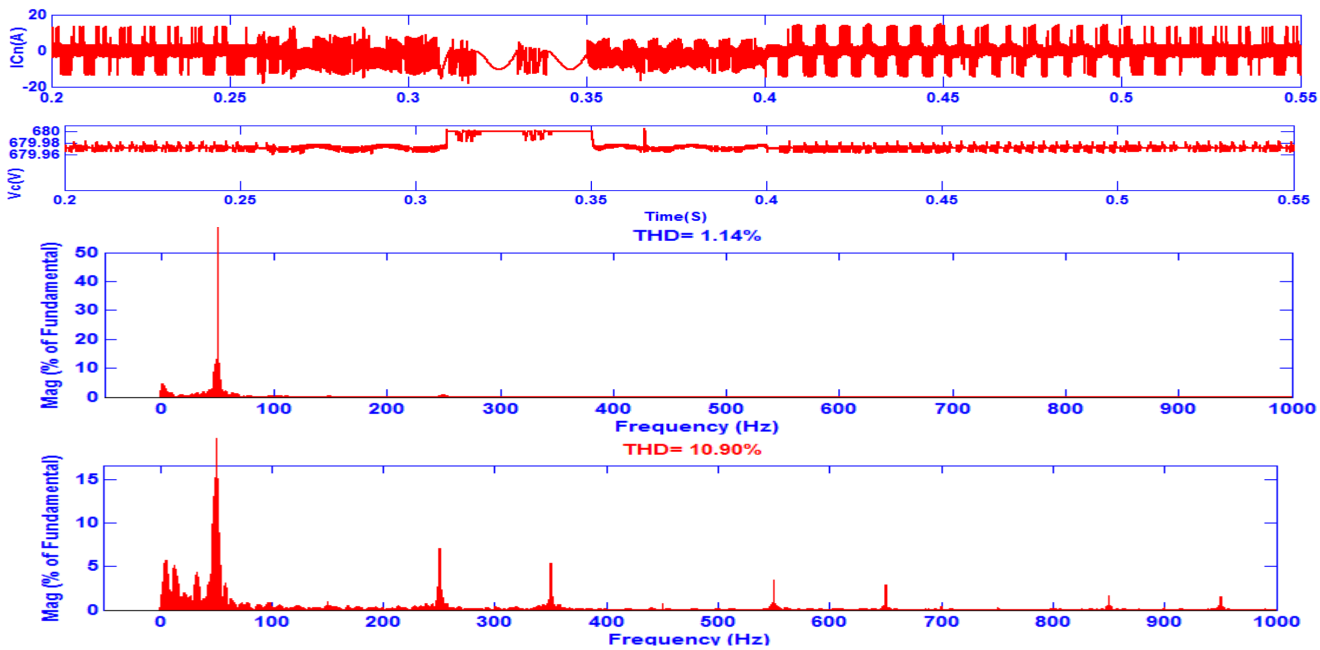
Performance under unbalanced voltage source condition for load case xiv. Traces of Fig. 7. .i) Unbalanced voltage source(Vsabc) ii) 3-φ source currents (Isabc) iii) 3-φ load currents (ILabc) iv) load current of linear load (IL1) v) load current of three 1-φ bridge rectifiers with RL load (IL2) vi) load current of three 1-φ bridge rectifiers with RC load (IL3) vii) load current of three phase controlled bridge rectifier fired at $\alpha = 25°$ with RL load (IL4) viii) compensator current of 3P3W DSTATCOM (Icomp) ix) source neutral current (Isn) x)load neutral current (ILn) xi)compensator neutral current of single phase APF (ICn) xii) DC bus voltage of DSTATCOM (Vc) xiii)Harmonic spectrum of compensated source current for phase a xiv)Harmonic spectrum of load current for phase a.





Performance under balanced and distorted voltage source condition for load case xiv. Traces of Fig 8. i) balanced and distorted voltage source(Vsabc) ii) 3-φ source currents (Isabc) iii) 3-φ load currents (ILabc) iv) load current of linear load (IL1) v) load current of three 1-φ bridge rectifiers with RL load (IL2) vi) load current of three 1-φ bridge rectifiers with RC load (IL3) vii) load current of three phase controlled bridge rectifier fired at $\alpha = 25°$ with RL load (IL4) viii) compensator current of 3P3W DSTATCOM (Icomp) ix) source neutral current (Isn) x)load neutral current (ILn) xi)compensator neutral current of single phase APF (ICn) xii)DC bus voltage of DSTATCOM (Vc) xiii)Harmonic spectrum of compensated source current for phase b xiv)Harmonic spectrum of load current for phase b.





Performance under unbalanced and distorted voltage source condition for load case xiv. Traces of Fig 9. i) unbalanced and distorted voltage source (Vsabc) ii) 3-φ source currents (Isabc) iii) 3-φ load currents (ILabc) iv) load current of linear load (IL1) v) load current of three 1-φ bridge rectifiers with RL load (IL2) vi) load current of three 1-φ bridge rectifiers with RC load (IL3) vii) load current of three phase controlled bridge rectifier fired at $\alpha = 25°$ with RL load (IL4) viii) compensator current of 3P3W DSTATCOM (Icomp) ix) source neutral current (Isn) x) load neutral current (ILn) xi) compensator neutral current of single phase APF (ICn) xii)DC bus voltage of DSTATCOM (Vc) xiii)Harmonic spectrum of compensated source current for phase a xiv)Harmonic spectrum of load current for phase a.

Table 2
Details of various source voltage conditions

Case:A	Case:B	Case:C	Case:D
Ideal voltage source condition: 415V, 50 Hz, with phase difference of (0°,-120°,+120°).	Unbalanced voltage source conditions (both amplitude and phase): 415V, 50 Hz. phase unbalance of (20°, -120°,+120°) & Amplitude unbalance of 50% sag in all three phases for the duration between 0.25 and 0.45 seconds	Balanced and Distorted voltage source condition: 415V, 50Hz. phase unbalance of (0°, -120^0,+120°) & Distorted condition: 15% of 3rd order and 18% of 5th order harmonics for the duration between 0.35 and 0.5 seconds.	Unbalanced (both amplitude and phase) and Distorted voltage source condition: 415V, 50 Hz, phase unbalance of (20°, -120°, +120°) & Amplitude unbalance of 50% sag in all three phases for the duration between 0.25 and 0.45 seconds. Distorted condition: 15% of 3rd order and 18% of 5th order harmonics for the duration between 0.35 and 0.5 seconds.

Table 3
Details of variation of load with respect to time

Load Conditions	Three phase load	Two phase load	Single phase load
	Time in s	Time in s	Time in s
i to xiv	0.2 to 0.25 & 0.4 to 0.55	0.25 to0.3 & 0.35 to 0.4	0.3 to 0.35

Table 4
Comparison of performance of DSTATCOM with proposed controller and conventional controller for ideal voltage source condition

Load Conditions	% THD									Proposed Controller		Conventional Controller	
	I_{La}	I_{Lb}	I_{Lc}	Proposed Controller			Conventional Controller			I_{SN} rms(A)	V_c rms(V)	I_{SN} rms(A)	V_c rms(V)
				I_{Sa}	I_{Sb}	I_{Sc}	I_{Sa}	I_{Sb}	I_{Sc}				
i)	12.05	12.34	11.96	1.78	0.86	0.99	1.93	1.76	0.99	0.5265	680	0.5685	678.4
ii)	10.43	13.99	13.73	1.64	2.79	3.17	1.78	2.80	4.04	0.72	680	0.864	678.4
iii)	13.11	16.23	17.57	1.36	2.62	3.10	1.76	3.16	5.79	0.8378	680	0.8605	678.4
iv)	28.09	24.78	26.06	3.92	3.52	4.10	11.70	11.62	12.05	9.43	680	9.576	678.4
v)	11.93	11.86	12.33	0.94	0.83	0.66	1.04	1.17	0.71	0.2059	680	0.2169	678.4
vi)	11.34	11.74	11.93	0.86	0.75	0.62	0.96	0.99	0.63	0.1611	680	0.1859	678.4
vii)	10.54	12.64	12.56	1.38	0.90	0.82	1.35	0.97	0.65	0.47	680	0.559	678.4
viii)	10.80	13.43	13.53	0.89	1.23	1.56	0.82	1.25	1.41	0.4597	680	0.4678	678.4
ix)	11.48	12.23	12.91	1.52	2.60	2.25	2.70	2.34	2.52	0.5045	680	0.6249	678.4
x)	11.94	14.05	15.83	1.80	2.25	3.08	2.55	1.44	2.61	0.6619	680	0.5733	678.4
xi)	11.04	11.63	11.99	0.71	0.67	0.62	0.75	0.87	0.58	0.0656	680	0.0925	678.4
xii)	12.78	13.66	13.59	1.12	0.89	0.78	0.69	0.57	0.56	0.1908	680	0.2028	678.4
xiii)	11.28	11.66	11.71	0.87	0.65	0.66	0.80	0.67	0.79	0.1463	680	0.171	678.4
xiv)	11.23	11.80	11.93	0.79	0.71	0.68	0.55	0.55	0.60	0.0617	680	0.0896	678.4

Table 5
Comparison of performance of DSTATCOM with proposed controller and conventional controller for unbalanced voltage source condition

Load Conditions	% THD									Proposed Controller		Conventional Controller	
	I_{La}	I_{Lb}	I_{Lc}	Proposed Controller			Conventional Controller			I_{SN} rms(A)	V_c rms(V)	I_{SN} rms(A)	V_c rms(V)
				I_{Sa}	I_{Sb}	I_{Sc}	I_{Sa}	I_{Sb}	I_{Sc}				
i)	13.47	12.78	12.32	1.93	1.01	0.93	1.87	1.31	1.82	0.5316	680	0.5609	678.4
ii)	13.75	15.98	14.20	1.87	3.23	3.46	1.47	2.26	2.72	0.7142	680	0.8657	678.4
iii)	11.48	14.58	15.22	1.22	2.50	2.84	2.06	3.26	5.75	0.8418	680	0.8562	678.4
iv)	24.09	24.22	22.36	2.90	3.49	3.11	12.10	12.20	13.10	9.967	680	9.605	678.4
v)	12.06	11.69	12.07	0.79	0.58	0.54	0.82	0.93	0.76	0.2051	680	0.2168	678.4
vi)	11.65	11.57	11.50	0.72	0.53	0.57	0.77	0.80	1.04	0.1608	680	0.186	678.4
vii)	13.95	12.59	12.89	1.36	0.67	0.91	1.64	1.76	1.07	0.4761	680	0.5571	678.4
viii)	10.69	13.09	13.21	0.82	1.29	1.59	0.91	1.57	2.07	0.4575	680	0.4677	678.4
ix)	10.65	12.79	12.47	0.82	2.15	1.60	3.18	3.38	2.58	0.5111	680	0.6321	678.4
x)	11.95	14.42	15.55	1.92	3.25	4.14	2.70	1.54	2.42	0.5996	680	0.5678	678.4
xi)	10.97	11.23	11.57	0.55	0.52	0.43	0.88	1.04	1.28	0.0628	680	0.0925	678.4
xii)	12.06	11.99	11.39	0.88	0.70	0.54	0.68	0.65	0.77	0.1911	680	0.1982	678.4
xiii)	11.62	11.56	11.90	0.79	0.62	0.53	1.20	1.17	1.00	0.1454	680	0.171	678.4
xiv)	11.24	11.47	11.72	0.59	0.47	0.50	0.82	0.55	0.95	0.0601	680	0.0880	678.4

Table 6
Comparison of performance of DSTATCOM with proposed controller and conventional controller for balanced and distorted voltage source condition.

Load Conditions	% THD									Proposed Controller		Conventional Controller	
	I_{La}	I_{Lb}	I_{Lc}	Proposed Controller			Conventional Controller			I_{SN} rms(A)	V_c rms(V)	I_{SN} rms(A)	V_c rms(V)
				I_{Sa}	I_{Sb}	I_{Sc}	I_{Sa}	I_{Sb}	I_{Sc}				
i)	12.11	12.33	12.05	1.68	1.15	0.82	2.33	2.31	1.09	0.531	680	0.570	678.4
ii)	12.63	15.76	15.18	1.95	2.71	3.57	2.42	3.87	4.31	0.7142	680	0.8558	678.4
iii)	12.27	15.96	17.03	1.58	2.18	2.96	2.20	3.99	5.67	0.8378	680	0.8544	678.4
iv)	26.62	25.09	24.83	2.82	3.45	3.64	12.28	12.38	12.68	9.378	680	9.591	678.4
v)	11.63	11.74	12.21	0.69	0.96	0.78	1.22	1.57	0.97	0.2051	680	0.2168	678.4
vi)	11.36	11.86	11.95	0.60	0.85	0.80	1.07	1.33	0.93	0.1611	680	0.1859	678.4
vii)	14.40	14.03	13.45	1.33	1.15	1.04	1.66	1.18	0.77	0.4784	680	0.559	678.4
viii)	10.45	13.45	13.63	0.91	0.94	1.34	1.21	1.60	1.86	0.4579	680	0.4678	678.4
ix)	10.40	12.68	12.80	1.26	1.86	1.55	3.43	2.90	2.94	0.5018	680	0.6249	678.4
x)	11.18	13.52	14.47	1.11	1.86	1.68	3.06	2.19	3.15	0.5993	680	0.5733	678.4
xi)	11.06	11.94	12.00	0.63	0.85	0.82	0.94	1.20	0.95	0.0647	680	0.0925	678.4
xii)	11.79	11.70	11.50	0.88	0.65	0.83	1.11	0.87	0.95	0.1909	680	0.1949	678.4
xiii)	11.22	11.72	11.76	0.94	0.69	0.89	1.03	0.85	1.03	0.1465	680	0.1714	678.4
xiv)	10.94	11.82	11.96	0.63	0.81	0.82	0.99	0.86	0.99	0.0593	680	0.0896	678.4

Table 7
Comparison of performance of DSTATCOM with proposed controller and conventional controller for unbalanced and distorted voltage source condition.

Load Conditions	% THD									Proposed Controller		Conventional Controller	
	I_{La}	I_{Lb}	I_{Lc}	Proposed Controller			Conventional Controller			I_{SN} rms(A)	V_c rms(V)	I_{SN} rms(A)	V_c rms(V)
				I_{Sa}	I_{Sb}	I_{Sc}	I_{Sa}	I_{Sb}	I_{Sc}				
i)	13.29	13.83	12.57	2.70	1.75	1.36	2.56	1.79	2.52	0.5316	680	0.564	678.4
ii)	13.29	15.11	14.03	2.47	4.04	4.24	1.53	2.55	2.39	0.7142	680	0.8634	678.4
iii)	11.97	14.39	15.01	2.07	3.20	3.68	2.40	3.85	5.67	0.8403	680	0.8562	678.4
iv)	21.06	33.14	20.20	4.29	4.19	3.07	9.31	10.07	10.29	9.318	680	9.61	678.4
v)	11.61	11.21	11.66	1.43	1.29	1.11	1.37	1.50	1.16	0.2053	680	0.2168	678.4
vi)	11.19	11.12	11.22	1.22	1.22	1.04	1.34	1.34	1.46	0.1615	680	0.186	678.4
vii)	11.60	11.01	11.67	1.85	1.39	1.37	2.17	1.99	1.74	0.4785	680	0.5576	678.4
viii)	10.19	12.43	12.64	1.48	1.68	2.21	1.44	2.36	2.57	0.458	680	0.4677	678.4
ix)	10.14	11.98	11.98	1.61	2.70	2.34	3.55	2.87	2.84	0.5111	680	0.6321	678.4
x)	11.78	13.82	14.89	2.02	3.20	4.04	3.55	2.87	2.84	0.5996	680	0.6321	678.4
xi)	10.55	10.76	11.19	1.10	1.18	1.00	1.19	1.48	1.67	0.06284	680	0.0925	678.4
xii)	11.54	11.42	10.85	1.43	1.23	0.97	1.35	1.17	1.34	0.1911	680	0.2005	678.4
xiii)	11.17	11.12	11.56	1.21	1.12	0.96	1.55	1.58	1.26	0.1454	680	0.171	678.4
xiv)	10.90	11.07	11.27	1.14	1.03	1.01	1.32	1.43	1.14	0.06019	680	0.0897	678.4

The dynamic performance of the neural network based proposed system is validated using the following inferences made from the simulation results.

i) Under all changing conditions of load and source, the source currents are sinusoidal, balanced and nearly in phase with supply voltage. The %THD of the compensated source current is well below 5% which is bench mark value of IEEE-519 standard, whereas the %THD of the uncompensated source current is high.

ii) Even under 2-ϕ and 1-ϕ load conditions, the source currents are balanced and sinusoidal.

iii) When the 1-ϕ APF is switched ON, the neutral current of the source is nearly zero and this ensures proper neutral current compensation. When the load is changed from 3-ϕ to 2-ϕ, there is a considerable reduction in the neutral current (i.e.,) nearly 60%.

iv)It is also inferred from the waveform that the DC bus voltage of the DSTATCOM is retained at the reference value under varying load and source conditions.

v) In the source side, the power factor is nearly unity.

vi)Compensated source current THD is well below 5% even for unbalanced and distorted source voltage condition which makes the load more critical. Harmonic mitigation is achieved effectively in spite of high harmonic content of supply voltage.

vii) Based on the performance comparison of DSTATCOM with proposed controller and conventional controller for varying source and load conditions in Table 4, 5,6 and 7. It is inferred that

- The %THD of the source current with proposed controller is lesser than that of conventional controller for all varying source and load conditions.
- The conventional controller fails to reduce the %THD of the source current below 5% for the load case (iv) and phase c source current for load case (iii) which does not satisfy IEEE-519 standard.
- Single phase APF with proposed controller mitigate source neutral current more effectively with less Rms value of the I_{SN} when compared to conventional controller.
- The voltage across the DC bus capacitor is well regulated at 680V using proposed controller compared to the conventional controller.

7 Conclusion

A novel neural network control strategy is proposed and has been implemented for the DSTATCOM in 3P4W distribution system. The proposed control strategy performance is evaluated for all possible source conditions with varying fourteen types of non-linear and linear loads. The propounded DSTATCOM performance has been investigated and validated through simulation employing MATLAB/Simulink software. The simulation results and tabulation proves the efficacy of the control strategy over conventional control under varying load and source conditions. The dynamic performance of the neural network based D-STATCOM is validated and highlighted using the following inference made from the simulation results.

i) Compensation of harmonic content.

ii) Under all changing conditions of load and source, the supply currents are sinusoidal, balanced and nearly in phase with supply voltage.

iii) Reactive power compensation.

iv)Compensation of neutral current under unbalanced linear and non-linear loads.

v) Maintenance of DC capacitor voltage to its reference value under all operating conditions.

vi)In addition, the proposed control scheme reduces the source current's THD well below 5% which is the bench mark value of IEEE-519 standard.

vii) The performance of the DSTATCOM with proposed controller is found to be superior to with conventional controller for all varying source and load conditions.

APPENDIX A

Simulation Parameters: Rated source voltage: 3Φ, four wire system, 415V, 50Hz. Zs = R_s=0.05Ω, L_s=2mH. DC bus voltage 680V. DC bus capacitance 3000μF. DSTATCOM coupling inductor: Rsh=2Ω,Lsh=2mH. 1φ APF coupling inductor: Rsn=1Ω,Lsn=3mH. Ripple filter: R_f=5Ω,C_f=5μF

i)Linear Load: Phase-a 25.93kVA,Phase-b 50.47kVA, Phase-c 75.31kVA. ii) Non –Linear load: Case a) Three 1Φ bridge rectifier with RL load connected between, the phase –a and neutral with load Rdc=2Ω, L_{dc}=1mH, phase –b and neutral with load Rdc=3Ω, L_{dc}=2mH, phase –c and neutral with load Rdc=4Ω, L_{dc}=3mH. Case b) Three 1Φ bridge rectifier with RC load connected between, the phase –a and neutral with load Rdc=2Ω, C_{dc}=9μF, phase –b and neutral with load R_{dc}=3Ω, C_{dc}=5μF, phase –c and neutral with load R_{dc}=5Ω, C_{dc}=10μF. Case c) Three phase controlled bridge rectifier fired at $\alpha=25^o$ with RL load R_{dc}=7Ω, L_{dc}=3mH.

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