Improved Performance of the Positive Output Elementary Split Inductor-Type Boost Converter using Sliding Mode Controller plus Fuzzy Logic Controller

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Abstract: - This article presents a design of variable frequency based reduced-order sliding mode controller (ROSMC) plus fuzzy logic controller (FLC) for positive output elementary split inductor-type boost converter (POESITBC). Because of the time varying switched mode of operation, the dynamic characteristics of POELSITBC is non-linear in nature. The conventional controllers are not able to improve the dynamic performance under the line and load variations. In order to enhance the dynamic characteristics together with the inductor current and output voltage regulation of the POTSITBC, a ROSMC plus FLC is developed. The designed ROSMC is fit to the naturally variable-structured POESITBC when expressed in the reduced order state-space average based model. The ROSMC is act as an inner current loop control for POESITBC and the FLC is act as an outer loop for the same converter, which are used to regulate the inductor current, regulate output voltage and reduce the steady state error as well as the outstanding initial start-up response of the converter in spite of line and load changes. The performance of the developed controller is validated at different working regions through the MATLAB/Simulink model over a ROSMC plus proportional-double integral-controller (PDIC). Simulated results are indicated that designed controller can acquire the superior output voltage and inductor current regulations at different stages.

Key-Words: - DC-DC power conversion, positive output elementary split inductor-type boost converter, sliding mode controller, proportional double integral controller, state-space average method

1 Introduction

In recent days, huge boost-up voltage transfer gains are essential for most of the present scenario applications such as battery backup models for uninterruptible power supply, solar cell energy conversion models, fuel cell energy conversion models, medical equipments, robot systems, renewable energy power systems, mobile phones applications [1-3]. Theoretically, traditional dc-dc converters such as the buck, boost, buck–boost, Cuk, SEPIC (single-ended primary inductor converter), Zeta converter and Luo-Converters can obtain a large voltage transfer gain viz. large duty cycle, however miserably, in practical implementation, which is restricted due to the consequence of power semiconductor switches, rectifier power diodes, and the equivalent series resistance (ESR) of inductors and capacitors. Additionally, the very large duty-cycle working will result in a serious reverse-recovery crisis [4-7]. The voltage transfer gain of the fly-back converter produces high and it need good electrical isolation and simple design. The main demerits of this converter has transformer, which make the more rate of change of voltage across the power switches, more switch on/off losses, EMI issues and decreasing the system efficiency. These problems are rectified by transformerless based dc-dc converters, namely; cascade boost type, and the boost type integrating with switched-capacitor technique has been reported [8]-[12]. Nevertheless, these techniques are all multifaceted and have a huge cost. To solve the above problems Cuk and Luo converters has been introduced. The Cuk converter needs two inductors and one additional energy-transferring capacitor, and the Luo converter needs more components over Cuk converter. According to this problems, positive - output KY boost converter is developed, which needs three additional capacitor, order of the system has increased and make the controller design is difficulty. The voltage lift technique (VLT) has been effectively employed in the design of advanced dc-dc converters, in which the output voltage raises stage-by-stage in arithmetic progression. In this

technique inductor and capacitor plays vital roll. The voltage-lift split inductor type boost converter has produced huge voltage transfer gains in comparison with voltage-lift technique as well as other conventional converters [13-14]. Thus, positive output elementary split inductor-type boost converter (POESITBC) does the same with a simple structure. The POTLSITBC is an advanced dc-dc converter topology, which converts the positive dc source voltage into positive dc load voltage. The POESITBC have complex non-linear models by means of circuit parameters variation. The control methodologies for such converter want to be premeditated for the upcoming application. Therefore, in this article the POESITBC is selected for study. The various modelling methods for switching dc-dc converters have been reported [15-18]. However, among these methods state space averaging technique has very famous tool for modelling of power converters. The small-signal analysis of dc-dc converters with sliding mode controller (SMC) has been addressed [19]. Still, this method would not expect the dynamic response of a switching converter in saturated region and works only for a particular condition. The verification of proportional-integral-derivative (PID) or Proportional-integral-controller (PIC) for buck, boost, and buck-boost converters has been demonstrated [20-24]. However, these control methods are very perceptive to circuit components modifications, changing from ON/OFF states, line and load variations etc. The victory of the classical non-linear controller lies in performing outstanding against these problems as dc-dc converters are intrinsically variable structure systems (VSS). The controller of the POESITBC must compensate with their inherent nonlinearity and extensive input supply and output side variations, guaranteeing constancy in any working condition while providing fast transient and enhanced dynamic responses. Basically, the SMC applies a high-speed switching control law to move the non-linear phase trajectory onto a particular surface in the phase plane, called the sliding manifold, and to keep it on this surface for all consecutive time [25-27]. Conventional based SMC design for dc-dc converters has been well executed [28-33]. The reduced order based SMC for Cuk' dc-dc converter has been discussed in [34]. All these SMC methods offer many advantages over the classical linear PIC or PID controller; they provide stability even for large line and load disturbances, robustness, first-rate dynamic response, and uncomplicated execution. The conventional SMCs are enforcing the system phase trajectory along with ideal sliding surface at infinite frequency. This is unwanted as high operating switching frequency will result in excessive switching losses, inductor loss and electromagnetic interference (EMI) noise difficulties. To resolve these problems, hysteresis bandwidths using the boundary conditions are normally employed to improve the above-mentioned problem in SMCs. The constant operating frequency based SMC for positive output triple-lift split inductor-type boost converter has been addressed [14]. Still, the results of the same converter using this controller has produced large peak overshoots and long settling time during the line and load variation as well as the transient region. The SMC for Luo-Converters with constant frequency operation has been discussed in [35]. From these articles, it is well visibly indicated that the output voltage and inductor current of the converters has produced more overshoots and taking long settling time using SMC. The current distribution control for shunt connected various dc-dc converters using SMC was presented in [36]. However, these articles discussed about the control of the output current and voltage for the SMC, which reported the additional number of sensors unit, is necessary, calculation is complexity, and more overshoots during dynamic conditions. A PWM based double-integral type of indirect SMCs for switched mode power converter has been presented [37-38]. Even if the results for applied control technique for the converter has generated huge start-up overshoot, more peak at line and load disturbances conditions, huge steady state error and settling time. Reduced order based fixed switching frequency SMC for Luo-converter has been well presented [39]. However, the converter using this control method has produced more overshoots under the line and load disturbances regions. The fixed switching frequency based SMC for higher-order dc-dc converters has been reported [40]. However, the problems of this control method have more calculations, implementation intricacy and necessities of more sensors units.

The fuzzy logic controller (FLC) is a form of heuristic-reasoning based expert-knowledge habitual control scheme, which can't need an accurate numerical model of the plant or intricate calculations. The control design is easy because it relies on the designer's accepting of the plant's activities and is based on the qualitative linguistic control rules [41]. The FLC for output voltage regulation of various dc-dc has been reported [42-43]. The main benefits of this controller have good dynamic performance during line and load disturbances and effortless design. These above mentioned problems are solved by the developed

reduced order sliding mode controller (ROSMC) plus FLC.

Therefore, in this article, it is developed to a design of a ROSMC plus FLC for POESITBC in continuous conduction mode (CCM). The reduced order model of the POESITBC is derived with help of the famous state space averaging method at first and then ROSMC plus PDIC is designed. The FLC is used to regulate output voltage the converter and its rules are designed based on the same converter performances.

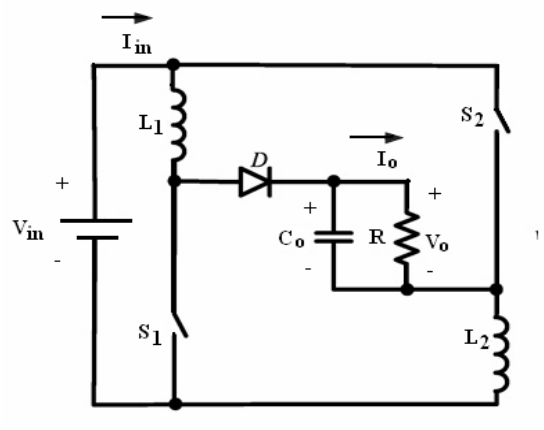
The performance of the POESITBC using the designed controller is confirmed at various working conditions viz. appropriate selection of the controller sliding surface coefficients and fuzzy rules. The controller coefficients of ROSMC are evaluated by reduced order state space average model of the same converter using trade-off choice. The major benefits of developed ROSMC is realization with variable frequency (within the boundary limit) has a effortless control structure, little calculations, easy implementation of control methodology, and less amount of sensing units.

The organization of this article is as follows. Section 2 presents the circuit operation, design of circuit parameters, state-space average reduced-order modelling of the POESITBC. The systematic step-by-step design procedure of ROSMC plus FLC and PDIC for the POESITBC is presented in section 3. The simulation results of the POESITBC using ROSMC plus FLC, and ROSMC plus PDIC at the various operating regions are discussed in sections 4. The conclusions are addressed in section 5.

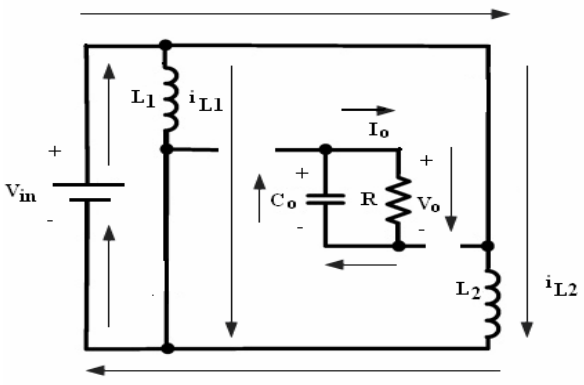
2 Operation and modelling of a POESITBC

2.1 Operation and modelling of POESITBC

The main power circuit of the POESITBC is shown in Fig.1 (a). It consists of two inductors (L_1, L_2), output capacitor C_o, two power switches (S_1, S_2), output diode D, V_O is the output voltage and load resistance R. the power switches are controlled concurrently with help of the single control signal. It is assumed that all the components are ideal and in addition, the POTLSITBC works in CCM. The operation of the same converter can be divided in to two states, viz. the switch-ON and the switch-OFF. Fig.1 (b) and Fig.1(c) show the two states of operation of this converter [14].



(a)



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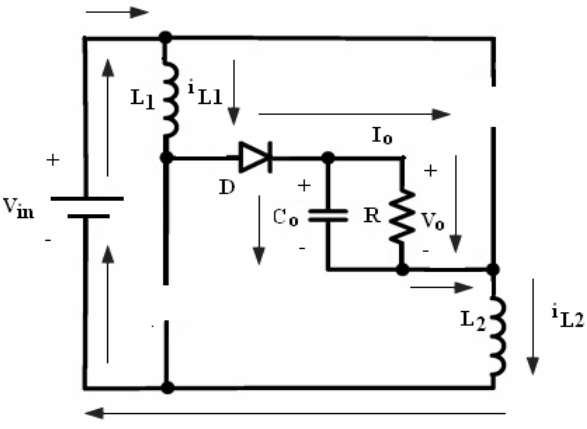

(c)

Fig. 1 Power circuit of POESITBC, (a) topology, (b) equivalent circuit during state 1 operation, and (c) equivalent circuit during state 2 operation.

In state1 operation (refer the Fig. 1(b)), when the switches (S_1, S_2) are closed and the diode D is reverse polarized. The stored energy in the output capacitor C_o releases to the load resistance. The supply voltage V_{in} is connected to the inductors in shunt arrangement; as a result, both the inductors are energized. Therefore, the potential across the inductor (L_1, L_2) can be expressed as equation (1)

$$V_{L1} = V_{L2} = V_{in} \tag{1}$$

The state space equation of the POTLSITBC in state 1 operation will be expressed as equation (2)

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_{in} \\ C_0 \dfrac{dV_0}{dt} = \dfrac{V_0}{R} \end{cases} \tag{2}$$

During the state 2 operation (refer the Fig. 1(c)), switches (S_1, S_2) are in open state, the output capacitor C_o, diode D, inductors (L_1, L_2), and input voltage (V_{in}) are connected in series arrangement. According to this arrangement, the total energy from the input source, energy stored in the storage components is transferred to the load. Then, the potential across the inductor (L_1, L_2) can be written as equation (3)

$$V_{L1} = V_{L2} = \frac{V_{in} - V_o}{2} \tag{3}$$

The state space equation of this converter during the state 2 operation can be inscribed as equation (4)

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = \dfrac{V_{in} - V_0}{2} \\ C_0 \dfrac{dV_0}{dt} = i_{L1} - \dfrac{V_0}{R} \end{cases} \tag{4}$$

In this circuit, there are two storage inductors, which are identical values. Therefore, the current flows through both the inductors are same (i_{L1}=i_{L2}). As a result, omitting the any one inductor (trade-off choice) in the converter. The state space variables of the POESITBC are selected such as the inductor current i_{L1}, and voltage V_o respectively x_1, and x_2. Utilizing equations (1), and (2), the reduced-order state-space average modelling of the POESITBC can be as expressed by equation (5).

$$\begin{bmatrix} i_{L1} \\ V_0 \end{bmatrix} = \begin{bmatrix} 0 & \dfrac{-1+d}{2L_1} \\ \dfrac{1-d}{C_0} & \dfrac{-1+2d}{RC_0} \end{bmatrix} \begin{bmatrix} i_{L1} \\ V_0 \end{bmatrix} + \begin{bmatrix} \dfrac{1+d}{2L_1} \\ 0 \end{bmatrix} V_{in} \tag{5}$$

$$A = \begin{bmatrix} 0 & \dfrac{-1+d}{2L_1} \\ \dfrac{1-d}{C_0} & \dfrac{-1+2d}{RC_0} \end{bmatrix}, B = \begin{bmatrix} \dfrac{1+d}{2L_1} \\ 0 \end{bmatrix}, C = \begin{bmatrix} 0 & 1 \end{bmatrix}, D = 0 \tag{6}$$

Where, A, B, C, and D are averaged reduced order system state space matrices.

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2.2 Design of POESITBC circuit elements

The POESITBC circuit elements are intended with the following specifications.

The design computation of the POESITBC as follow;

- Choose the duty cycle d for the POESITBC worked in CCM and it is evaluated by using the equation (7)

$$\frac{V_0}{V_{in}} = \frac{1+d}{1-d}, \quad d = 0.6 \tag{7}$$

- Estimate the I_o (average load current) with help of the equation (8)

$$I_0 = \frac{V_0}{R_0} = \frac{48}{50} = 0.96\,\text{A} \tag{8}$$

- Find out the output power with equation (8)

$$\begin{aligned} P_0 &= V_0 I_0 \\ P_0 &= 48 \times 0.96 \\ P_0 &= 46.08\ \text{W} \end{aligned} \tag{9}$$

- Choose the efficiency of the system and allow it be 93.27 % in this study and it is applied in equation (10) to obtain the input power

$$\eta = 93.27, \quad P_{in} = P_0 / \eta, \; P_{in} = \frac{46.08}{0.9327}$$
$$P_{in} = 49.404\text{W} \tag{10}$$

- Compute I_{in} (average input current) with help of equation (11)

$$I_{in} = \frac{P_0}{V_{in}} = \frac{49.404}{12}, \quad I_{in} = 4.117\text{A} \tag{11}$$

- Assume the inductors current ripple $\Delta i_{L1} = \Delta i_{L2} = 0.6A$ by using the precise switching frequency (refer the Table.1) to be used in the equation (12), and obtain the crucial value of the inductors.

$$L_1 = \frac{V_{in}\, d}{f \Delta i_{L1}}, \; L_1 = \frac{12 \times 0.6}{100e^3 \times 0.6}, \; L_1 = L_2 = 100\mu\text{H} \tag{12}$$

- Select output the capacitor voltage ripple $\Delta V_o = 0.16V$ by using the specified operating frequency (see the Table. 1) to be utilized in the equation (13), and found the necessary value of the capacitor.

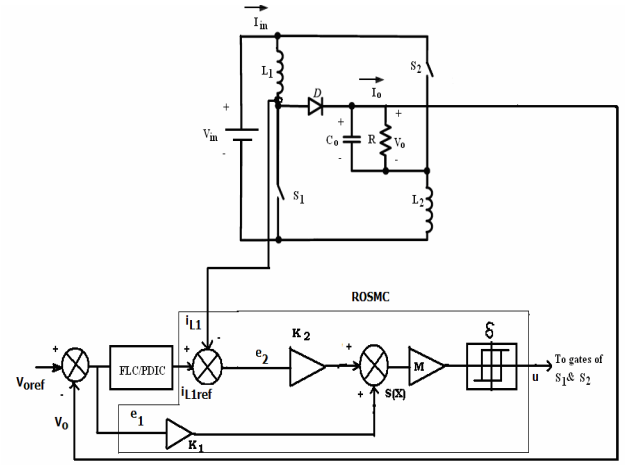
$$C_0 = \frac{V_0}{2R\Delta V_0 f}, C_0 = \frac{48}{2 \times 50 \times 0.16 \times 100e^3} = 300\mu F \tag{13}$$

The design specifications are substituted in equation (6) and after utilizing the phase-variable transformation, the system matrices become

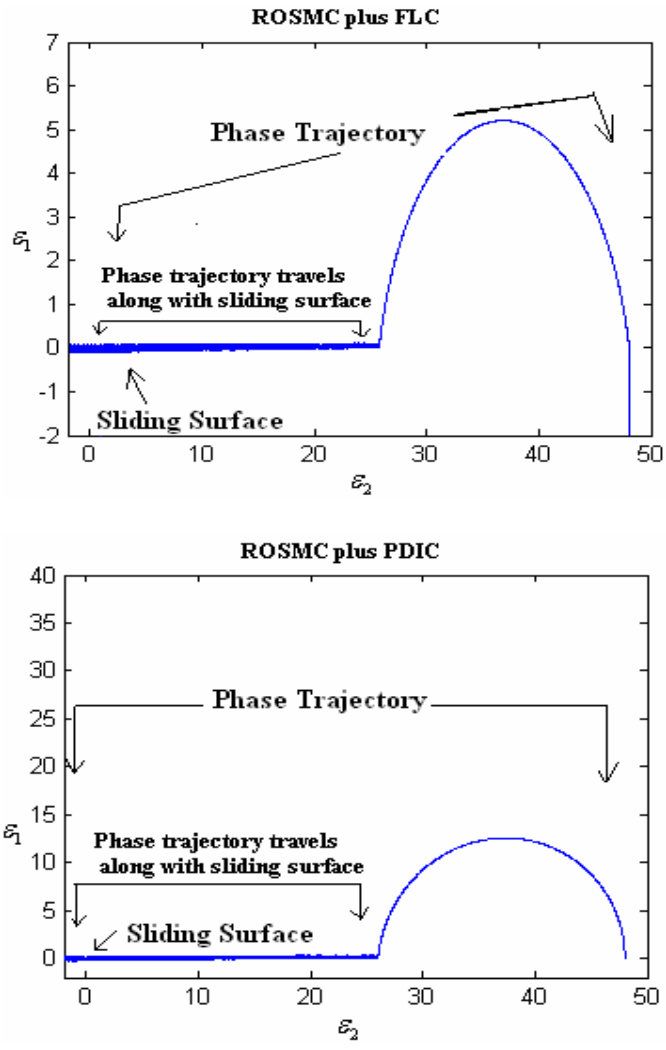
$$A = \begin{bmatrix} 0 & -2000 \\ 1333.34 & 13.34 \end{bmatrix}, B = \begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{14}$$

3 Design of control techniques

The main objective of this section is to argue about the developed controller for the POESITBC. The ROSMC plus FLC and ROSM plus PDIC scheme for a POESITBC is exposed in Fig. 2 (a). The controller is divided into two loops specifically, an inner current loop which uses ROSMC for regulate the inductor current, and an outer voltage control loop applying the FLC, and



(a)



(b)

Fig. 2 Development of ROSMC, (a) control scheme for POESITBC using ROSMC plus FLC/PDIC, (b) simulation result of region of existence of SM in the phase plane of POESITBC using ROSMC plus FLC and ROSMC plus PDIC.

the PDIC to control the output voltage and also, to reduce the steady state error of the converter. The input to the FLC and PDIC is the output voltage error and the output locates the average reference inductor current for inner loop. The inputs to the ROSMC are output voltage error e_1 and the current error e_2. The output of ROSMC u is the control signal, which in turn sets the new duty ratio of the switching pulse for driving the power MOSFET switches of the POESITBC.

3.1 Design of ROSMC

With help of the phase-variable transformation to signify the POESITBC, whereas fixing the sliding surface $\sigma(\varepsilon,t)$, the model of the POESITBC in phase-variable form is written as equation (15)

$$\dot{X} = AX + Bu \tag{15}$$

Where,

$$A=\begin{bmatrix} 0 & -2000 \\ 1333.34 & 13.34 \end{bmatrix}, B=\begin{bmatrix} 0 \\ 1 \end{bmatrix} \tag{16}$$

The switching surface of the converter is expressed as equations (17) and (18)

$$\sigma = N_1\varepsilon_1 + N_2\varepsilon_2 \tag{17}$$

$$\sigma(X) = X_1 + N_1\ X_2 \tag{18}$$

Where, ε_1 and ε_2 are the errors of the converter and it can be written as equation (19)

$$\varepsilon_1 = \left[i_{L1ref} - i_{L1} \right],\ \varepsilon_2 = \left[V_{oref} - V_o \right] \tag{19}$$

The tracking vector of the POESITBC is expressed as equation (20)

$$\sigma(\varepsilon,t) = [N][\varepsilon] \tag{20}$$

The error vector in the sliding surface is always to keep for all the time $\sigma(\varepsilon,t)=0$ and in addition the controller co-efficient vectors $N=\left[N_1\ N_2\right]$ and $N_1,\ N_2 \rangle 0$

$$\dot{\sigma}(\varepsilon,t) = [N][\dot{\varepsilon}] = 0 \tag{21}$$

The sliding surface of the second order converter is reduced into get the first order model through the differential equations and it can be written as equation (22)

$$\begin{aligned} \dot{\varepsilon} &= \dot{H} - \dot{X} \\ \dot{\varepsilon} &= \dot{H} - AX + Bu \end{aligned} \tag{22}$$

Substituting (A), $X = H - \varepsilon$ in (22) and Filippov's equivalent switch control u_{eq} that guarantees the $\dot{\sigma}(\varepsilon,t)=0$ and it can be represented as equation (23)

$$\dot{\sigma} = N\varepsilon = [N]\left[\dot{H} - AH + A\varepsilon - Bu_{eq} \right] = 0 \tag{23}$$

The converter control signal is evaluated using the equation (23) and it will be expressed as equation (24)

$$u_{eq} = [NB]^{-1} N\left[\dot{H} - AH + A\varepsilon \right] \tag{24}$$

By Substituting equation (24) in equation (22)

$$\dot{\varepsilon} = \dot{H} - AH + A\varepsilon - B(NB)^{-1} N\left[\dot{H} - AH + A\varepsilon \right] \tag{25}$$

$$\dot{\varepsilon} = \left[I - B(NB)^{-1} N \right]\left[\dot{H} - AH + A\varepsilon \right] \tag{26}$$

Substituting $\left[\dot{H} - AH \right] = 0$ (invariance conditions) in equation (26) the expression has been simplified as

$$\dot{\varepsilon} = \left[I - B(NB)^{-1} N \right] A\varepsilon = A_{eq}\varepsilon \tag{27}$$

If $(NB)^{-1}$ exists, the vector N is derived by choosing the eigen values of A_{eq} such that it guarantees the asymptotic convergence of error to zero at the desired value. The matrix A_{eq} is selected to satisfy equation (27) and it is expressed as

$$A_{eq} = \begin{bmatrix} -2.065 & 0 \\ 0 & -1 \end{bmatrix} \tag{28}$$

The values of matrix *N* is then found using equation (27) as

$$N = \left[N_1\ N_2 \right] = [1 \quad 2.065] \tag{29}$$

Thus, the sliding manifold σ is given by

$$\sigma = N_1\varepsilon_1 + N_2\varepsilon_2 \tag{30}$$

Equation (30) indicates that if the POESITBC operates in equilibrium mode (when σ = 0, stability condition), the dynamics of errors ε_1 and ε_2 be possible exponentially to zero with a time constant ratio of N_1/N_2. Even as in the step transient's period, the POESITBC is in reaching mode, and as a result for this exploit N_1 and N_2 are evaluated to be in 1 and 2.065, respectively. In addition, the equation (18) describes the error action under ROSMC. Once the sliding surface σ (ε , t) = N ε is designed then the control law for hitting condition is defined as

$$\begin{aligned} u &= M\ sgn(\sigma)x_2 \\ &= Ux_2 \end{aligned} \tag{31}$$

Where,

$$\begin{aligned} U &= 1 \quad for\ \sigma > \delta \\ U &= 0 \quad for\ \sigma < \delta\ . \end{aligned}$$

(U = 1 when the switch is the conduction subinterval, and U = 0 when the diode is the conduction subinterval).

In this case, hysteresis bandwidth δ = 0.05 is selected by trial and error iterative method (based on the system performance). Equation (31) is used to derive the gate pulse to drive power MOSFETs of converter, which in turn control dc output voltage, steady state error and inductor current. In this study, M is constant number and equal to unity so that $\sigma\dot{\sigma} < 0$ (existence condition is fulfilled). The reaching condition guarantees that the tracking error phase trajectory is asymptotically involved to σ = 0 (stability condition). It is showed that the (31) does not depend on the working regions, system parameters and limited disturbances. This is achieved as long as the control input u is more enough to maintain the converter subsystem in sliding mode.

$$\sigma(X) = X_1 + N_2 X_2 \tag{32}$$

Where, $N^T = [1, N_2]$ is the vector of sliding surface coefficients which correspond to K in equation (23)

$$\dot{\sigma}(X) = \begin{cases} N^{\mathrm{T}}AX + N^{\mathrm{T}}BU^{+} + C^{\mathrm{T}}D, & \text{for}\ \sigma(X) > 0 \\ N^{\mathrm{T}}AX + N^{\mathrm{T}}BU^{+} + C^{\mathrm{T}}D, & \text{for}\ \sigma(X) < 0 \end{cases} \tag{33}$$

Then, substituting the values of A, B, and N, the above equation can be expressed by

$$\begin{aligned} S(X_1) &= 1333.34N_2X_1 - 2000N_1X_1 + 13.34N_2X_2 \\ S(X_2) &= 1333.34N_2X_1 - 2000N_1X_1 + 13.34N_2X_2 + N_2 \end{aligned} \tag{34}$$

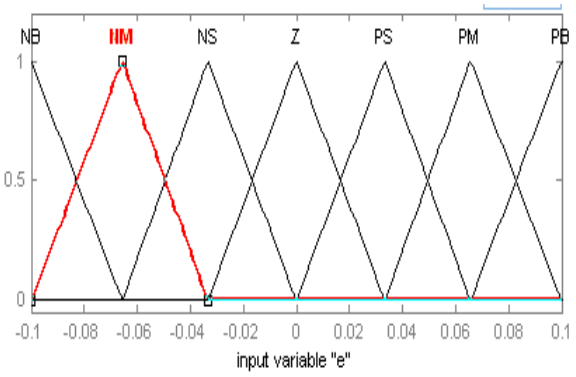
Equations $\sigma_1(X) = 0$ and $\sigma_2(X) = 0$ define two lines in the state plane with the same slope passing through the origin. These equations represent the sliding surface for switch ON/OFF states conditions, which are inadequate to single the sliding surface of a given converter with ROSMC plus FLC/PDIC for N_1, N_2 is shown in Fig. 2 (b). From this phase trajectory, it is evidently observed that the suitable value of N_2 controls the dynamic response of the system competently. Once the phase trajectory is on top of the sliding surface, the switch is turned off state (U= 0) and when the phase trajectory is lower the sliding surface, the switch is turned on state (U=1). Also, from the Fig. 2 (b) indicated that overshoots in the phase trajectory of the converter using the ROSMC plus FLC has small as compared to the ROSMC plus PDIC.

3.2 Design of PDIC

A PDIC is chosen for providing the good output voltage regulation for POESITBC (refer the Fig. 2(a)). In this case, the PDIC output sets the average reference inductor current for inner current loop. The PDIC parameters, proportional gain (K_p) and double integral times (T_is), are evaluated using Zeigler – Nichols tuning method. The PDIC parameters, proportional gain (K_p) and double integral times (T_is), are obtained by using Zeigler–Nichols tuning method [15-18]. After the tuning the controller using this method, the POESITBC is providing a sustained oscillation with ultimate gain for stability can be found by K_{cr}=0.2 and their corresponding ultimate period P_{cr}=0.2s. Using this method the values of $K_p = K_{cr}/2$=0.1 and integral times $T_i s = P_{cr}/1.2$=0.167s and 0.16s (this value is selected based on the system response) are determined.

3.3 Design of fuzzy logic controller

Here, the FLC is included as a outer loop, which is used to control the power switches of the POESITBC. The inputs and output of the FLC is shown in Fig. 3 (a) to (c). The voltage error (e) and its change in error (de) of this converter is applied as



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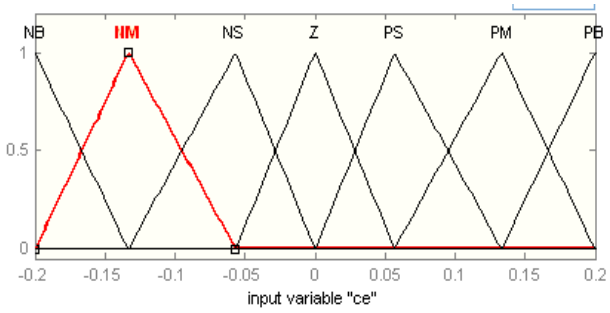

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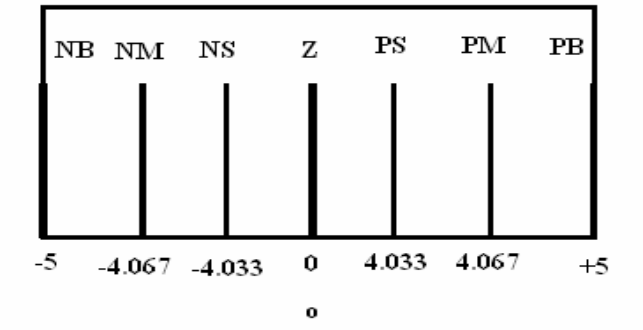


(c)

Fig. 3 Membership's functions of FLC, (a) error (e), (b) change in error (ce), and (c) output (o)

a input the FLC and the output is o (mark the reference current for the inductor). For expediency, the numerical ranges of the inputs/output of the FLC can be standardized and expressed as follows: e = [-0.1 -0.06 -0.034 0 0.034 0.06 0.1], ce = [-0.2 -0.14 -0.06 0 0.06 0.14 0.2] and o = [-5 -4.067 -4.033 0 4.033 4.067 5] and its corresponding fuzzy sets are [NB, NM, NS, Z, PS, PM, PB] where, NB (negative big), NS (negative small), Z (zero), PS (positive small), PM (positive medium), PB (positive big), respectively. The membership functions of the e, ce, and o are indicated in Fig. 3. The selection of FLC rules is entirely based on the performance behaviour of the converter. In this study, 49 rules are framed (refer the Table 1). Then, the weighted average method (defuzzification-method) is applied to complete the fuzzy work.

Table 1. Fuzzy rule base table of POESITBC

CE \ E	NB	NM	NS	Z	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NM	NM	NM	NS	Z	PS
NS	NB	NM	NS	NS	Z	PS	PM
Z	NB	NM	NS	Z	PS	PM	PB
PS	NM	NS	Z	PS	PS	PM	PB
PM	NS	Z	PS	PM	PM	PM	PB
PB	Z	PS	PM	PB	PB	PB	PB

Output (o) : NB=-5; NM= -4.067; NS= -4.033; Z=0; PB=5; PM= 4.067; PS= 4.033

4 Simulation results and discussions

The main purpose of this section is to discuss about the simulation results of the POESITBC with designed control schemes. A ROSMC plus PDIC is used for comparison with the designed ROSMC plus FLC. The validation of the system performance is done for different conditions. The MATLAB/Simulink simulation model is performed on the POESITBC circuits with specifications listed in section 2.2.

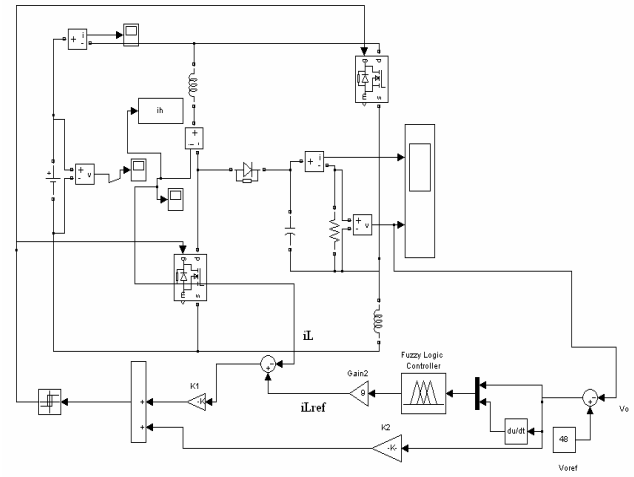


Fig. 4 MATLAB/Simulink model of the POTLSITBC using a ROSMC plus FLC

The parameters of the controller are: N_1 =1, $\mathbf{N}_2$ = 2.065, δ=0.05, K_p =0.1 and T_is = 0.167s and 0.16 as calculated in the previous section. The designed ROSMC plus FLC/PDIC is implemented in MATLAB/Simulink software platform as shown in Fig. 4 and its operation (refer the section 3).

4.1 Start-up transient

Fig. 5 shows the dynamic behaviour in terms of the output voltage start-up of the POESITBC for input voltage 12V using the ROSMC plus FLC and ROSMC plus PDIC. It can be seen that output voltage of the POESITBC has a negligible overshoot and settling time of 0.0015s (ROSMC plus FLC), and 0.004s (ROSMC plus PDIC) for V_{in} = 12V.

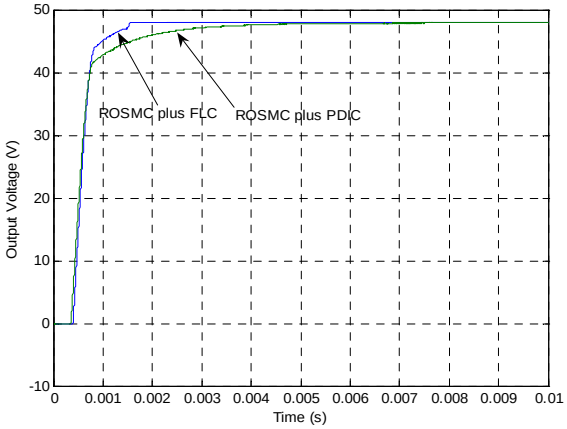
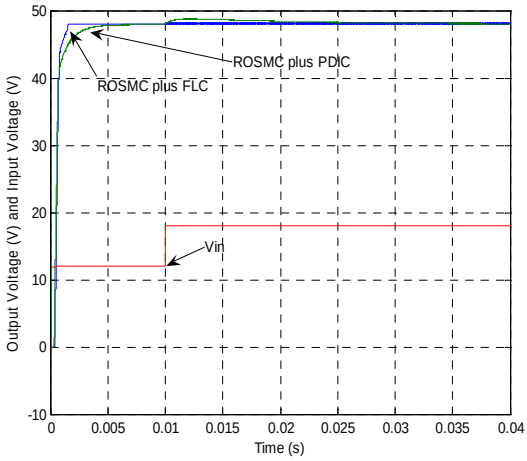
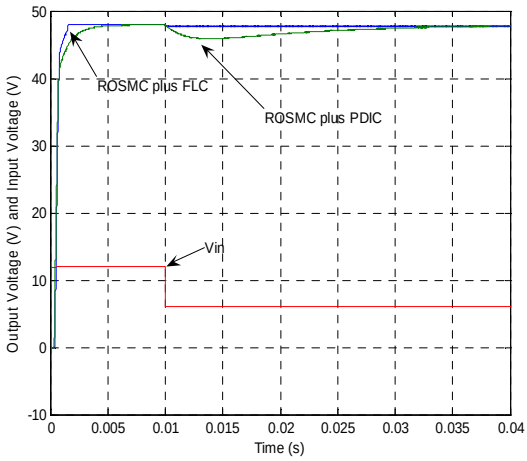


Fig. 5 Simulated startup response of output voltage of the POTLSITBC using ROSMC plus FLC and ROSMC plus PDIC

4.2 Line variation



(a)

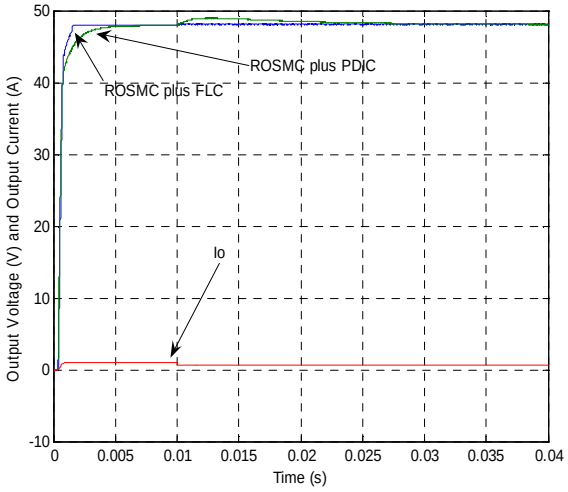


(b)

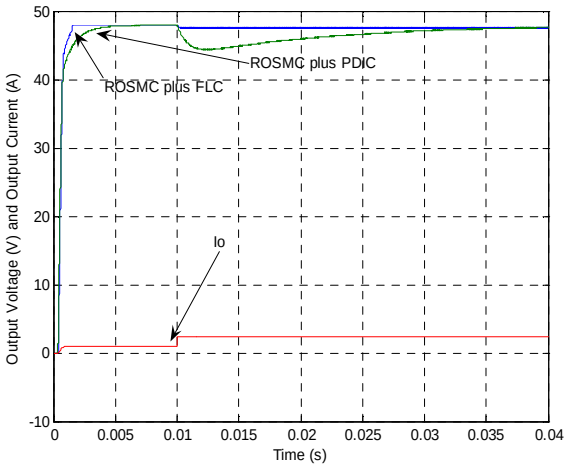
Fig. 6 Simulation responses of the output voltage of the POESITBC using designed controllers, (a) for input step change from 12V to 18V at time of 0.01s with R = 50Ω, and (b) for input step change from 12 to 06V at time of 0.01s with R = 50Ω

Figs. 6 (a) and (b) show the simulation response of output voltage of the POESITBC using ROSMC plus FLC and ROSMC plus PDIC for input voltage step change from 12V to 18V and 12V to 04V at time of 0.01s. From these figures, it is clearly found that the POESITBC using ROSMC plus FLC (negligible overshoots as well as settling time) has excellent dynamic performance in comparison with ROSMC plus PDIC (overshoots = 1V and settling time =0.02s) at line variation

4.3 Load variation



(a)

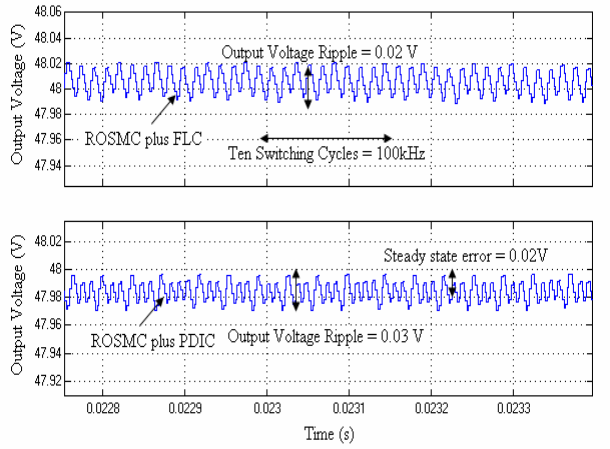


(b)

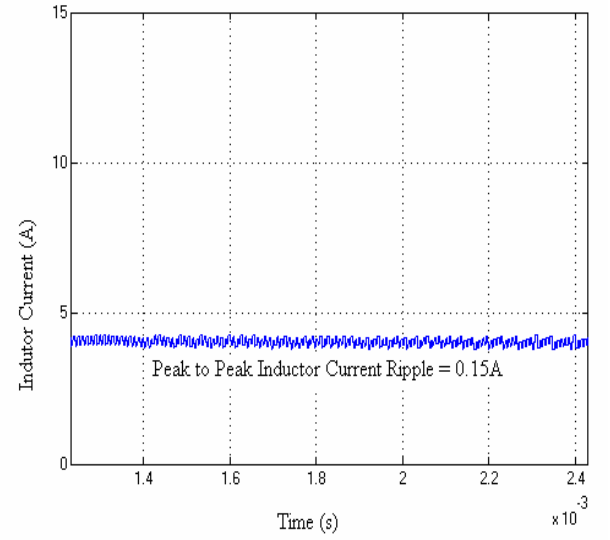
Fig. 7 Simulation responses of output voltage of POESITBC using designed controller, (a) when load value takes a step changes from 50 Ω to 80Ω at time 0.01s with V_{in}=12V, and (b) when load value takes a step changes from 50Ω to 20Ω at time 0.01s with V_{in} =12V

Fig.7(a) and Fig.7(b) show the simulation response of output voltage of the POESITBC using a ROSMC plus FLC and ROSMC plus PDIC for load step change 50Ω to 80Ω and 50Ω to 20Ω at time = 0.01s. It could be seen that the simulation results of output voltage of the POESITBC using a ROSMC plus FLC has a negligible overshoot and settling time, whereas the output voltage using ROSMC plus PDIC has produced maximum overshoots of 1.2V and settling time of 0.02s.

4.4 Steady state region



(a)



(b)

Fig. 8 Simulated responses of the POESITBC using the designed controller in steady state condition, (a) output voltage, and (b) inductor current

Fig. 8 (a) and (b) shows the simulation output voltage and the inductor current of the POESITBC in the steady state region using a ROSMC plus FLC and ROSMC plus PDIC. It is obvious from the figure that the output voltage ripple is very small about 0.02V, negligible steady state error (ROSMC plus FLC)/0.03V (ROSMC plus PDIC) and the peak to peak inductor ripple current is 0.15A for the average switching frequency of 100kHz closer to theoretical designed value listed (refer the section 2.2) and also it indicate that to keep the inductor current for the converter always continuous. Fig. 9

shows the graphs of the steady-state output voltage against the switching frequency of the POESITBC under the ROSMC plus FLC and ROSMC plus PDIC respectively for the rated load condition. From this figures, it is clearly found that the ROSMC plus FLC reduces the steady-state error regulation for all values of switching frequency in comparison with ROSMC plus PDIC.

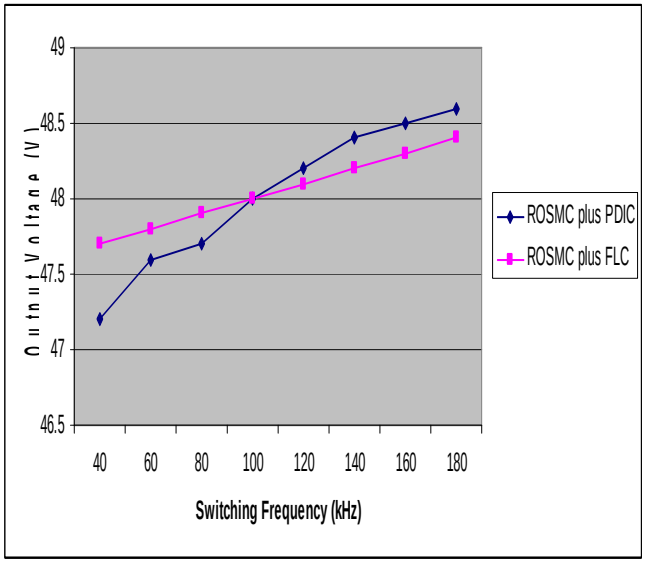
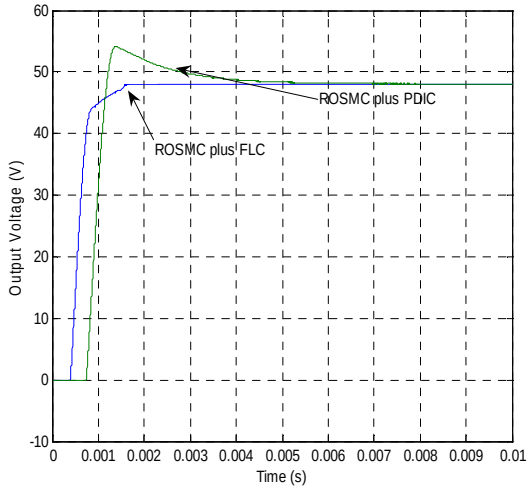


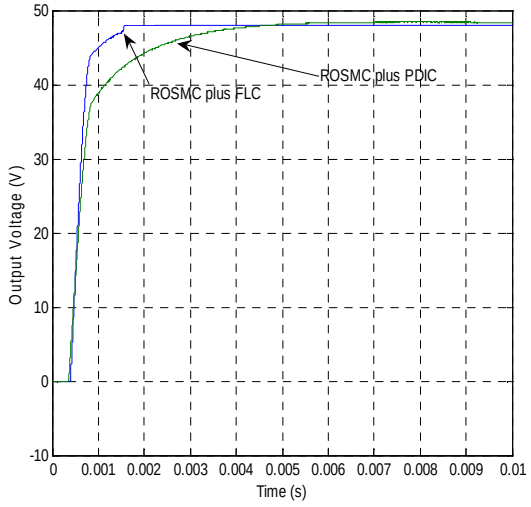
Fig. 9 Simulated graphical form of steady-state output voltage of the POESITBC against switching frequency with the ROSMC plus FLC ROSMC plus PDIC and ROSMC plus PIC at rated condition

4.5 Circuit components variations

Fig. 10(a) represents the simulation response of output voltage of the POESITBC using a both controllers for inductor L_1 variation from 100µH to 200µH. It could be found that the change does not influence the POESITBC behaviours due to a proficient ROSMC plus FLC. An interesting result is illustrated in Fig. 10(b). It shows the simulation response of output voltage of the same converter with a both the controllers for the variation in capacitors values from 300µF to 400µF. It can be seen that the proposed ROSMC plus FLC is very successful in suppressing effect of capacitance variation in comparison with ROSMC plus PDIC. Fig. 11(a) indicates the graphical form of simulation results of % efficiency of the converter using a ROSMC plus FLC at various load conditions. From this figure, it is clearly found that the % efficiency of the POESITBC using a ROSMC plus FLC has maintained from 92.5 % to 93.6 % at various load conditions. Fig. 11 (b) show the graphical results of simulated output voltage of the POESITBC using ROSMC plus FLC and ROSMC plus PDIC for varying input voltage range from 2V to 20V. From this figure, it is clearly showed that output voltage deviation is 0.1 V (ROSMC plus FLC) for whole input voltage variation. Finally, the designed ROSMC plus FLC performed well in the entire operating situation of the POESITBC.

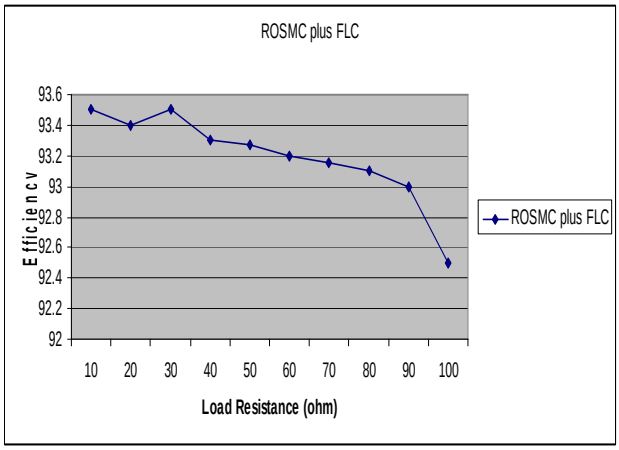


(a)

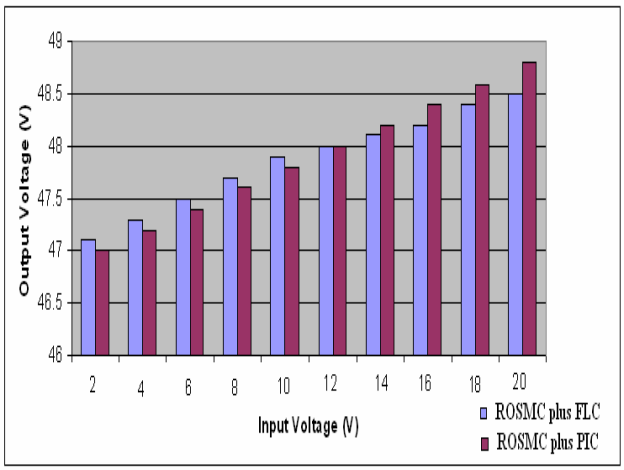


(b)

Fig. 10 Circuit components variations of POESITBC, (a) response of output voltage when inductor variation from 100µH to 200µH using both controller schemes, and (b) response of output voltage when inductor variation from 300µF to 400µF using both controller schemes.



(a)



(b)

Fig. 11 Perofomance of POESITBC using deiigned controller is expressed in graphical representation, (a) simulated results of % efficiency at various load conditions, and (b) graphical simulated output voltage results at diferent input voltage

5 Conclusion

In this article, theoretical analysis, design and output voltage regulation of the POESITBC operated in CCM using a variable frequency based ROSMC plus FLC and ROSMC plus PDIC has been successfully demonstrated through the computer simulation using MATLAB/Simulink. The simulation results are proved that the designed ROSMC plus FLC has excellent performance at different working conditions over the ROSMC plus PDIC. It is fit for low power applications like LED TV, mobile phones, robot systems and medical equipments.

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