Grid Synchronization in a 3-Phase Inverter using Double Integration Method

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Abstract: - Distributed renewable energy sources (DRESs) have additional benefits compared with conventional fossil fuel-based energy sources. These sources are connected to the utility grid using a suitable synchronization method. It requires accurate information on grid voltage magnitude and phase angle. But the presence of harmonics, DC Offset, and voltage unbalances makes the synchronization process more challenging. Conventionally synchronous reference frame (SRF)- PLL is implemented for this purpose, however, it has a problem with 100Hz ripple during distorted grid conditions. A double integration method (DIM) is administered for the synchronization of a 3-phase inverter under non-ideal grid conditions. It is important for DIM implementation to remove the DC offset or integrating constants of pure integrators without involving any phase shift. This method is also compared with conventional SRF-PLL based on mathematical modelling and simulations using a MATLAB/Simulink toolbox. The results are verified based on ideal and non–ideal grid conditions and also tested on grid-connected 3-phase Inverter.

Key-Words: - Double Integration Method, PLL, Pulse width Modulation, grid Synchronization, Inverter,Harmonics.

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1 Introduction

Due to the expansion in consumption of electrical power, the generation of electricity needs to be increased. Therefore, the demand for renewable energy sources such as solar, and wind also get multiplied, [1]. These sources are environment-friendly, pollution free, and distributed in nature, [2]. These DRESs are connected to grid using parallel inverters. To achieve parallel operation, of inverters, its parameters; a) voltage magnitude b) phase c) frequency must be synchronized to grid parameters, [3]. An increase in network diversity and connection of various types of DS makes the synchronization process more challenging. As grid voltage contains disturbances like DC Offset and harmonics its waveforms are distorted and the synchronization process is also affected, [4]. Many synchronization techniques are discussed in the literature. These techniques can be categorized as; a) open-loop b) closed-loop. A feedback mechanism is required in a closed loop system while an open loop has no feedback involved but filtering is needed for the extraction of required parameters, [5], [6]. A brief description of these techniques is shown in Figure 1, [7]. These methods include zero crossing detector (ZCD) [8], discrete Fourier transform (DFT) [9], adaptive notch filtering (ANF) [10], Phase locked loop (PLL) [11] and Kalman filter

[12]. There are several performance parameters detected from the literature including; unbalanced conditions, harmonics, DC offsets, phase angle adjustment, and accuracy during the signal synchronization process. A band pass filter is used to remove the DC offset, but it initiates a phase shift as frequency deviates, [13]. Second-order integrator (SOG) PLL is proposed to remove DC components in a single-phase system, [14]. A de-coupled double synchronous reference frame (DDSRF-PLL) is proposed for the grid synchronization during non-ideal grid conditions but problems of the DC-off set is not solved. The SRF-PLL technique is sensitive to grid voltage unbalanced waveforms and also has a 100 Hz problem, [15]. An enhanced-PLL (E-PLL) and dual-EPLL (DE-PLL) methods are developed for solving grid voltage disturbances but these techniques can be affected by harmonics, [16], [17]. The moving average filter (MAF) is used in the structure of SRF-PL to counter-unbalance and harmonic in the voltage signals. However, it has a long settling time and oscillations, [18]. The multi-complex co-efficient filter (MCCF) is implemented to extract harmonic components and to eliminate negative sequence components but multiple filter modules are used that increases the computational burden, [19]. A solar PV-based 3-phase grid connected Inverter using double integration is proposed in [20], that considered steady state conditions only.

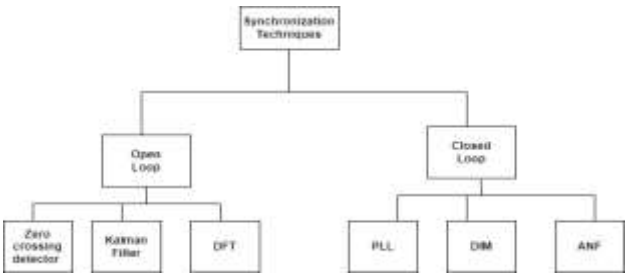


Fig. 1: Synchronization techniques

The key contribution of this paper is to propose the DIM method in a 3-phase grid tied Inverter under distorted grid conditions. In this paper ,current amplitude is corrected using gain values of the controllers to adjust the amplitude of current .To mitigate harmonics additional filters are not needed during non-ideal grid conditions using the proposed method, since the generated signal remains in phase with the current.The DIM method recovers naturally from transients, as nonlinear feedback always remains active.It only synchronizes giving a current or voltage reference. Therefore the proposed method works well during non-ideal grid conditions. A PI in the feedback will result in a high pass filter. The low pass will make it a compensator integrating low and high frequencies,

2 Modelling of Synchronization Techniques

The SRF-PLL and DIM techniques are further discussed in this section

2.1 SRF-PLL

The input to SRF-PLL is the grid's three-phase voltages and the output is phase angle and frequency, V_d and V_q are the d-axis and q-axis components as shown in Figure 2. The d-axis corresponds to the amplitude of the voltage signal and q-axis corresponds to phase angle information of any one of the phases. This structure of PLL is called Synchronous Reference Frame (SRF- PLL) or d-q PLL. The phase angle $\boldsymbol{\theta}$ makes a feedback loop; the proportional integral (PI) controller is in a forward path to secure the d-axis component $\boldsymbol{V_d = 0}$ .It will also ensure grid voltage vector is perfectly aligned with the q-axis component, [21].

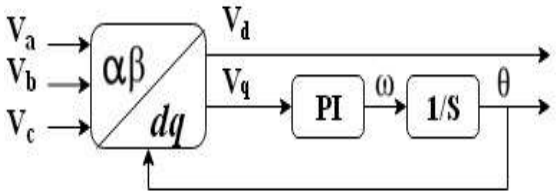


Fig. 2: Basic structure of SRF- PLL

2.2 Double Integration Method (DIM)

DIM is synchronization technique without involving the extraction of grid voltage phase angle or frequency. It is a strategy for fixing the reference value (voltage or current) over time as shown in equation (1), [22].

$$V_{ref} = \iint V_t dt^2 \quad (1)$$

Where V_t grid voltage and requirement is to remove DC constant of integration.

Let's consider the grid voltage in equation (2)

$$\mathrm{V} = V_m \mathrm{Sin}(\omega * t) \quad (2)$$

Now taking double integration of equation (2) can be expressed as

$$\mathrm{V} = -V_m \frac{1}{\omega^2} \mathrm{Sin}(\omega * \mathrm{t}) + \mathrm{C} \quad (3)$$

where C denotes the integrating constant. In a pure sine wave signal, double integration produces a phase shift of 180 degrees. Therefore, it can be

applied to synchronize grid voltage or grid current. A block diagram of single-phase digital DIM is shown in Figure 3.

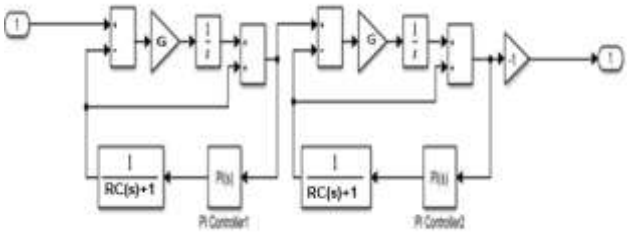


Fig. 3: Single-phase DIM

A PI compensator is designed as non-linear feedback to remove DC offsets at each integrator. During steady-state conditions, there will be no interaction of the feedback and it only acts when DC offset or distortion occurs.Since voltage has an upper limit and frequency has a lower limit. The integrals can be clamped for + and - afterwards, the average can be tuned to zero.There will be a shift in phase using a high pass filter.In steady state conditions, there will be no interaction of the feedback, as then the phase is exactly 180 even if the frequency changes.

The low pass filter RC value is selected as 0.0031 for the cut-off frequency around 50 Hz. The kp and ki values of DIM are selected as 0.1803967 and 1.821326 respectively to give a phase margin of 53° degrees to make this system stable. The low pass filter RC+1 value is opted as 0.0031 to cut off frequency around 50 Hz. The DIM provides no phase shift as frequency changes but amplitude can change. Unlike, [22], current amplitude is corrected using gain values of controllers in a digital circuit. In references [23] and [24], grid synchronization and dc offset problem is solved without considering distorted grid conditions.A comparison between different Grid synchronization techniques and the proposed technique is given in Table 1.

Table 1. Comparision

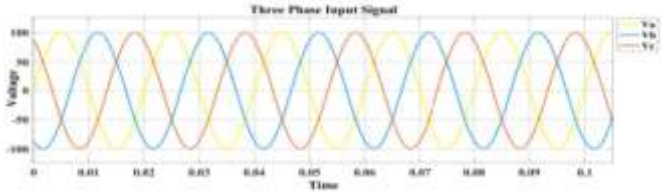
References	PLL	DIM	DC-Offset removal	grid synchronization	grid distorted conditions
20	-	✔	✔	✔	-
21	✔	-	✔	✔	-
23	✔	-	✔	✔	-
24	✔	-	✔	✔	-
proposed	-	✔	✔	✔	✔

3 Simulation Results

The SRF-PLL and DIM are simulated and compared during normal and distorted grid conditions.

3.1 Ideal Grid Conditions

Figure 4(a-g), shows the simulation results of SRF-PLL and DISM during ideal grid conditions. Figure 4(a) shows the 3-phase balanced input signal. Figure 4(b-f) shows the output of PLL synchronized with the input signal, the phase angle of SRF-PLL, frequency error signal, and FFT analysis of SRF-PLL and DIM method. Figure 4(g) shows the output of DIM synchronized with input signal at t= 0.005s.



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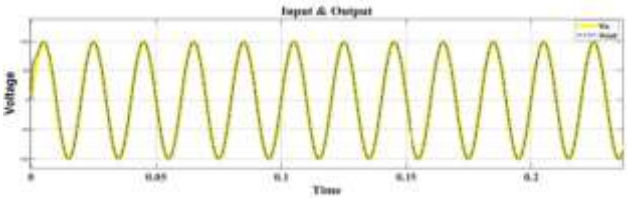

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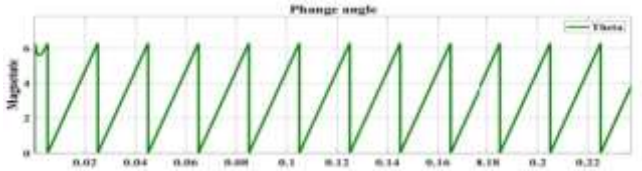

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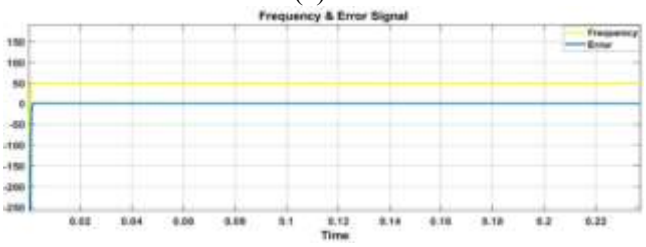

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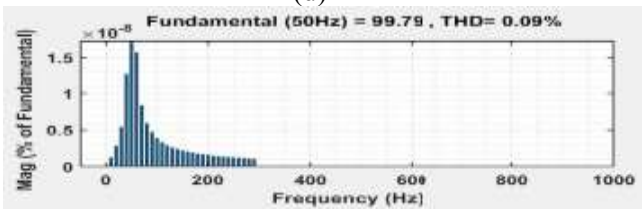

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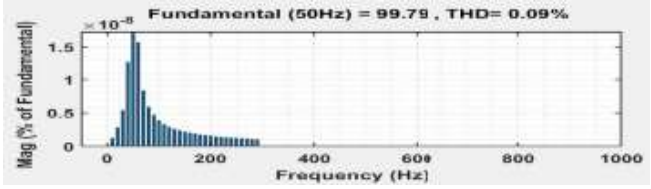

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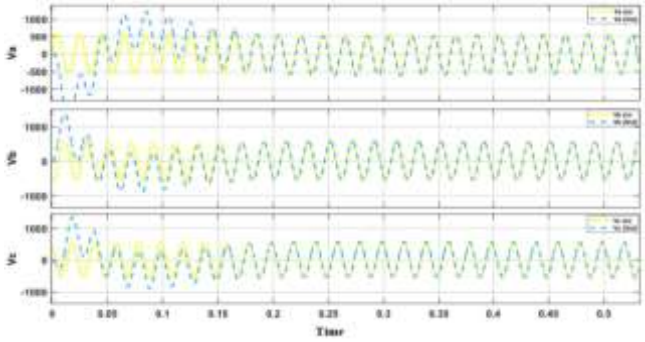


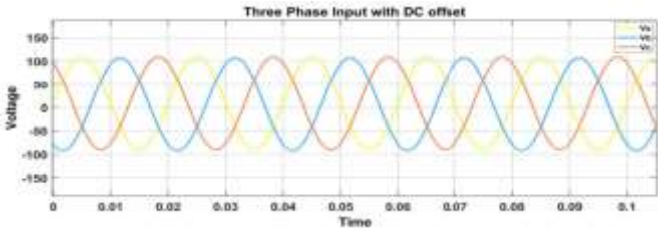
(g)

Fig. 4: SRF-PLL and DIM during Ideal Condition. (a) Input signal. (b) Input & Output SRF- PLL. (c) Phase angle SRF-PLL. (d) frequency and error signal of SRF- PLL. (e) Input FFT analysis SRF-PLL. (f) Output FFT analysis SRF-PLL. (g) Input and Output DIM

3.2 Distorted Grid Conditions

The following distorted conditions with input signal are simulated a) DC offset; b) harmonics; c) voltage unbalance; d) frequency unbalances.

Figure 5(a-h), indicates the simulation results of SRF-PLL and DISM during non ideal conditions. The 10, 8, and 10 % DC offset values are injected in 3- 3-phasevoltages Va, Vb, and Vc respectively. Figure 5(a) indicates the 3-phase DC offset input signal. Figure 5(b-f) shows the output of PLL synchronized with the input DC offset signal, phase angle of PLL, frequency error signal, and FFT analysis of input and output PLL. The Figure 5(g-h) shows output of DIM synchronized with input signal having DC offset at t= 0.005s and FFT analysis gives its THD value of 0.02%.



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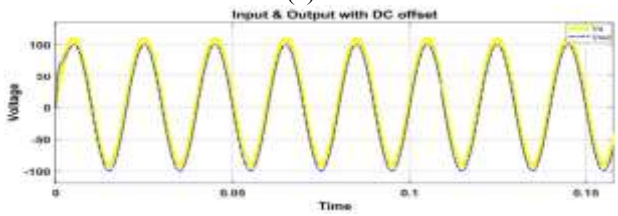

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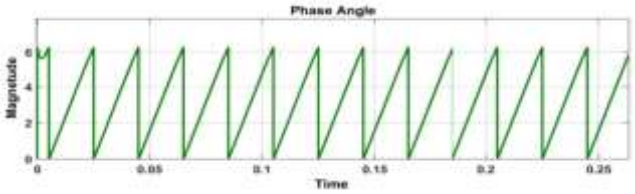

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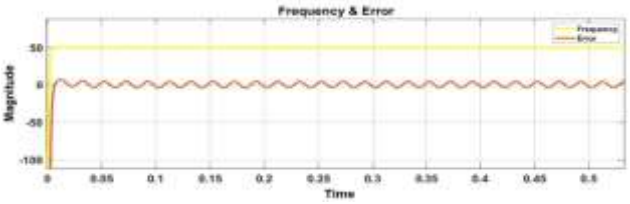

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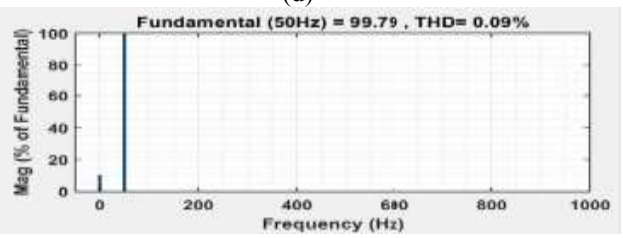

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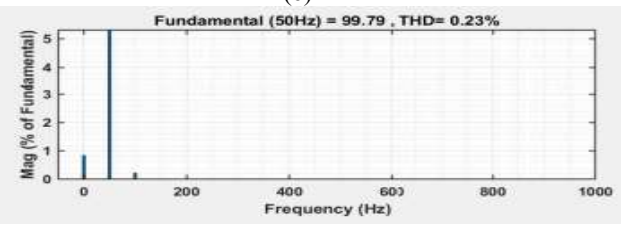

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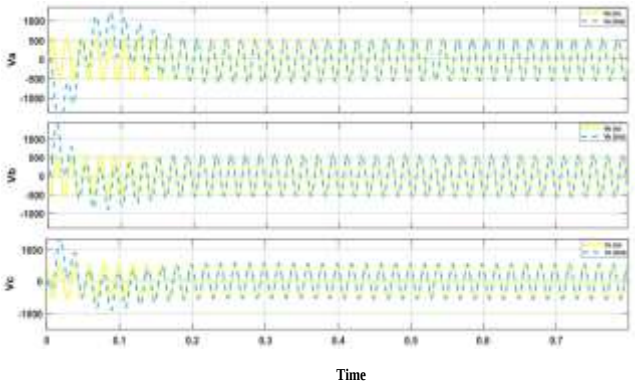

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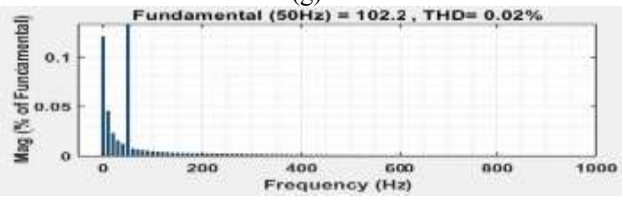
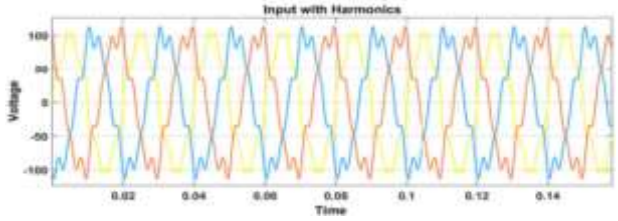


(h)

Fig. 5: SRF-PLL and DIM DC offset. (a) Input of PLL. (b) Input & Output of PLL. (c) phase Angle of PLL. (d) frequency and error signal of PLL. (e) Input FFT analysis of PLL. (f) Output FFT analysis of PLL. (g) Input & Output of DIM. (h) Output FFT analysis DIM

Conventional SRF-.PLL does not perform well during harmonics and an additional filter is required at the cost of time delay or slow response. The input signal with 5th, 7th, and 11th harmonics is added with 0.1, 0.08, and 0.05 % of Vm respectively. Figure 6(a-h), shows the simulation results of SRF-PLL and DISM with harmonics in input signal. Figure 6(a) shows a 3-phase input signal with 5th, 7th, and 11th harmonics in it. Figure 6(b-f) shows the output of SRF-PLL synchronize with 5th, 7th and 11th harmonics in the input, phase angle of SRF-PLL, frequency error signal and FFT analysis of input and output PLL. Figure 6(g-h) shows output of DIM synchronized with input DC offset signal at t= 0.005s and FFT analysis gives its THD value of 0.28%.



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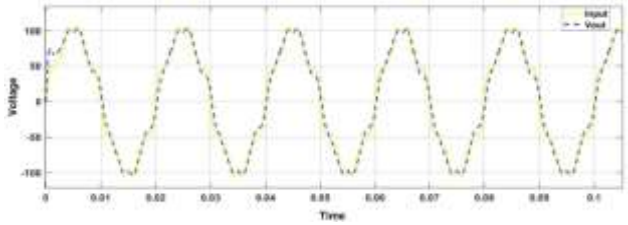

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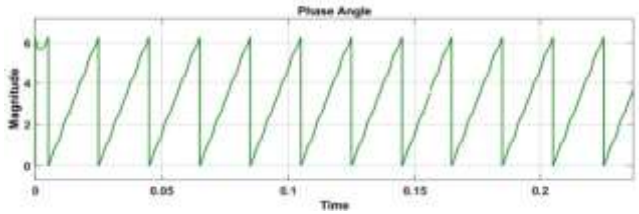

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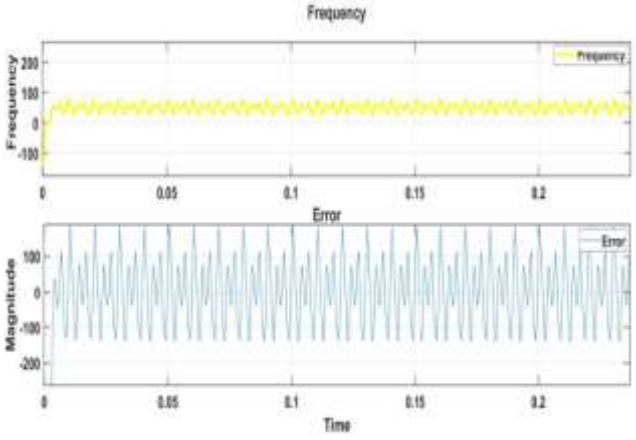

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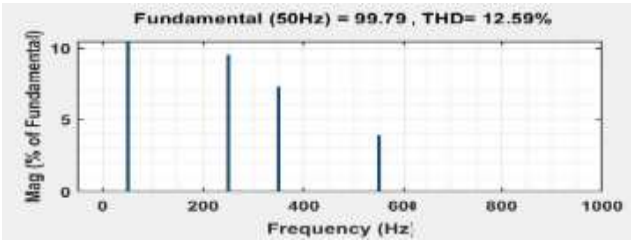

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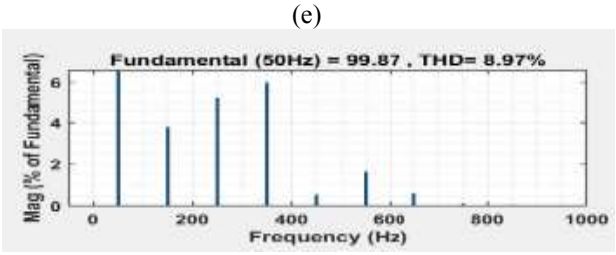

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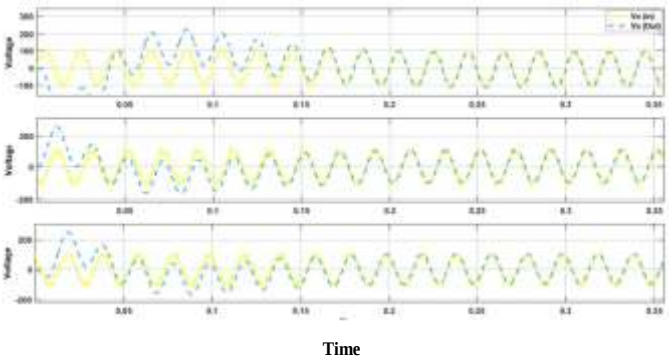

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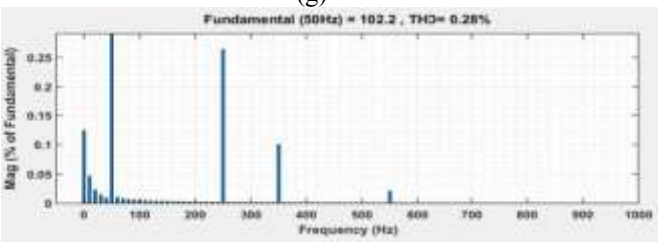
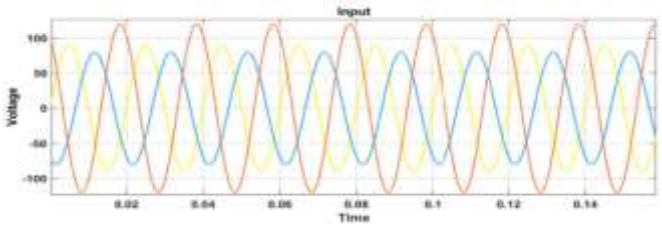


(h)

Fig. 6: SRF-PLL and DIM with Harmonics injection. (a) Input of PLL. (b) Input and output SRF-PLL. (c) Phase angle SRF-PLL. (d) frequency and error signal SRF-PLL (e) Input FFT analysis SRF-PLL. (f) Output FFT analysis SRF-PLL. (g) Input and output DIM. (h) Output FFT analysis DIM

The 3-phase input signal is included with voltage unbalances with voltage magnitudes of 0.9, 0.8 and 1.2 % of Vm phase voltage. Figure 7(a-h), shows the simulation results of SRF-PLL and DISM with voltages unbalances in input signal as shown in Figure 7(a) Whereas, Figure 7(b-f) shows the output of PLL synchronize with the input phase voltage unbalance signal, phase angle of PLL, frequency error signal and FFT analysis of input and output of PLL. The Figure 7(g-h) shows the output of DIM synchronized with input signal with

voltages unbalance at t= 0.005s and FFT analysis gives THD value of 0.02%.



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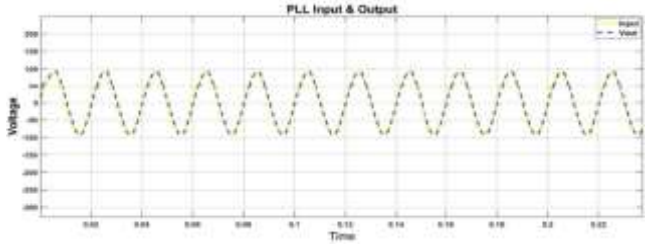

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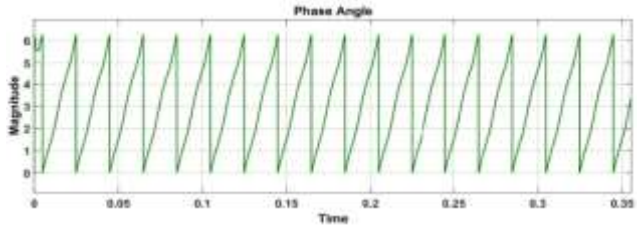

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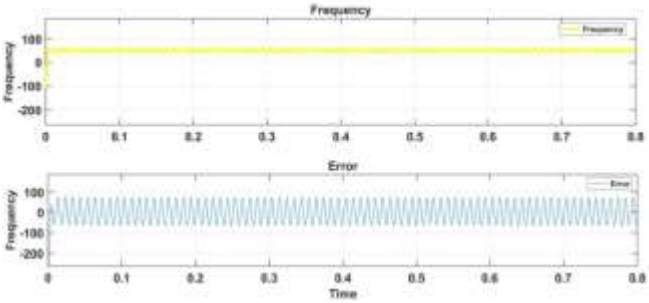

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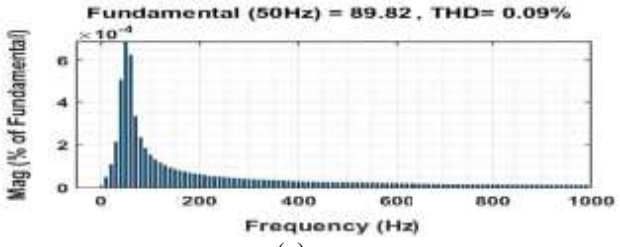

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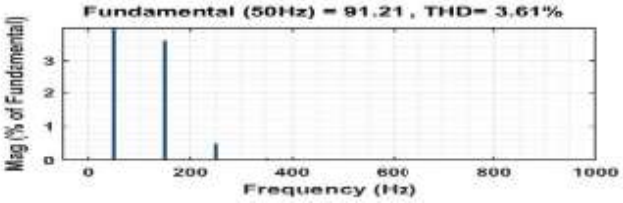

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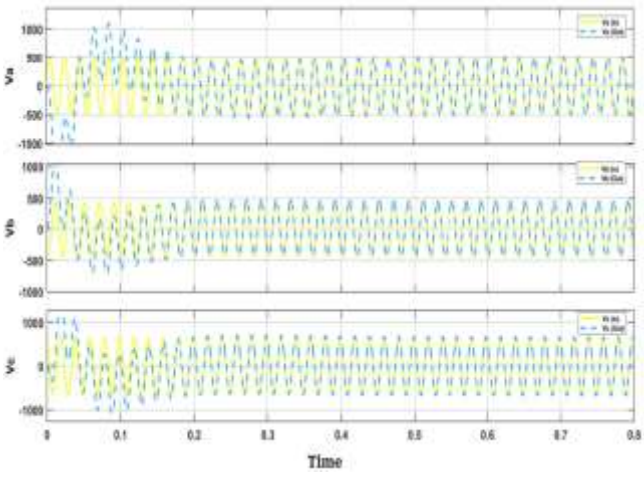

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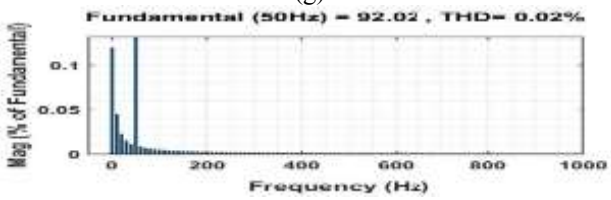

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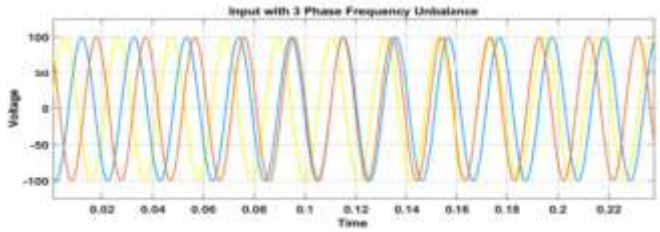
Fig. 7: SRF-PLL and DIM 3-Phase Voltage Unbalance. (a) Input of PLL. (b) Input and output SRF-PLL. (c) Phase angle SRF- PLL. (d) frequency and error signal PLL. (e) Input FFT analysis SRF-PLL. (f) Output FFT analysis SRF-PLL. (g) Input and output DIM. (h) Output FFT analysis DIM

The 3-phase input signal is added with frequency unbalances using unequal frequencies of 0.95, 0.97 and 1.03 times of fundamental frequency. Figure 8(a-h), exhibits the simulation results of SRF-PLL and DIM with frequencies unbalances in the input signal as shown in Figure 8(a) Whereas, Figure 8(b-f) shows the output of PLL synchronized with input signal having un balance frequencies, phase angle of PLL, frequency error signal and FFT analysis of input and output of PLL. Figure 8(g-h) shows the output of DIM synchronized with the input signal with frequencies unbalanced at t= 0.005s and FFT analysis gives a THD value of 28.47%.



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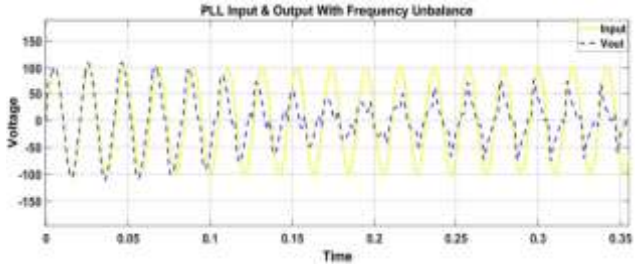

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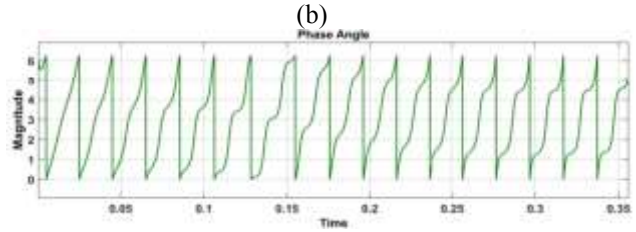
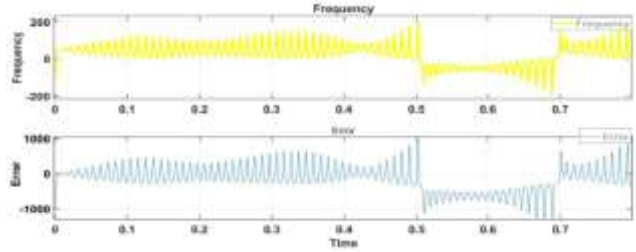
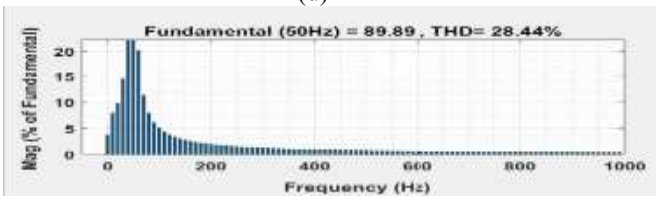


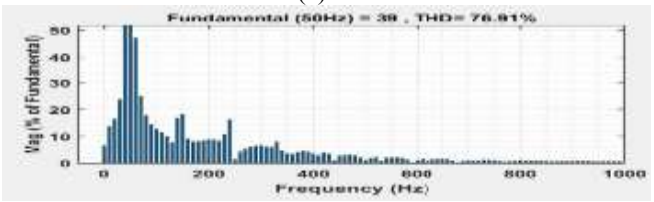
(c)



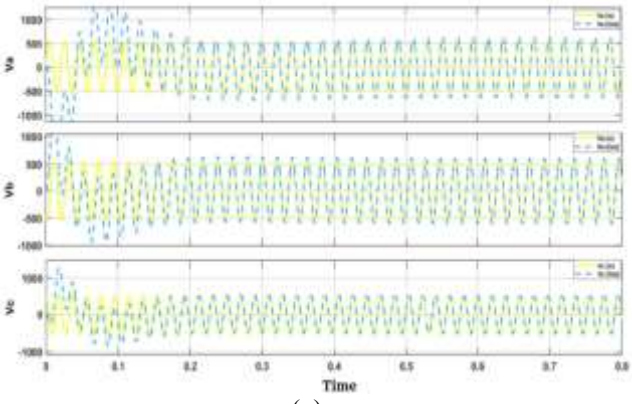
(d)



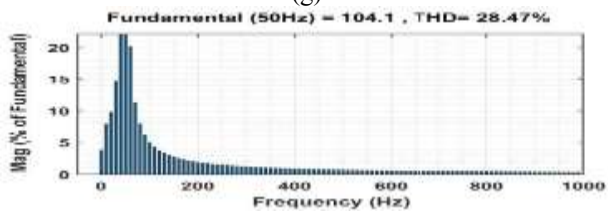
(e)



(f)



(g)



(h)

Fig. 8: SRF-PLL and DIM 3-Phase Frequency Unbalances. (a) Input SRF-PLL. (b) Input & Output of SRF-PLL. (c) Phase angle SRF-PLL. (d) Frequency and error signal SRF- PLL. (e) Input FFT analysis SRF-PLL. (f) Output FFT analysis SRF-PLL. (g) Input and output of DIM. (h) Output FFT analysis DIM

The results comparison between SRF-PLL and DIM during distorted grid conditions are given in Table 2.

Table 2. ResultsSRF-PLL and DIM

	PLL	**DIM**
Ideal condition	0.002 s (Response Time)	0.005 s (Response Time)
DC offset	0.9 % of fundamental, 0.23% THD	0.13% of fundamental, 0.02% THD
Harmonics	Addition of 3rd Harmonic, 8.97 %THD	0.28% THD
Voltage unbalance	3rd and 5th harmonics, 3.61 %THD	0.12 % DC offset, 0.02%THD
Frequency unbalance	76.91 THD	28.47 THD

4 Inverter Grid Synchronization

3-phase Inverter is synchronized with a grid voltage using SRF-PLL and DIM methods under ideal and distorted grid conditions as shown in Figure 9, [25]. The control system developed for SRF-PLL and DIM is displayed in Figure 10 and Figure 11 respectively.

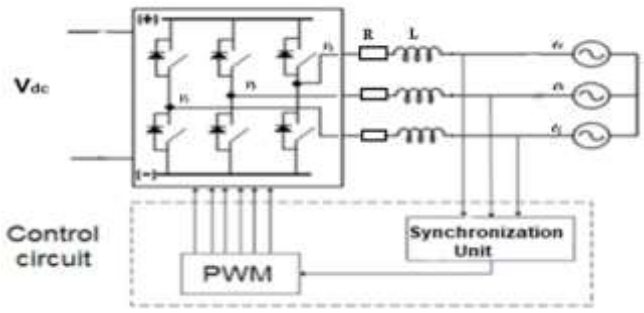


Fig. 9: 3-Phase Grid Tied Invertor

The mathematical model of a 3-phase grid-tied inverter in a natural reference frame is shown in (9).

$$\begin{bmatrix} L\frac{di_a}{dt} \\ L\frac{di_b}{dt} \\ L\frac{di_c}{dt} \end{bmatrix} = \begin{bmatrix} -R & 0 & 0 \\ 0 & -R & 0 \\ 0 & 0 & -R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} \quad (4)$$

After the d-q transformation, equation (4) becomes;

$$\begin{bmatrix} L\frac{di_d}{dt} \\ L\frac{di_q}{dt} \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ \omega L & -R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} e_d \\ e_q \end{bmatrix} \quad (5)$$

By re-arranging equation (5);

$$L\frac{di_d}{dt} + i_d R = V_d + \omega L i_q - e_d \quad (6)$$

$$L\frac{di_q}{dt} + i_q R = V_q - \omega L i_d - e_q \quad (7)$$

There is coupling (current) between d axis and q axis, to achieve zero steady-state error, the PI regulators can be used as shown in Figure 10;

$$K_{Pd}\left(1 + \frac{1}{t_{id}S}\right) = V_d + \omega L i_q - e_d \quad (8)$$

$$K_{pq}\left(1 + \frac{1}{t_{iq}S}\right) = V_q - \omega L i_d - e_q \quad (9)$$

The output Voltage V_d and V_q can be obtained can be obtained, where ω is angular frequency;

$$V_d = K_{Pd}\left(1 + \frac{1}{t_{id}S}\right) - \omega L i_q + e_d \quad (10)$$

$$V_q = K_{pq}\left(1 + \frac{1}{t_{iq}S}\right) + \omega L i_d + e_q \quad (11)$$

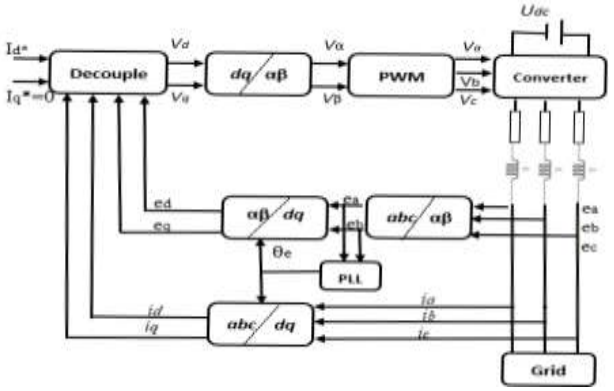


Fig. 10: 3-Phase grid-connected control system SRF-PLL

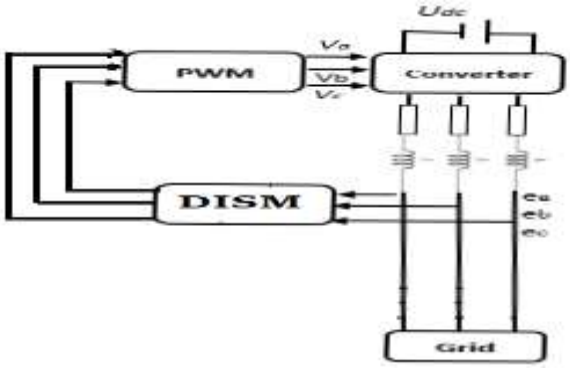


Fig. 11: 3-Phase grid-connected control system DIM

Pant Transfer function is given in equation (12) using values, R=0.1 and L=500μH:

$$G = \frac{1}{0.0005S + 0.1} \quad (12)$$

And PI transfer function including kp =10, ki=500 values

$$G_c = \frac{0.1042\,s + 62.57}{s} \quad (13)$$

The total forward transfer function is given in equation (14)

$$G_t = G * G_c \quad (14)$$

The step response to the plant during uncompensated and compensated is shown in Figure 12 and its frequency plots are shown in Figure 13.It shows the system is stable.

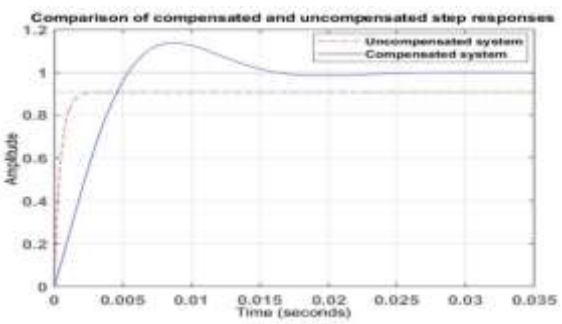


Fig. 12: Comparison of Step responses

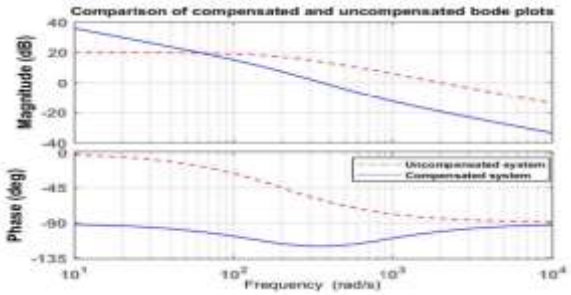
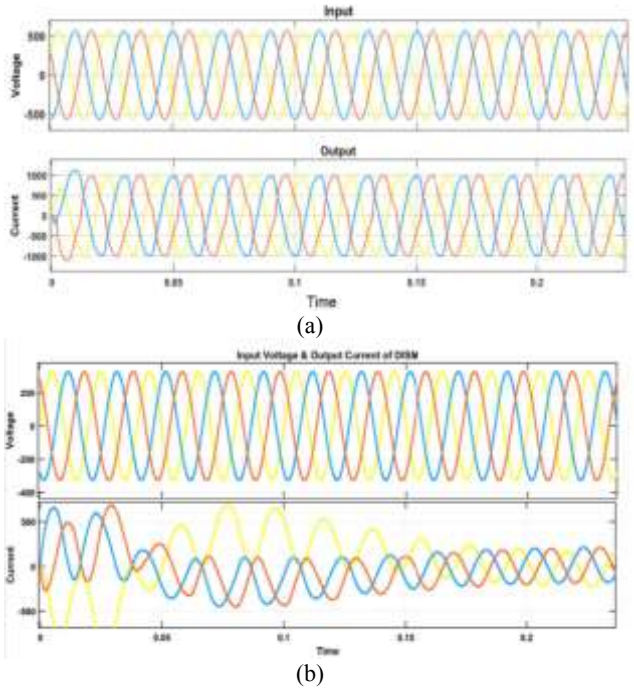


Fig. 13: Comparison of Compensated and Uncompensated Bode Plots

The SRF-PLL and DIM synchronized with a 3-phase Inverter is tested and simulated during ideal and following distorted grid conditions; a) DC offset; b) harmonics; Figure 14(a-h), shows the simulation results of SRF-PLL and DIM with grid-connected 3-phase inverter during ideal conditions. Figure 14(a-b) shows 3-phase input voltage and output current.

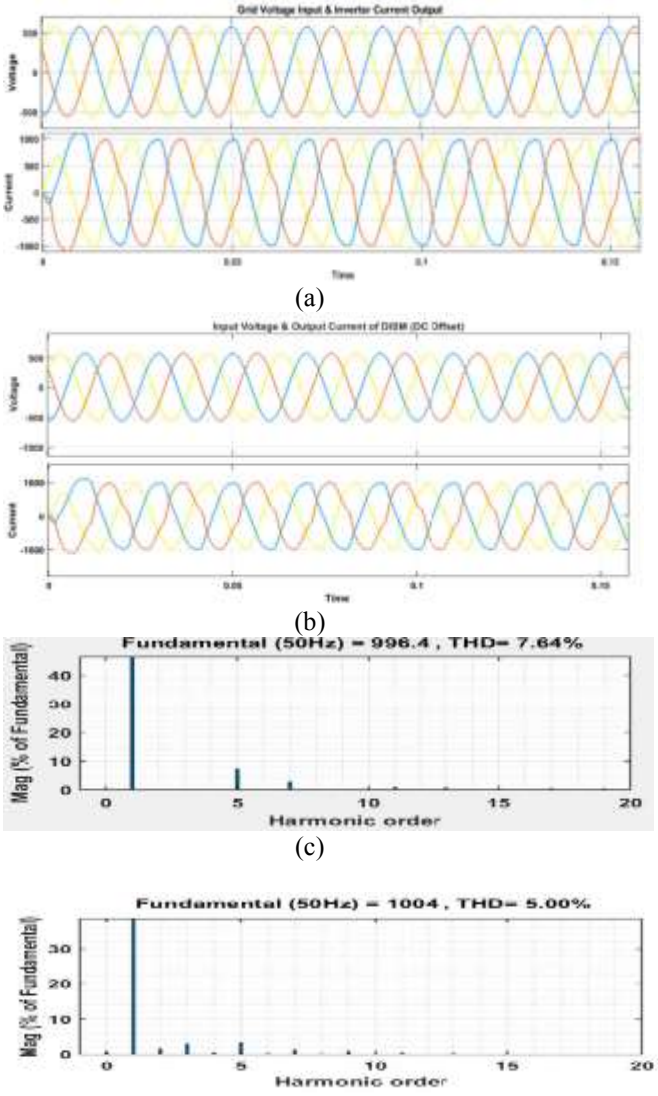


(a)

(b)

Fig. 14: Grid-connected Inverter SRF-PLL and DIM, Ideal Grid conditions. (a) Input and output SRF- PLL. (b)Input and output DIM

In this case DC Offset introduces (10, 8, 10) times of Vm, into the input signal, and gets the results as shown in Figure 15. Figure 14(a-b), displays the simulation results of SRF-PLL and DIM with grid-connected 3-phase inverter during DC offset conditions. Figure 15(a-b) shows a 3-phase input voltage and output current. Figure 15(c-d) shows FFT analysis SRF-PLL and DIM.



(a)

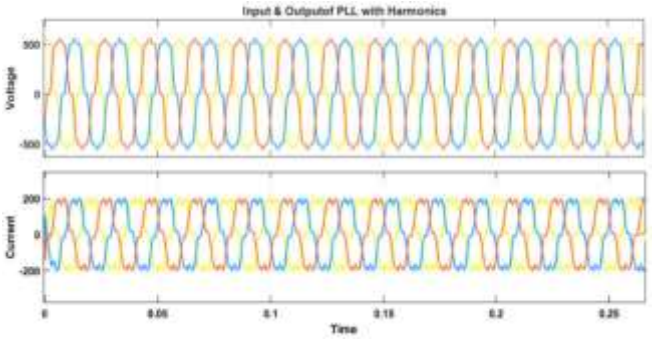
(b)

(c)

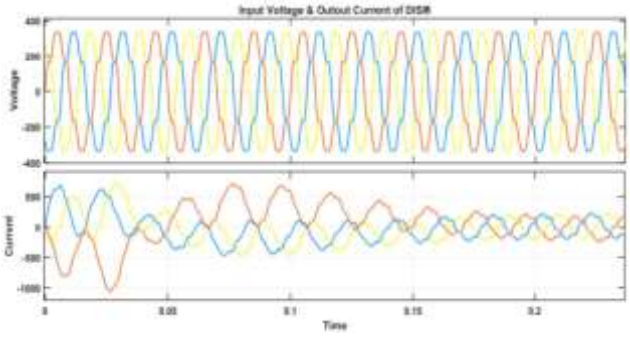
(d)

Fig. 15: Grid-connected Inverter SRF-PLL and DIM during DC Offset. (a) Input and Output SRF-PLL. (b) Input and Output DIM Output (C) FFT analysis SRF-PLL (c) FFT analysis DIM

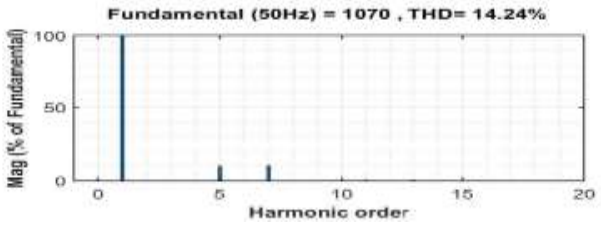
The 5th and 7th Harmonics are added into the input signal and results as shown in Figure 16(a-b), represents the simulation results of SRF-PLL and DIM of input voltage and output current with grid connected 3-phase inverter during harmonics. Figure 16(c-d) shows the FFT analysis of SRF-PLL and DIM.



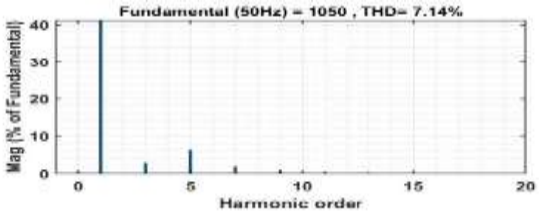
(a)



(b)



(c)



(d)

Fig. 16: Grid-connected Inverter SRF-PLL and DIM during Harmonics Injection. (a) Input and Output of SRF-PLL. (b) Input and Output DIM (C) FFT analysis SRF-PLL (c) FFT analysis DIM

Table 3 shows the simulation results of PLL & DIM in a Grid-tied Inverter. The DIM method outperforms the SRF-PLL method with reduced THDs.

Table 3. Comparison of PLL & DIM Grid Tied Inverter

	PLL	**DISM**
Ideal condition	0.002 s (Response Time)	0.005 s (Response Time)
DC offset	7.64 % THD	5 % THD
Harmonics	14.24 %THD	7.14 % THD

The art in the double integral principle is to remove DC components without neither distortion nor phase shifts. It will limit amplitude, removing DC in one or two periods.The limitation ofDIM method is to correct the amplitude and integrate constant in one period.

5 Conclusion

This research work proposed DIM method for grid synchronization in the presence of DC offset, harmonics, voltage unbalances and frequency unbalances. This method outperforms the SRF-PLL method in mitigating the effects of DC offset, harmonics,3-phase voltages, and frequency unbalances and enabling precise synchronization with the grid voltage. The SRF- PLL method shows errors in tracking the distorted voltage waveforms. The DIM method offers improved performance in dealing with non – ideal grid problems such as DC offset, harmonics, and 3-phase voltage unbalances.
Linear lagging feedback, the circuit is developed, that eliminates DC offset at each integrator as well as phase error reduction. In future work, the DIM method will be compared with other types of PLL available in the literature.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- Faheem Farooq and Kamran Hafeez carried out the simulations and paper wrting.
- Bayan Mahdi Sabbar and Mohannad Jabbar Mnatii have helped in designing and overall supervision of obtaining results.

Conflict of Interest

The authors have no conflicts of interest to declare.

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