Analysis of Cascaded Asymmetric Inverters using Low Frequency Technique

LAKSHMI PRASANNA, T. R. JYOTHSNA
Department of Electrical Engineering,
Andhra University,
Visakhapatnam,
INDIA

Abstract: - Multilevel inverters include a wide range of configurations and numerous benefits. Since each level switching angle is not neatly prepared, most conventional inverters cannot produce optimized waveforms. To attain an adequate voltage profile, we should indeed closely review the switching angle arrangement to attain a minimal Total Harmonic Distortion (THD). This work focuses on Cascaded H Bridge (CHB) multilevel inverters with asymmetrical configuration operating under a low frequency (LF) scheme. This work discusses various methods of harmonic mitigation techniques that comes under the LF scheme which includes the finest switching angle optimizations for generating various levels. Furthermore, the effectiveness of the topologies is investigated by minimizing lower-order harmonics and THD. THD is compared for various mitigation techniques for seven and nine-level configurations. The proposed configurations are simulated by employing MATLAB/Simulink. THD is calculated theoretically and evaluated by comparing it to simulated results for the suggested inverters. Additionally, thermal simulations of the configuration are carried out in PLECS to estimate power losses and efficiency. The suggested configurations are examined utilizing OPAL-RT (4510) test bed and the outcomes are included.

Key-Words: - Asymmetric Inverter, Harmonic mitigation techniques, Low-frequency scheme, Total Harmonic Distortion, Total Standing Voltage, OPAL-Rt.

Received: April 12, 2023. Revised: February 13, 2024. Accepted: April 16, 2024. Published: May 9, 2024.

1 Introduction

Multilevel inverters (MLI) are rapidly gaining importance in sustainable energy conversion and applications in industry owing to their superior output waveform to two-level inverters. The traditional two-level inverter drawbacks like larger harmonic distortion, lower efficiency, reduced power quality, and so on. Considering these aspects, MLIs have proved to be an effective substitute in a wide range of applications, [1], [2]. Classic MLI configurations such as Neutral Point Clamped MLI (NPCMLI), Cascaded H-Bridge MLI (CHBMLI), and Flying Capacitor MLI (FCMLI) are widely utilized in industries, [3], [4]. Conversely, traditional MLI has restrictions including capacitor voltage imbalance in NPC and FC. Among these inverters, the CHB MLI necessitates minimal component count than other conventional inverter topologies for creating an identical level of output. CHB inverters are transitioning from a traditional perspective to real-world applications due to capabilities that include high degree of modularity, and the ability to safely link to medium voltage with superior power quality, [5], [6].

The beneficial effects associated with utilizing higher levels involve improved efficiency, lessened filter size, substantial power density, reliability, as well as a wider implementation range, [7], [8]. However, researchers encountered a few obstacles while reducing component counts, such as enhanced rated voltage of switching devices, losses in extensibility, minimization of number of concurrent states, occasional demand of bidirectional switches, advanced control methodologies, enormous prevalence of sources to accomplish the anticipated level count from the existing topologies, [9], [10]. Modulation techniques are the fundamental aspect for any MLI structure, [11]. Suggesting novel modulation schemes that can be implemented for any type of structure to meet specified requirements can be viewed as a distinct area of research, [12]. A schematic illustration of modulation schemes is depicted in Figure 1. MLI modulation schemes are commonly categorized as high frequency (HF) or low frequency (LF). A comparison of various HF schemes for hybrid MLI is described, [13].

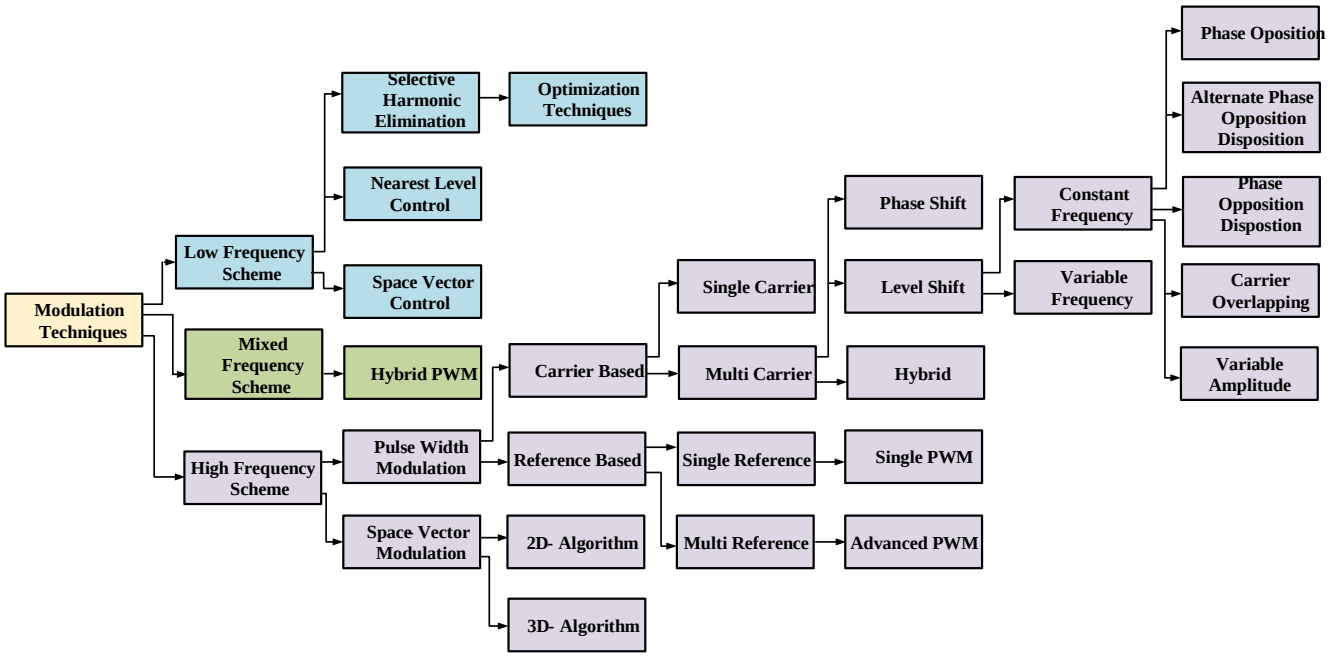


Fig. 1: Various Modulation Techniques

The worth of utilizing an LF scheme rather than HF scheme are reduced switching losses, minimum stress on switches, improved device utilization factor, and enhanced converter efficiency. The most popular LF schemes include selective harmonic elimination (SHE), nearest level control (NLC), and space vector control. If the number of levels is greater, SVC is a reasonable technique only issue is it does not eliminate specific harmonic. The above problem is mitigated using the SHE method by adjusting the switch angles mentioned, [14].

Review of SHE technique algorithms described, [15], [16]. Minimization of harmonics utilizing the Particle Swarm Optimization (PSO) approach for symmetrical MLI configuration is presented, [17]. The deal of the PSO technique for an asymmetrical configuration is put forward in[18]. Furthermore, the PSO approach, [17], [18] is lacking in estimating switching angles for specified modulation indices (m_a) based on computational results from the Genetic Algorithm (GA) approach, [19]. As the level of output extends, obtaining solutions using SHE becomes more challenging to implement. Consequently, another straightforward approach of SHE addresses the above issue has been executed in [20], that is harmonic mitigation which involves remarkable minimization of lower order harmonics rather than entirely eradicating them.

The effectiveness of Packed U Cell (PUC) topology using PWM methods is proposed, [21]. A single phase seven-level inverter using an HF scheme applicable to PV is presented, [22]. In [23], Hybrid topology is designed, taking the merits of an H-bridge inverter with minimum components. A novel topology with few component counts using HF scheme is discussed, [24]. The Typhoon Hardware-in-Loop (HIL) Simulator is employed to develop and evaluate CHB-based multilevel inverters (MLI) for nine-level generation, [25]. A hybrid PWM technique is employed for nine-level topology in [26]. A dual input configuration utilizing a few components for nine-level generation is described, [27]. T-type PUC topology using identical sources for the creation of nine levels is mentioned, [28].

The functioning of asymmetrical CHBMLI topologies considering mitigation techniques is proposed in this work. This work has the following structure: Section 2 confronts proposed topologies with all switching states for seven and nine levels, respectively. Section 3 focuses on mitigation techniques, voltage stress analysis, and calculation of power losses. Section 4 includes simulation results, Thermal modeling, and HIL Implementation. Section 5 deals with comparative PWM technique analysis and Section 6 refers to a conclusion.

2 CHB Topology

The proposed inverter structure is designed by cascading two H-bridges. Figure 2 depicts a basic cascaded multilevel inverter circuit. As seen, it involves the use of eight switches and two isolated sources. Using the same topology, seven and nine levels are created based on the selection of DC voltage sources. When two input sources are in

binary proportion, the inverter operates in a seven-level configuration. If the DC sources have a trinary ratio, the inverter will operate in a nine-level configuration. The operating modes of seven and nine levels are explained as follows. The green and red colors in Figure 3 and Figure 4 point to a conductivity and non-conductivity path respectively.

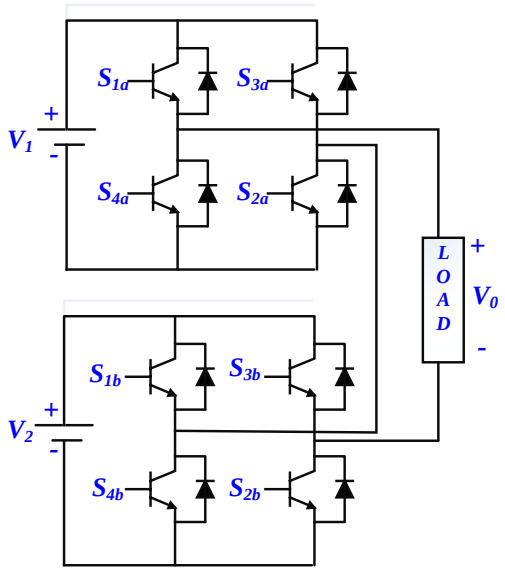


Fig. 2: Basic Topology

2.1 Seven-Level Topology

Figure 2 depicts the structure of design with source voltages in binary ratio. Table 1 shows the switching modes of this topology,0 indicates the off position and 1 indicates the on position of the switch respectively. The switching modes of positive, and negative modes of operation are shown in Figure 3. The operating modes are explained as follows.

$\pm 3V_{dc}$: To get a positive output voltage of $+3V_{dc}$, S_{1a}, S_{2a}, S_{1b} and S_{2b} conducts to connect the load to the source depicted in Figure 3(a). In the same fashion $-3V_{dc}$ is produced by the conduction of S_{3a}, S_{4a}, $S_{3b,}$ and S_{4b} respectively as illustrated in Figure 3(f).

$\pm 2V_{dc}$: To obtain an output voltage of $+2V_{dc}$, S_{1a}, S_{3a}, S_{1b} and S_{2b} conducts shown in Figure 3(b). For getting $-2V_{dc}$ as output voltage S_{2a}, S_{4a}, S_{3b} and S_{4b} conducts shown in Figure 3(e).

$\pm 1V_{dc}$: For $+1V_{dc}$ operating mode S_{1a}, S_{2a}, S_{1b} and S_{3b} conducts and voltage occurs across the load as shown in Figure 3(c). For $-1V_{dc}$ operating *mode* S_{3a}, S_{4a}, $S_{2b,}$ and S_{4b} conducts and voltage occurs across the load as illustrated in Figure 3(d).

2.2 Nine-Level Topology

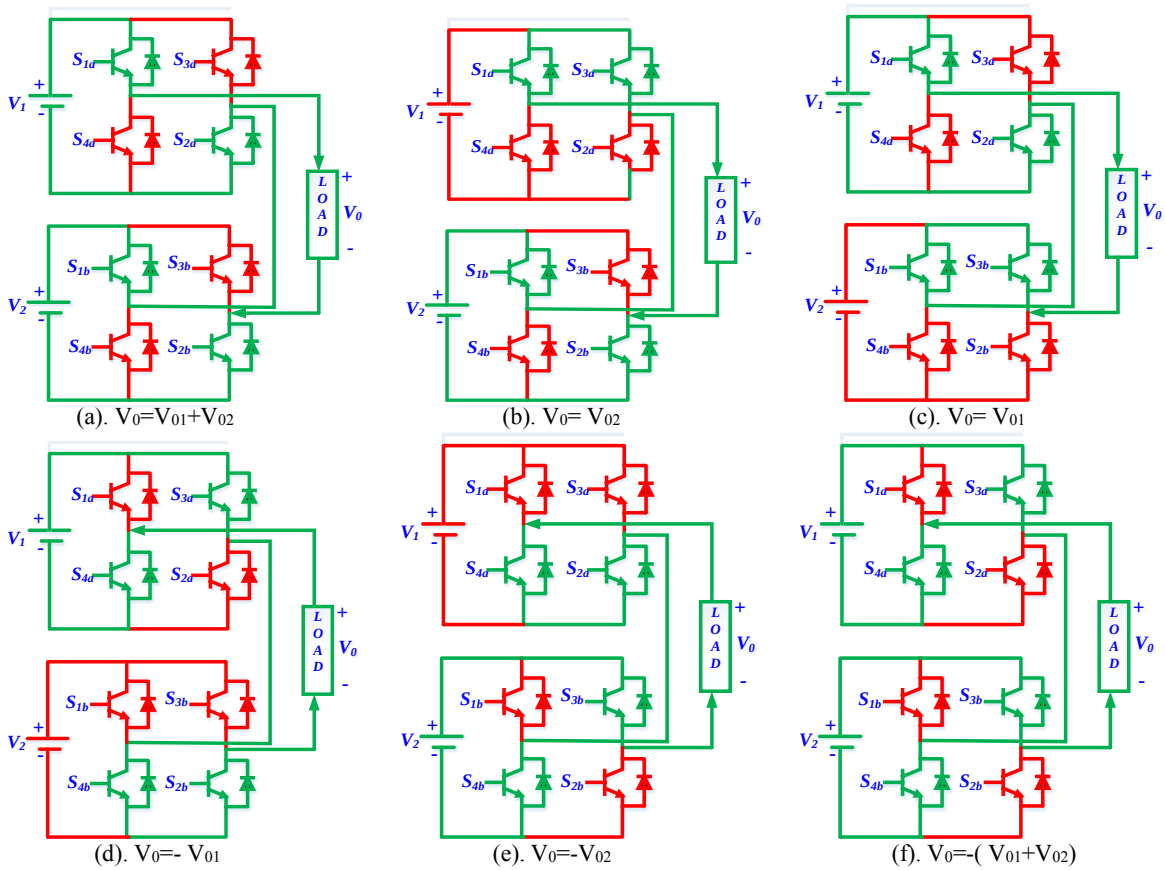
As previously stated, it utilizes eight devices and two sources in a trinary fraction. Like Table 1 it follows the same logic mentioned in Table 2. The operating modes ($\pm 4V_{dc}$, $\pm 3V_{dc}$, $\pm 2V_{dc}$, and $\pm 1V_{dc}$) are described below:

$\pm 4V_{dc}$: During the creation of $+4V_{dc}$ as output voltage switches S_{1a}, S_{2a}, $S_{1b,}$ and S_{2b} form the conduction path, resulting in the display of input voltage across the load shown in Figure 4 (a). In the same direction that S_{3a}, S_{4a}, $S_{3b,}$ and S_{4b} create conduction path input voltage across the load to deliver $-4V_{dc}$ as output voltage, as shown in Figure 4 (h).

$\pm 3V_{dc}$: The operation described earlier for the $\pm 2V_{dc}$ mode, shown in Figure 3(b) and (e), is reinforced in this case, i.e., for $\pm 3V_{dc}$ the conduction path during the positive and negative depicted in Figure 4(b) and (g) respectively.

$\pm 2V_{dc}$: The conduction path is created by S_{3a}, S_{4a}, S_{1b} and S_{2b} for the generation of $+2V_{dc}$ as the voltage across the load shown in Figure 4(c). S_{1a}, S_{2a}, $S_{3b,}$ and S_{4b} establish a conduction path to yield $-2V_{dc}$ as the voltage across a load illustrated in Figure 4(f).

$\pm 1V_{dc}$: S_{1a}, S_{2a}, S_{1b} and S_{3b} form the conduction path shown in Figure 4(d) to produce $+1V_{dc}$ as the output voltage. S_{3a}, S_{4a}, $S_{2b,}$ and S_{4b} conduct and create the path of current flow from source to load and $-1V_{dc}$ across load as shown in Figure 4(e).



(a). $V_0=V_{01}+V_{02}$ (b). $V_0=V_{02}$ (c). $V_0=V_{01}$

(d). $V_0=-V_{01}$ (e). $V_0=-V_{02}$ (f). $V_0=-(V_{01}+V_{02})$

Fig. 3: Operating modes of seven-level Topology

Table 1. Switching modes of Seven-level Topology

Switching action				*Cell1 O/P Voltage*	*Switching action*				*Cell2 O/P Voltage*	*Total O/P Voltage*
S_{1a}	S_{2a}	S_{3a}	S_{4a}	V_{o1}	S_{1b}	S_{2b}	S_{3b}	S_{4b}	V_{o2}	V_o
1	1	0	0	$+1V_{dc}$	1	1	0	0	$+2V_{dc}$	$+3V_{dc}$
1	0	1	0	0	1	1	0	0	$+2V_{dc}$	$+2V_{dc}$
1	1	0	0	$+1V_{dc}$	1	0	1	0	0	$+1V_{dc}$
0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	$-1V_{dc}$	0	1	0	1	0	$-1V_{dc}$
0	1	0	1	0	0	0	1	1	$-2V_{dc}$	$-2V_{dc}$
0	0	1	1	$-1V_{dc}$	0	0	1	1	$-2V_{dc}$	$-3V_{dc}$

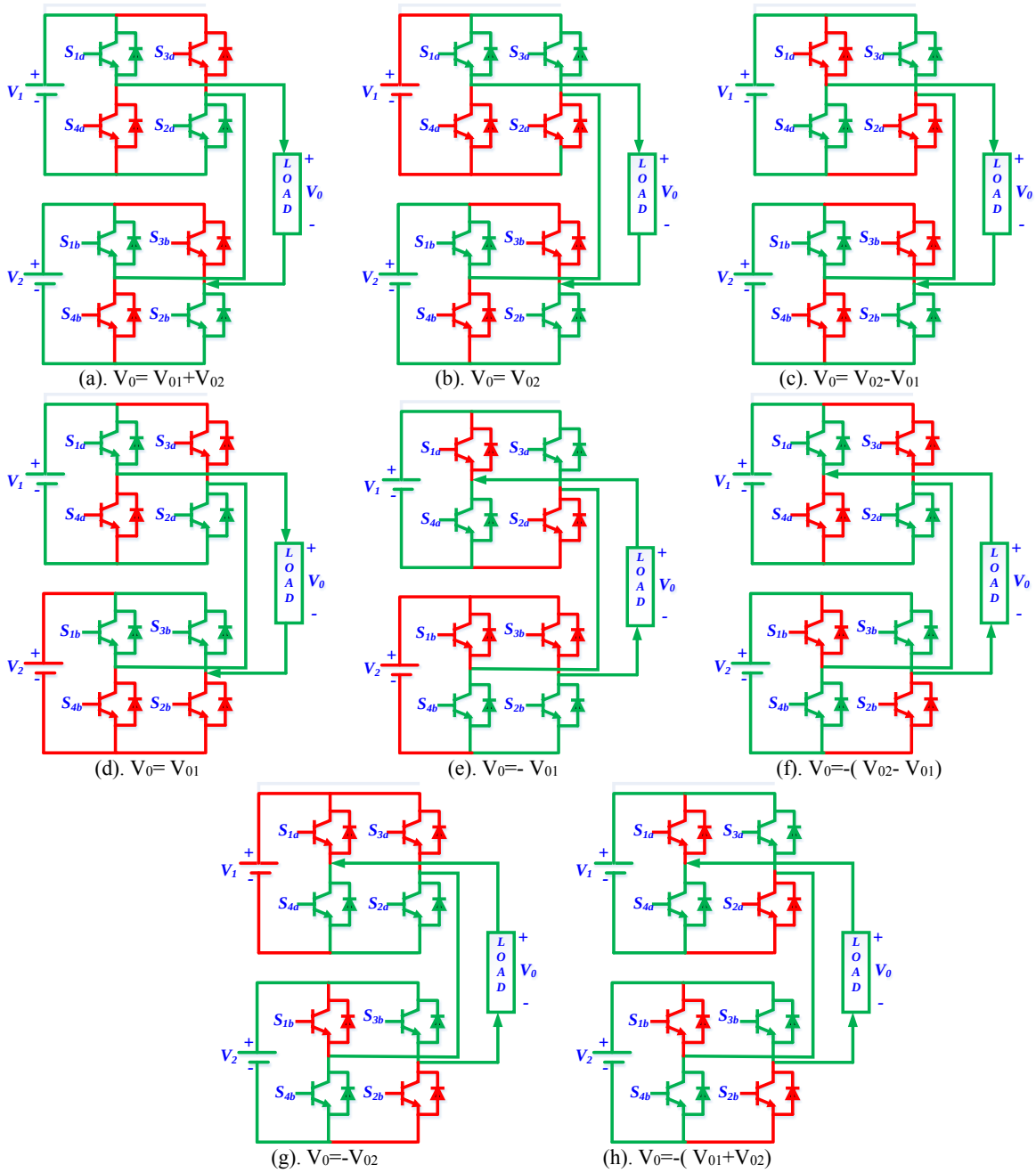


Fig. 4: Operating modes of Nine-level topology

Table 2. Switching modes of Nine-level Topology

Switching action				*Cell1 O/P Voltage*	*Switching action*				*Cell2 O/P Voltage*	*Total O/P Voltage*
S_{1a}	S_{2a}	S_{3a}	S_{4a}	V_{o1}	S_{1b}	S_{2b}	S_{3b}	S_{4b}	V_{o2}	V_o
1	1	0	0	$+1V_{dc}$	1	1	0	0	$+3V_{dc}$	$+4V_{dc}$
1	0	1	0	0	1	1	0	0	$+3V_{dc}$	$+3V_{dc}$
0	0	1	1	$-1V_{dc}$	1	1	0	0	$+3V_{dc}$	$+2V_{dc}$
1	1	0	0	$+1V_{dc}$	1	0	1	0	0	$+1V_{dc}$
0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	$-1V_{dc}$	0	1	0	1	0	$-1V_{dc}$
1	1	0	0	$+1V_{dc}$	0	0	1	1	$-3V_{dc}$	$-2V_{dc}$
0	1	0	1	0	0	0	1	1	$-3V_{dc}$	$-3V_{dc}$
0	0	1	1	$-1V_{dc}$	0	0	1	1	$-3V_{dc}$	$-4V_{dc}$

3 Analysis of Mitigation Techniques, Voltage Stress, and Power Losses

3.1 Mitigation Techniques

The switching angles considered for a quarter wave symmetry are shown in Figure 4. There are 2(m-1) switching angles expressed in the figure m-level (m is an odd digit) output voltage waveform. As seen in Figure 5, switching angles are divided into four quadrants. The first quadrant (range from 0 to π/2) switching angles are called main switching angles. By using main switching angles remaining quadrant angles are calculated easily.

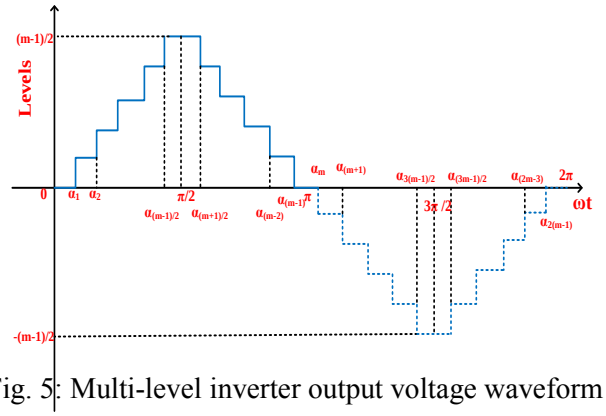


Fig. 5: Multi-level inverter output voltage waveform

In the First quadrant interval (0 - π/2), the main switching angles are denoted as

$$\alpha_1, \alpha_2, ..., \alpha_{(m-1)/2} \tag{1}$$

In the second Quadrant interval (π/2 - π), the switching angles are represented as

$$\alpha_{(m+1)/2} = \pi - \alpha_{(m-1)/2}, ..., \alpha_{(m-1)} = \pi - \alpha_1 \tag{2}$$

In the third quadrant interval (π- 3π/2), the switching angles are indicated as

$$\alpha_m = \pi + \alpha_1, ..., \alpha_{3(m-1)/2} = \pi + \alpha_{(m-1)/2} \tag{3}$$

In the fourth quadrant interval (3π/2 -2π), the switching angles are indicated as

$$\alpha_{(3m-1)/2} = 2\pi - \alpha_{(m-1)/2}, ..., \alpha_{2(m-1)} = 2\pi - \alpha_1 \tag{4}$$

By using the above analysis of switching angles, based on the mitigation technique switching angle is modified. The conventional methods are explained as follows.

Equal Phase Method (EPM): The formula (5) is capable of being utilized to create an assessment of switching angles in this method. The switching angles are equally distributed, with an average spectrum of (0 - π/2). The number m denotes the generated number of levels.

$$\alpha_i = i * \frac{180}{m} \tag{5}$$

where i=1, 2, ……., (m-1)/2

Half Equal Phase Method (HEPM): Since the result is too narrow as well as the resulting waveform appears as a triangle in EPM, the HEPM approach has been created to obtain a larger and more effective output from the MLIs. The switching angles in the (0 - π/2) spectrum are calculated using the formula as follows:

$$\alpha_i = i * \frac{180}{(m+1)} \tag{6}$$

Half Height Method (HHM): Even though the first two methods can smoothly arrange the main switching angles, the output waveform does not look like a sinusoidal. By using this method, the switching angles in the first quadrant are estimated depending on the sine function. The theory is that when the sine function value raises to half the altitude of the level, the switching angle is positioned, leading to an improved output waveform. The following formula specifies the main switching angles.

$$\alpha_i = \sin^{-1}\left(\frac{2i-1}{m-1}\right) \tag{7}$$

Feed Forward Method (FFM): Unlike the rest of the approaches, it was designed to minimize the difference between the two half cycles of output, as represented by equation (8)

$$\alpha_i = \frac{1}{2}\sin^{-1}\left(\frac{2i-1}{m-1}\right) \tag{8}$$

As a result, the main switching angles are effectively obtained for the 'm' number of levels by using four Equations (5-8). For seven-level topology, the three main switching angles are calculated based on the four methods and depicted in Table 3. In the same fashion for nine-level topology four switching angles are generated and represented in Table 4 based on the four methods.

$$THD = \frac{\sqrt{\left(\left(\frac{\pi^2 p^2}{8}\right) - \left(\frac{\pi}{4}\left(\sum_{i=0}^{p-1}(2i-1)\alpha_i\right)\right) - \left(\sum_{i=1}^{p}\cos\alpha_i\right)^2\right)}}{\left(\sum_{i=1}^{p}\cos\alpha_i\right)} \quad (9)$$

Table 3. Switching angles of Seven-level Topology

Methods	Main switching angles (Degrees)		
	α_1	α_2	α_3
EPM	25.71	51.43	77.14
HEPM	22.50	45.00	67.5
HHM	9.60	30.00	56.44
FFM	4.80	15.00	28.22

By using main switching angles Total Harmonic Distortion (THD) is expressed as equation (9)

Table 5 displays the calculated THD values for seven-level and nine-level topology. Table 5 shows that when compared to EPM, the HEPM has a lower %THD irrespective of the level of configuration. The FFM has a lower %THD compared to the EPM and HPEM. HHM yields superior results for both configurations while all methods are acknowledged.

Table 4. Switching angles of Nine-level Topology

Methods	Main switching angles (Degrees)			
	α_1	α_2	α_3	α_4
EPM	20	40	60	80
HEPM	18	36	54	72
HHM	7.18	22.02	38.68	61.04
FFM	3.59	11.01	19.34	30.52

3.2 Voltage Stress Analysis

The maximum voltage stress of complementary switches has identical magnitudes for the presented design. Equations (10) and (11) show the maximum voltage stress of the switches for the seven-level topology.

$$V_{s1a} = V_{s2a} = V_{s3a} = V_{s4a} = 1V_{dc} \quad (10)$$

$$V_{s1b} = V_{s2b} = V_{s3b} = V_{s4b} = 2V_{dc} \quad (11)$$

$$TSV = 4*(V_{s1a} + V_{s1b}) = 12V_{dc} \quad (12)$$

Table 5. Calculated %THD of seven-level and nine-level topology

Mitigation method	THD (%)	
	Seven-level Topology	Nine-level Topology
EPM	31.35	25.9
HEPM	25.8	22.32
HHM	12.5	9.4
FFM	22.5	21.57

where V_{sn} stands for the peak voltage appearance of the switch during the turn-off process. For this structure, the total standing voltage (TSV) is denoted as equation (12). The TSV (p.u.) is the proportion of the combined value of the blocking voltages of switches with the peak voltage that appears across the load. In this instance for a seven-level configuration TSV (p.u.) is 4. Considering the same approach for nine-level configuration voltage stress and TSV (p.u) are estimated.

For seven-level configuration blocking voltage of switches is represented as a bar chart in Figure 6(a). From Figure 6(a), for $+3V_{dc}$ mode, the switches S_{1a}, S_{2a}, S_{1b}, and S_{3b} switches create a conduction path and the remaining switches are non-conductive elements. Therefore, the blocking voltage of switches S_{3a}, *and* S_{4a} is $+1V_{dc}$, and S_{3b}, *and* S_{4b} switches $+2V_{dc}$ respectively. In the same manner for other modes of operation are illustrated in Figure 6(a). Identically for nine-level topology blocking voltage of switches considering all the operating modes is depicted in Figure 6(b).

3.3 Power Losses

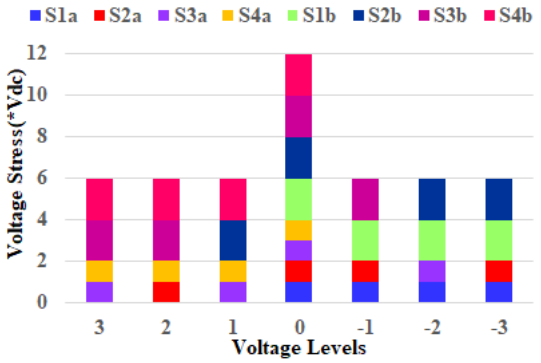
Switching and conduction losses are different types of power losses experienced by switching devices. Conduction losses are brought on by on-state resistance while switching losses are a result of delays in the switch's on/off processes. It is possible to express the switching loss during the turn-on process as

$$P_{swlturnon}(i) = f_{carrier}\int_0^{t_{on}} v(t)i(t)dt = f_{carrier}\int_0^{t_{on}}\left(\left(\frac{V_{swoff,i}}{t_{on}}(t_{on}-t)\right)\left(\frac{i_{on,i}}{t_{on}}t\right)\right)dt$$

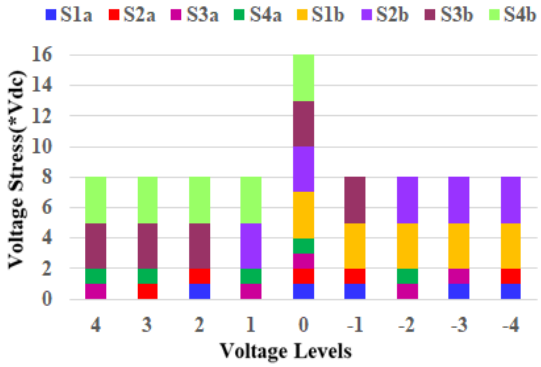
$$= \frac{1}{6}f_{carrier} * V_{swoff,i} * i_{on,i} * t_{on} \quad (13)$$

$$P_{swlturnoff}(i) = f_{carrier}\int_0^{t_{off}} v(t)i(t)dt = f_{carrier}\int_0^{t_{off}}\left(\left(\frac{V_{swoff,i}}{t_{off}}t\right)\left(\frac{i_{off,i}}{t_{off}}(t_{off}-t)\right)\right)dt$$

$$= \frac{1}{6}f_{carrier} * V_{swoff,i} * i_{off,i} * t_{off} \quad (14)$$



(a). Seven-level



(b). Nine-level

Fig. 6: Voltage stress of switches for various configurations

Where $P_{swlturnon}(i)$, $P_{swltunoff}(i)$ and V_{swoff} denotes the ith switch's turn on, turn off loss, and off-state switching voltage, respectively. Currents during the switch's on- and off-states, respectively, are called I_{on} and I_{off}. Total switching losses (P_{sw}) are calculated by summing turn-on and turn-off losses.

$$P_{sw}(Total) = \sum_{i=1}^{N_{sw}} \left(\sum_{j=1}^{N_{on}(i)} P_{swlon}(ij) + \sum_{j=1}^{N_{off}(i)} P_{swloff}(ij) \right) \quad (15)$$

Where N_{sw} is the total number of switches of the proposed MLI.

Conduction losses appear in a switch during the conduction period due to on-state resistance and voltage drop across the switch. The generalized equation for conduction losses of the diode and switch is as follows

$$P_{Dcon} = V_{Don} * i_{Davg} + R_{Don} * i_{Drms}^2 \quad (16)$$

$$P_{swcon} = V_{swon} * i_{swavg} + R_{swon} * i_{swrms}^2 (17)$$

Where P_{Dcon} and P_{swcon} are diode and switch conduction losses, V_{Don} and V_{swon} are on-state voltage drops of diode and switch respectively. R_{Don} and R_{swon} are on-state resistances of the diode and switch, i_{Davg}, i_{swavg}, i_{Drms}, and i_{swrms} are average and RMS currents of the switch respectively.

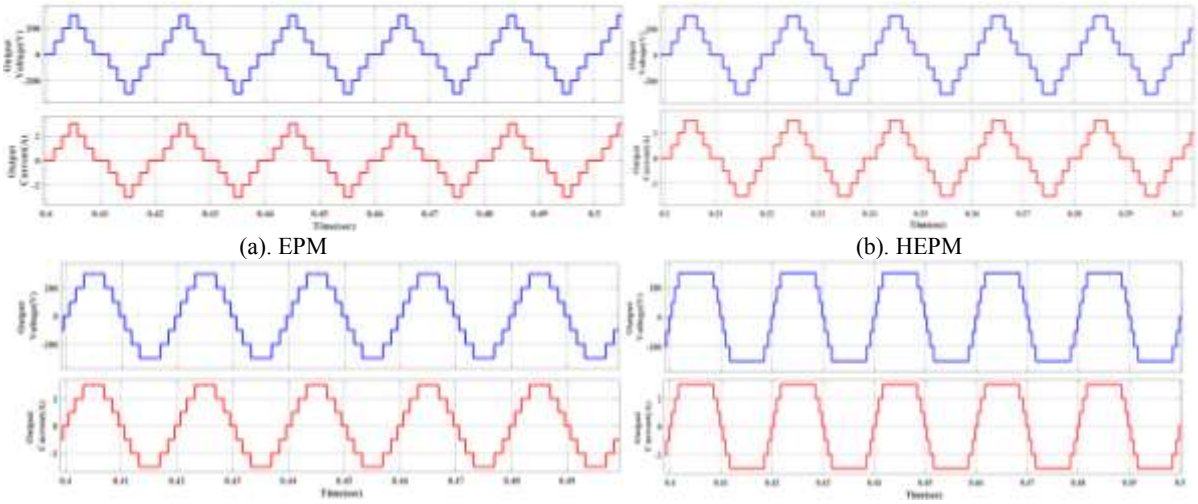
4 Results and Discussions

4.1 Simulation Results

MATLAB/Simulink platform is utilized for simulating the execution of seven-level and nine-level operations respectively. The source voltages for the seven-level and nine-level are categorized as (100V,200V), (100V,300V), and load parameters are 100Ω and100mH respectively. The operating frequency of the proposed inverter is fundamental frequency i.e., 50Hz. Blue and red color represent load voltage and current respectively.

Figure 7 shows the performance of the inverter for R-load. The output current appears to be in proportion to the output voltage irrespective of the mitigation technique. Figure 8 shows the performance of the inverter under different loading conditions for seven-level operation. According to Figure 8, it indicates that output voltage remains constant irrespective of load scenarios, however current is null during unloading, implying voltage for Resistive loads and delays for inductive loads.

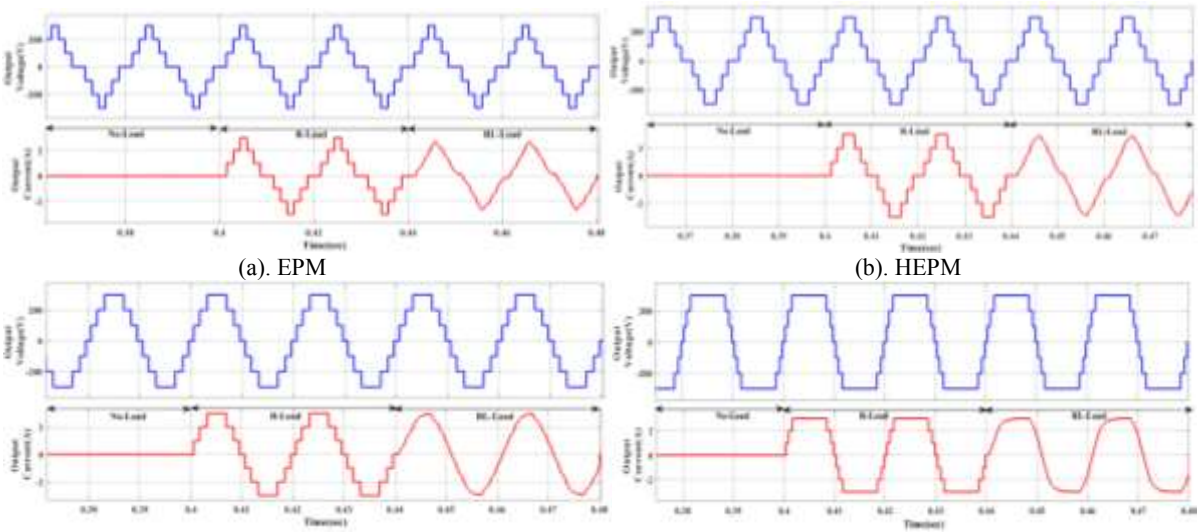
Figure 9 represents the waveforms of voltage and current with respect to various RL-Loads. Figure 9 shows that as inductance increases, the current falls due to high inductive load leads more lagging of current. In contrast to other methods, the HHM current waveform is more sinusoidal. Figure 10 depicts three waveforms, the first waveform (purple color) is the voltage across bridge1, the second waveform (brown color) is the voltage across bridge2 and the third waveform (blue color) is the total output voltage waveform respectively. Figure 11 shows the THD of a seven-level inverter for various mitigation methods. The THD shown for seven-level HHM is 12.13% which is less compared to other methods. It shows the minimization of THD by using this method.



(a). EPM (b). HEPM

(c). HHM (d).FFM

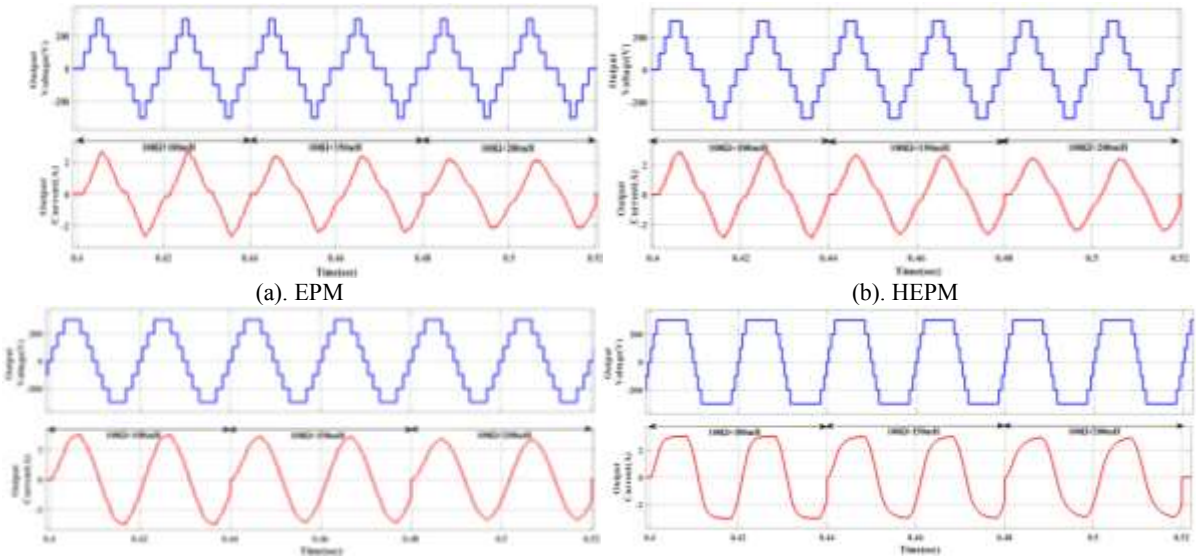
Fig. 7: Output Voltage and Current for R-Load (Seven-level topology)



(a). EPM (b). HEPM

(c). HHM (d).FFM

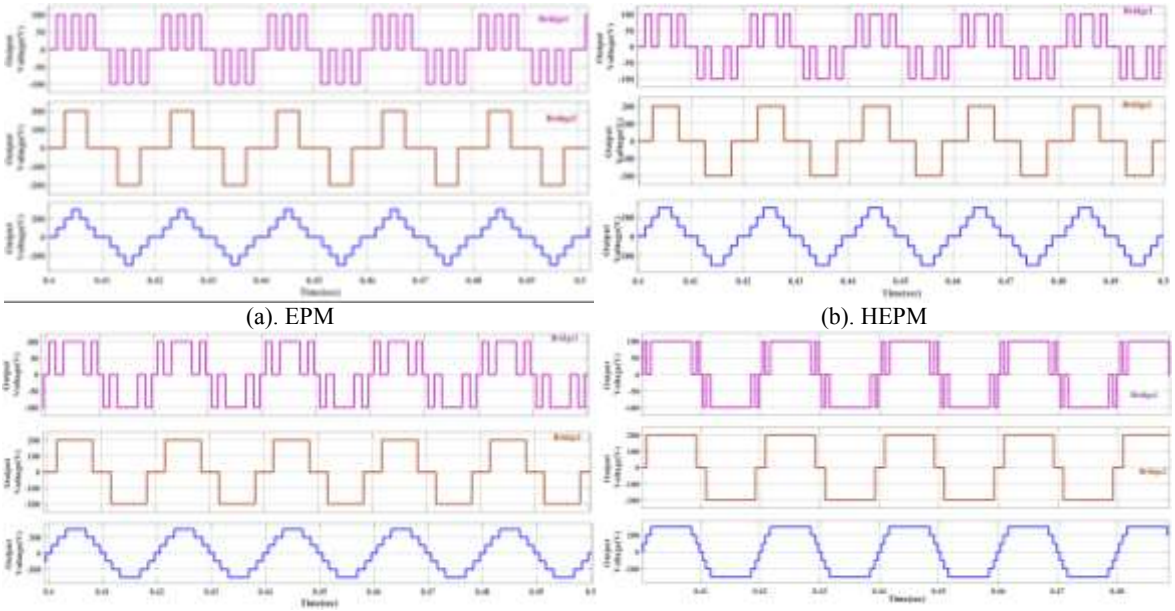
Fig. 8: Output Voltage and Current for various Loading conditions (Seven-level topology)



(a). EPM (b). HEPM

(c). HHM (d).FFM

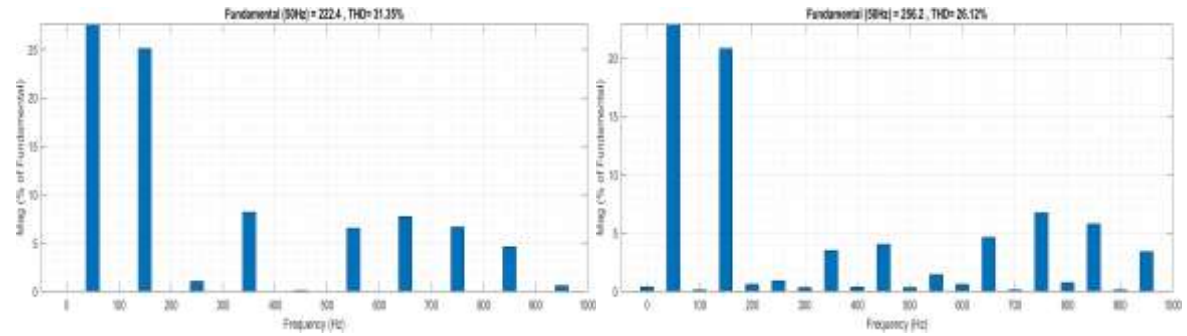
Fig. 9: Output Voltage and Current for various RL-Loads (Seven-level topology)



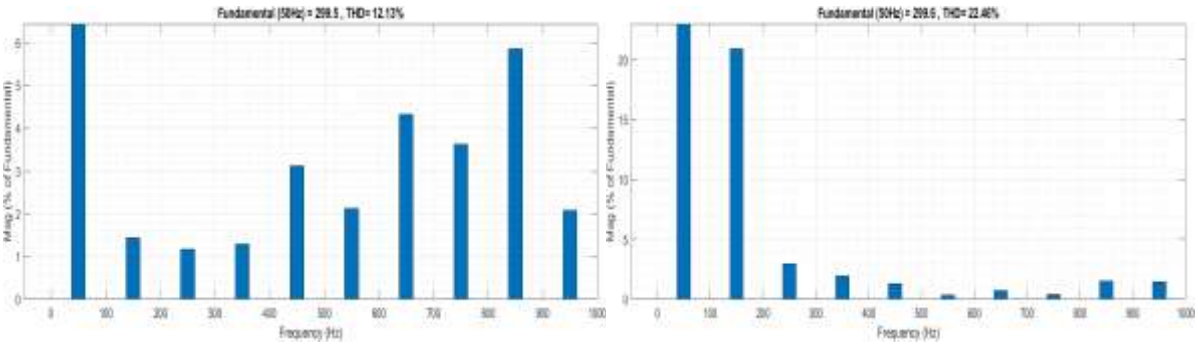
(a). EPM (b). HEPM

(c). HHM (d).FFM

Fig. 10: Output Voltage of individual bridges and Total output voltage (Seven-level topology)



(a). EPM (b). HEPM



(c). HHM (d).FFM

Fig. 11: Output voltage %THD (Seven-Level Topology)

Likewise, for nine-level topology various loading conditions are considered for validating the inverter output performance. Figure 12 shows the performance of the inverter under resistive loading conditions. From Figure 12, the current follows the output voltage. Figure 13 shows the operation of the inverter under various loading conditions. From Figure 13, it seems that there is no variation of output voltage whatever the circumstances, only current effects based on loading. if there is no load current does not flow, if it is resistive current follows voltage, if it is the sum of resistive and inductive then the current becomes lagging concerning voltage.

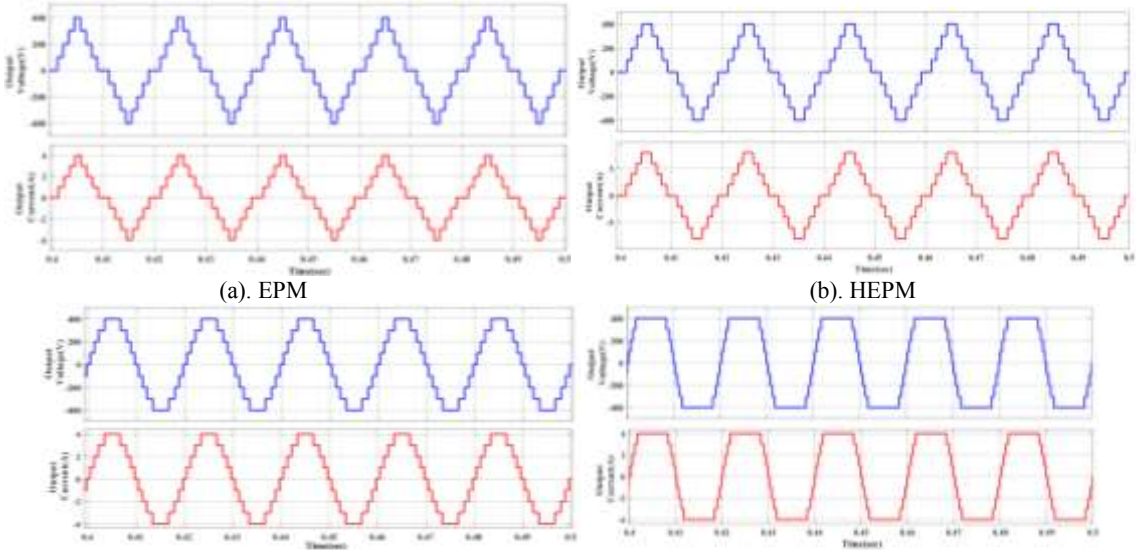
Figure 14 illustrates the operating condition of the inverter under different inductive loading conditions. From the observation of Figure 14, current reduces as load increases and becomes lagging in nature. In Figure 15 it represents three waveforms, first and second waveforms are the

voltage across bridge1and bridge2 and the third waveform is the total output voltage waveform respectively. The %THD of the nine-level topology is shown in Figure 16. It shows that 9.22% of THD for HHM is minimum than other methods.

Figure 17 portrays the switching patterns of the seven-level and nine-level topology for HHM respectively. Blue and red color indicates switching patterns of bridge1 and bridge2 respectively. Figure 18 illustrates a comparison of THD (%) for all the methods considering both topologies. It seems that whatever the topology HHM is superior compared to other methods. Following the simulation outcome, the suggested inverter works for all conditions of load.

4.2 Thermal Modelling

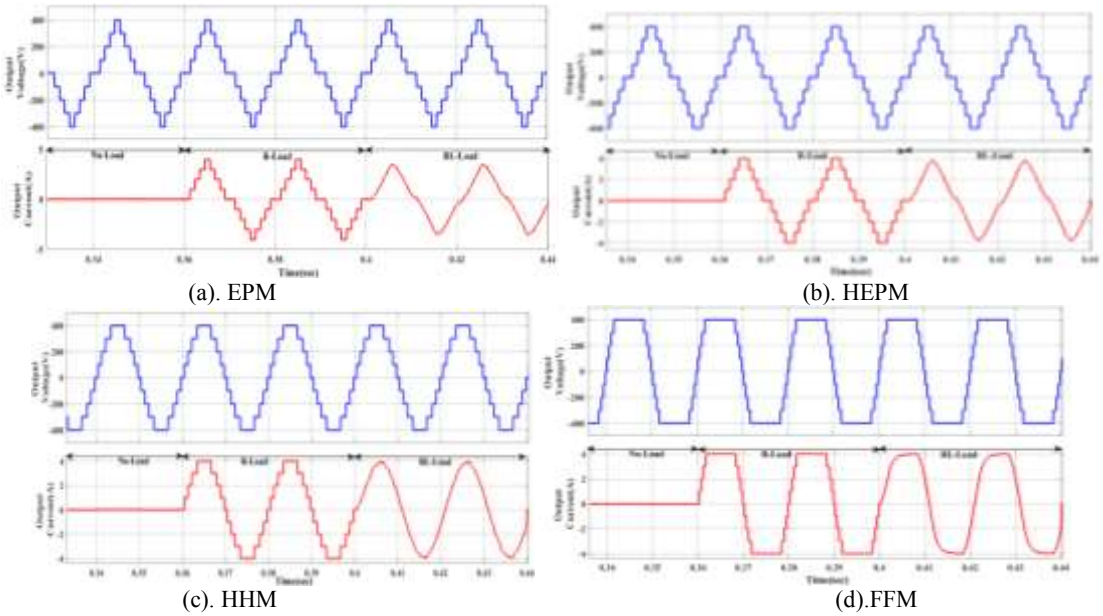
PLECS software serves to thermally model the power semiconductor devices of the suggested configuration. Figure 19(a) and (b) indicate the percentage of losses for semiconductor devices for seven-level operation at loading conditions of 100Ω and 100Ω +100mH respectively. The efficiency is computed through simply R loads and displayed in favor of the output power (0-5000W). Similarly, Figure 20(a) and (b) indicate the percentage of losses for nine-level operations under the previously specified loading conditions. As shown in Figure 21, the effectiveness spans 98.2% to 97.0%. The efficiency declines as the load grows. When load rises, conduction losses grow, which causes temperatures to rise, causing a decline in efficiency.



(a). EPM (b). HEPM

(c). HHM (d).FFM

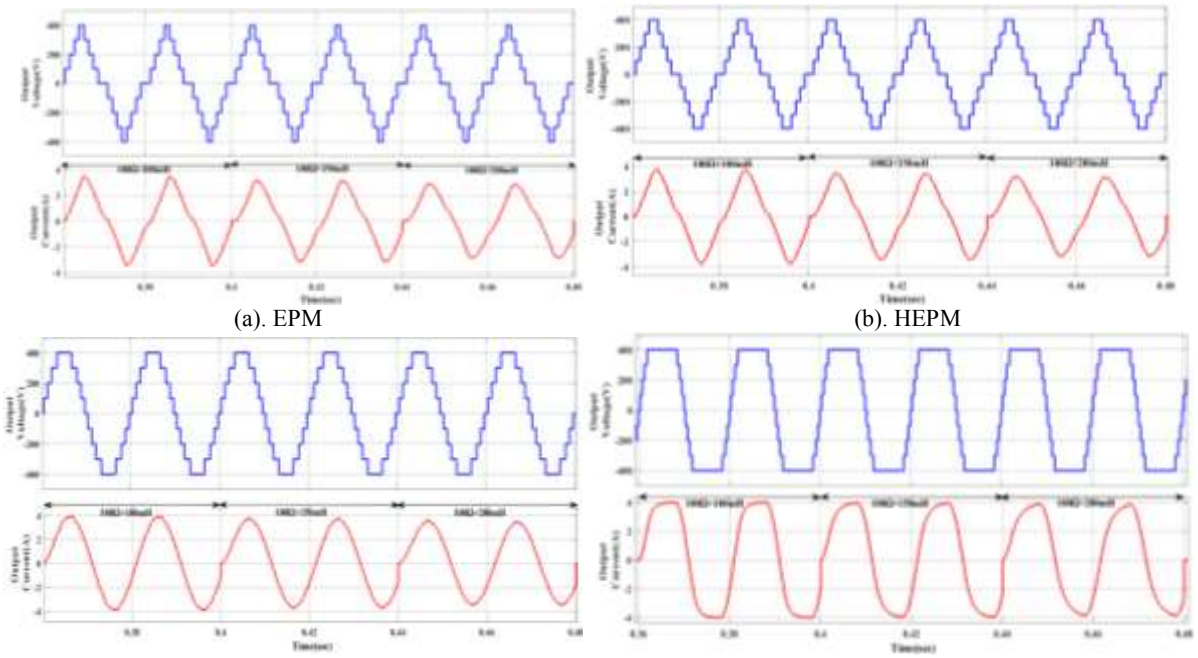
Fig. 12: Output Voltage and Current for R-Load (Nine-level topology)



(a). EPM (b). HEPM

(c). HHM (d).FFM

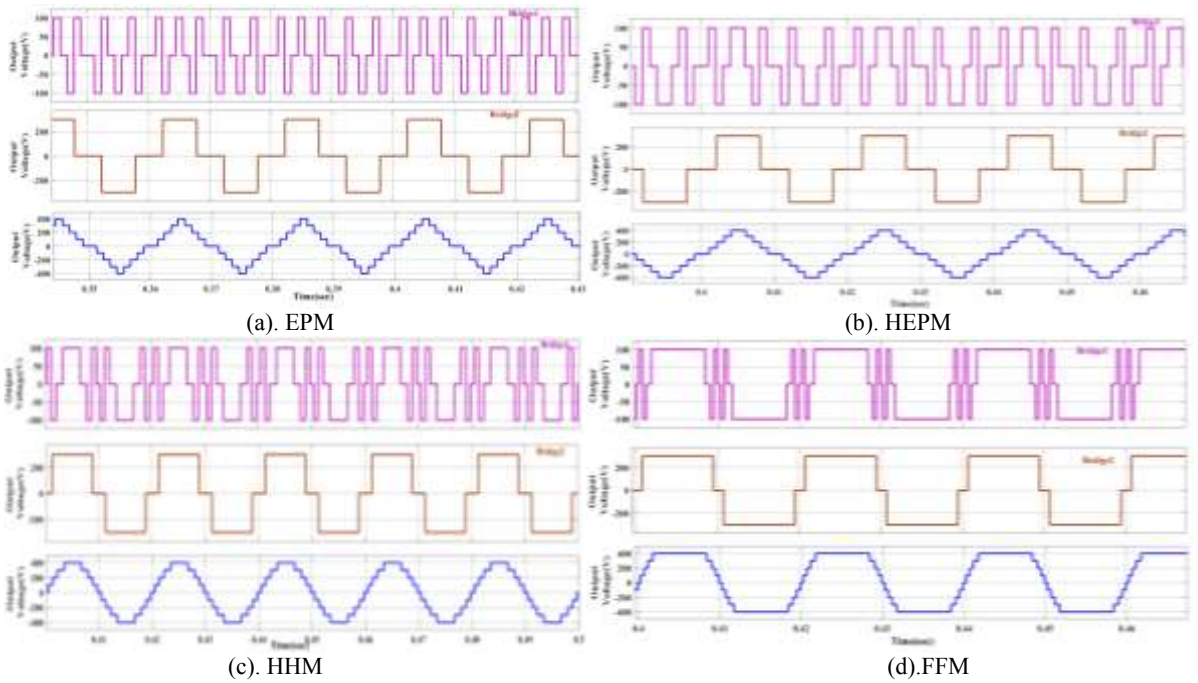
Fig. 13: Output Voltage and Current for various Loading conditions (Nine-level topology)



(a). EPM (b). HEPM

(c). HHM (d).FFM

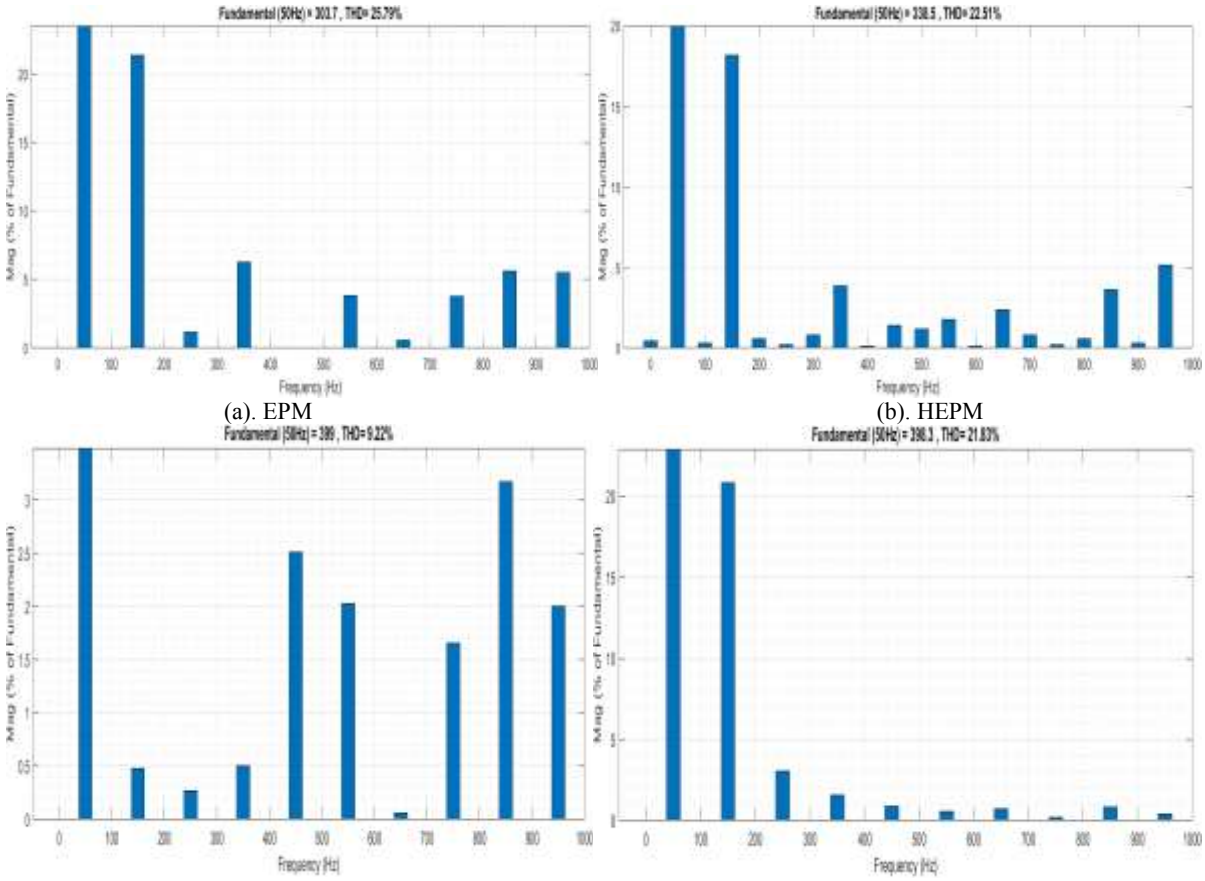
Fig. 14: Output Voltage and Current for various RL-Loads (Nine-level topology)



(a). EPM (b). HEPM

(c). HHM (d).FFM

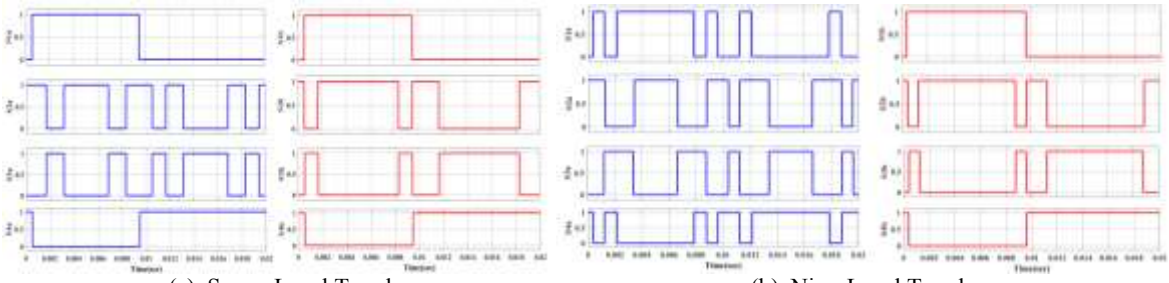
Fig. 15: Output Voltage of individual bridges and Total output voltage (Nine-level topology)



(a). EPM (b). HEPM

(c). HHM (d).FFM

Fig. 16: %THD of output voltage (Nine-Level Topology)



(a). Seven-Level Topology (b). Nine-Level Topology

Fig. 17: Switching patterns of switches for HHM

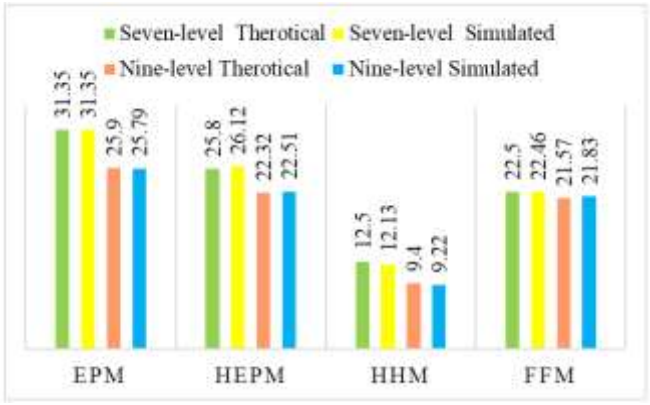
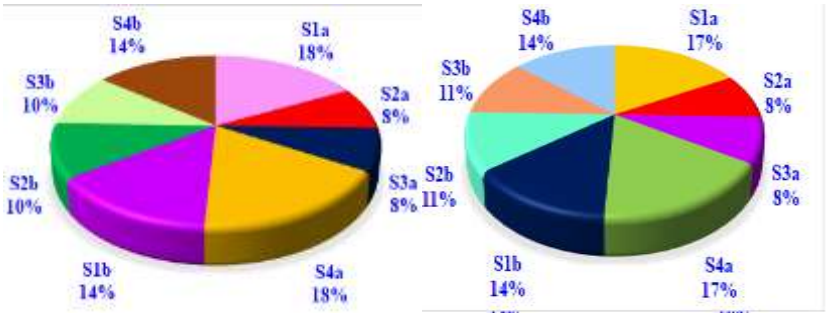


Fig. 18: Comparison of THD for all methods



(a). For R -Load (b). For RL- Load

Fig. 19: Percentage of losses for Seven-level Inverter

(a). For R -Load (b). For RL- Load

Fig. 20: Percentage of losses for Nine-level Inverter

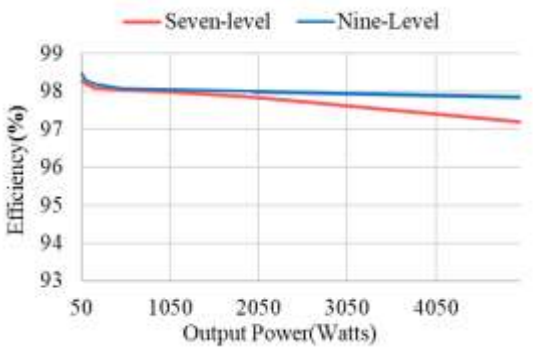
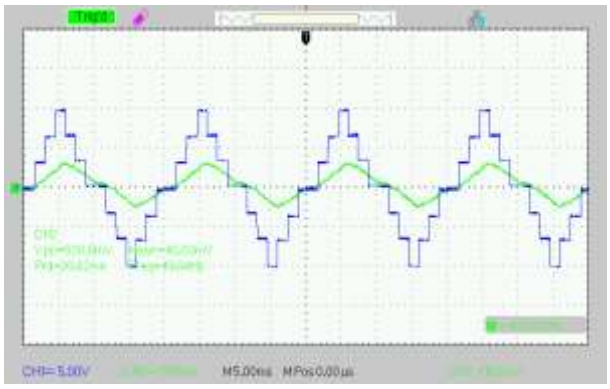


Fig. 21: Efficiency curves for Seven-level and Nine-level inverter

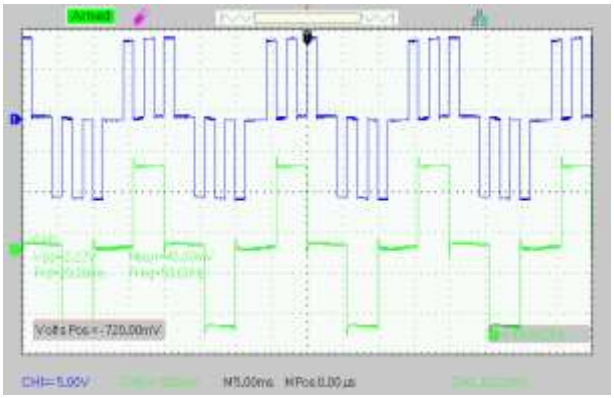
4.3 HIL Implementation

Real-time simulator plays a crucial role in designing and validating system effectiveness and accuracy since models built in real-time operate at an identical pace as real systems in existence. The OPAL-RT simulator links with the Sim Power System in MATLAB/Simulink employing the RT-LAB software. The OPAL-RT RT-LAB and eFPGAsim real-time platforms, along with advanced Intel processors and FPGA chips, are all bundled in the OP4510. This multi-rate FPGA-based architecture facilitates users to model power converters for HIL applications with a few time steps of less than 7 μs for INTEL CPU-based sections with a duration of fewer nanoseconds on the FPGA chip. Following that, an advanced PWM controller can regulate real hardware for Quick Control Modelling (QCM) services concerning timing improvement superior to 20 nanoseconds. The OP4510 can additionally serve as an independent semiconductor device test system with established models. All the methods related to seven-level and nine-level configurations are executed through OP4510 and are presented in this section.

The real time simulated results of seven-level operation correspond to four mitigation methods are illustrated in Figure 22, Figure 23, Figure 24 and Figure 25 respectively. The observation of the real time results shows that the HHM results of Figure 24 shows a better stepped waveform concerning other waveforms indicated in Figure 22, Figure 23 and Figure 25 respectively. For HHM both for R-Load and RL-Load the waveforms are presented. Therefore, from the real-time results HHM represents optimized results. The switching pulses of seven-level for HHM are depicted in Figure 26. Likewise, nine-level real-time results are indicated in Figure 27, Figure 28, Figure 29 and Figure 30 respectively. The switching pulses are shown in Figure 31. For the nine-level also HHM results are indicated as best results in contrast to other methods.

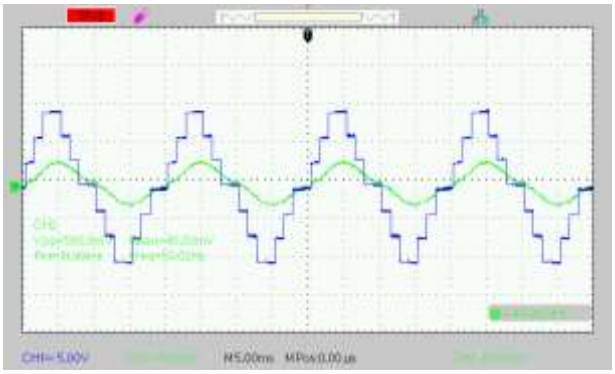


(a). Output Voltage and Current

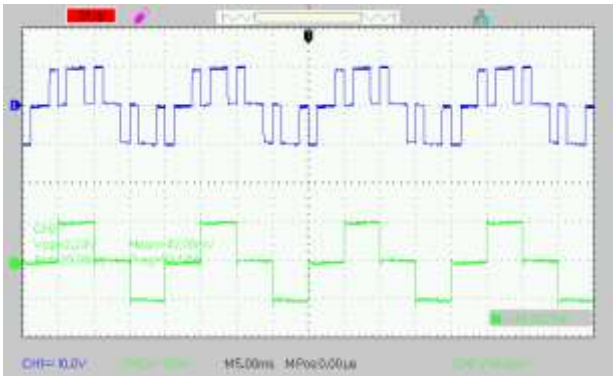


(b). Voltage appears across individual bridges

Fig. 22: EPM method results (Seven-level)

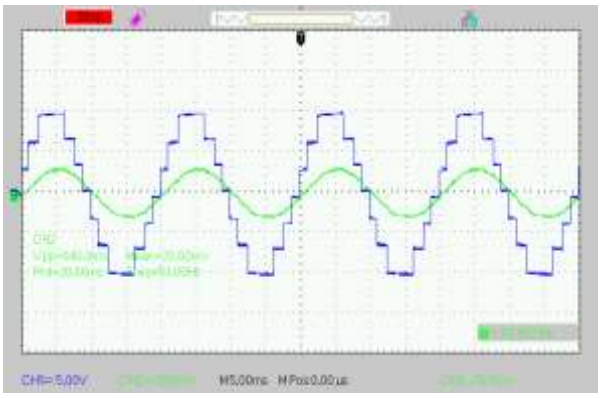


(a). Output Voltage and Current

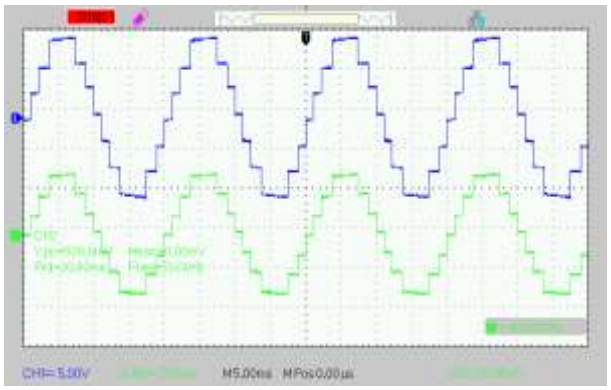


(b). Voltage appears across individual bridges

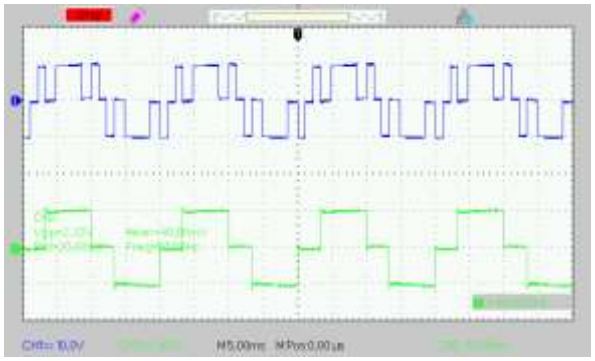
Fig. 23: HEPM method results (Seven-level)



(a). Output Voltage and Current for RL-Load

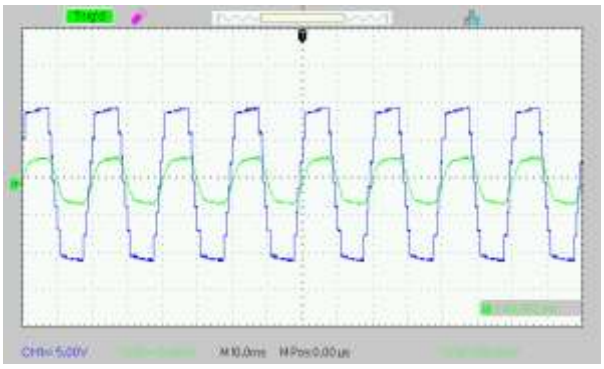


(b). Output Voltage and Current for R-Load

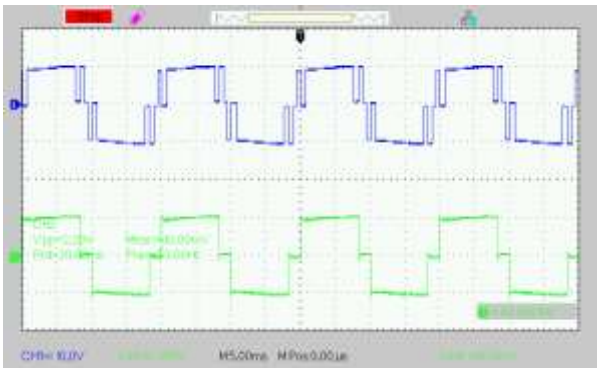


(c). Voltage appears across individual bridges

Fig. 24: HHM Results (Seven-level)

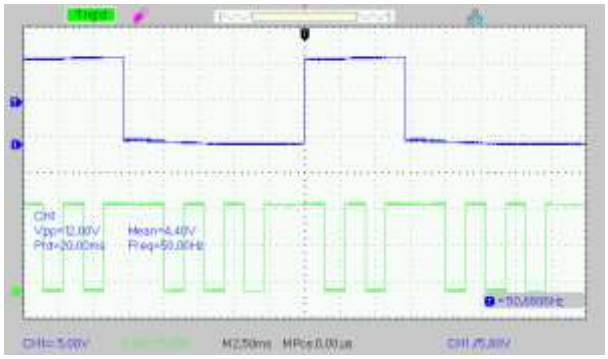


(a). Output Voltage and Current

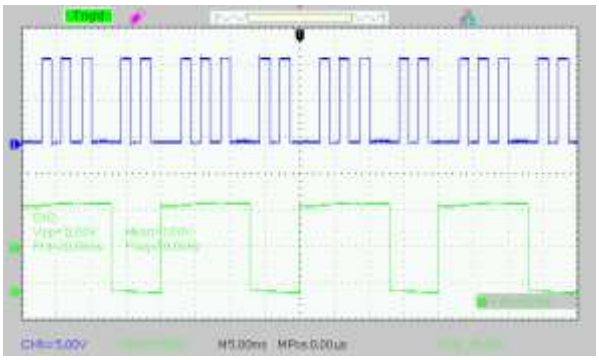


(b). Voltage appears across individual bridges

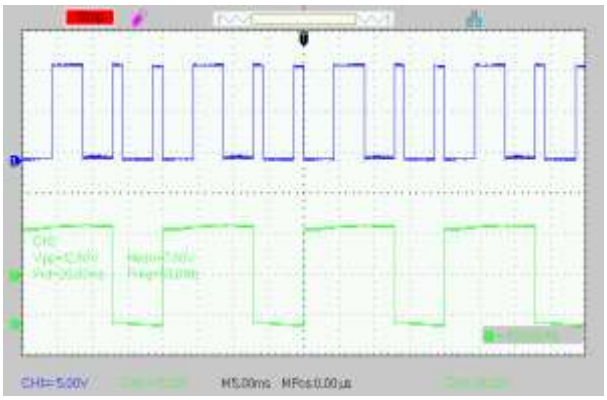
Fig. 25: FFM Results (Seven-level)



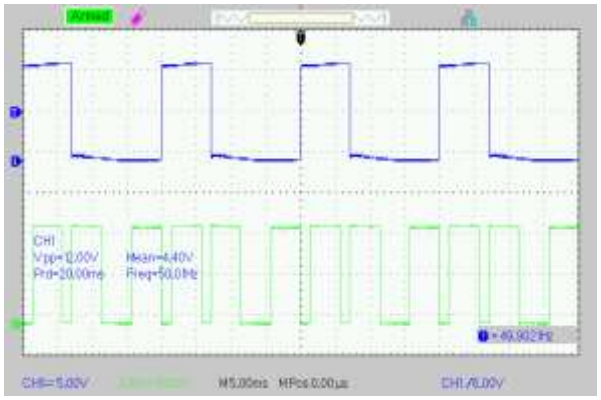
(a). (S_{1a}-S_{2a})



(b). (S_{3a}-S_{4a})

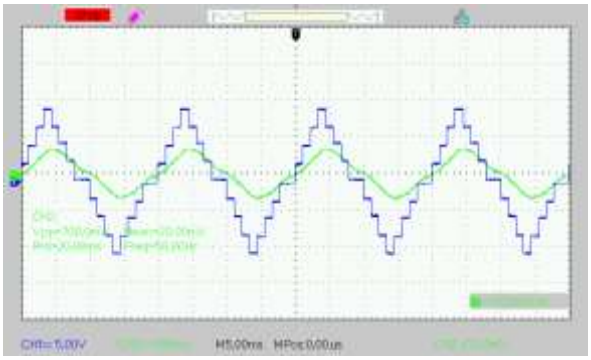


(c). (S_{1b}-S_{2b})

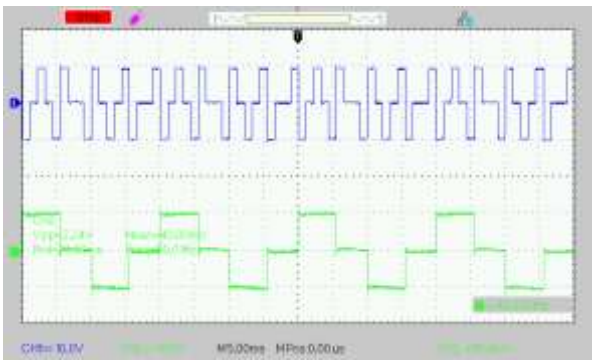


(d). (S_{3b}-S_{4b})

Fig. 26: Switching pulses of HHM(Seven-level)

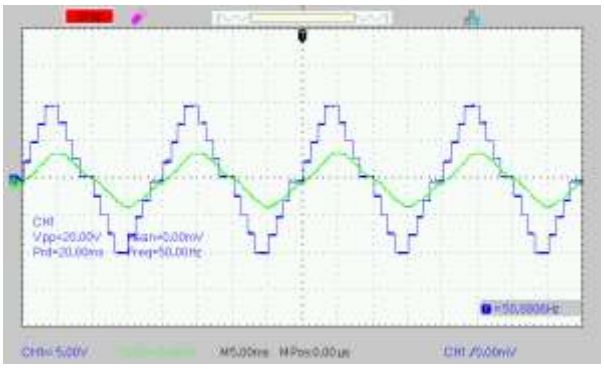


(a). Output Voltage and Current

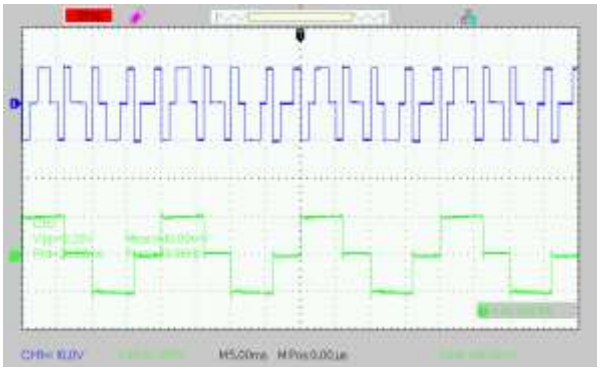


(b). Voltage appears across individual bridges

Fig. 27: EPM Results (Nine-level)

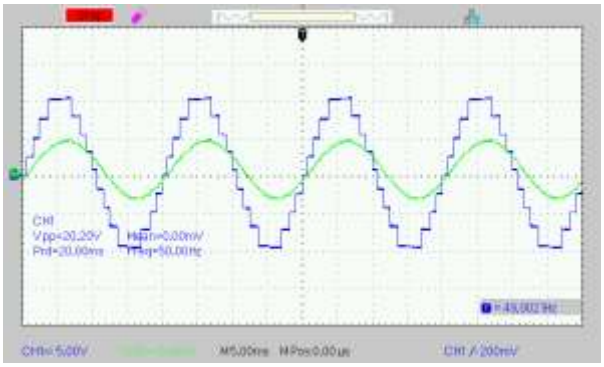


(a). Output Voltage and Current

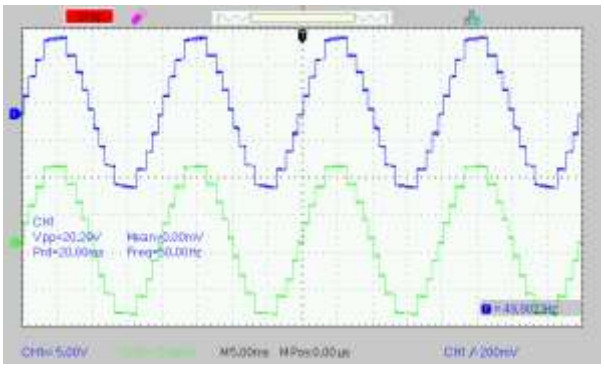


(b). Voltage appears across individual bridges

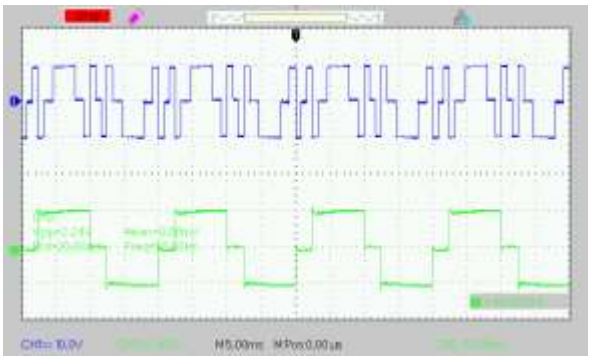
Fig. 28: HEPM Results (Nine-level)



(a). Output Voltage and Current for RL-Load

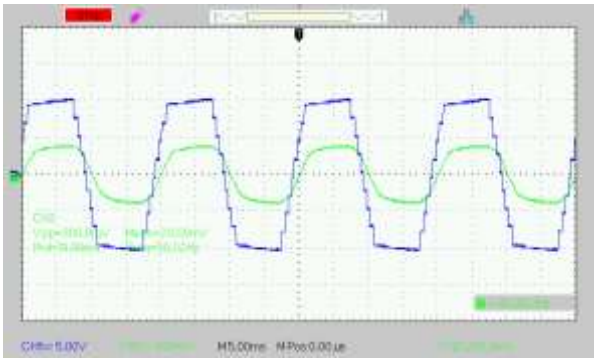


(b). Output Voltage and Current for R-Load

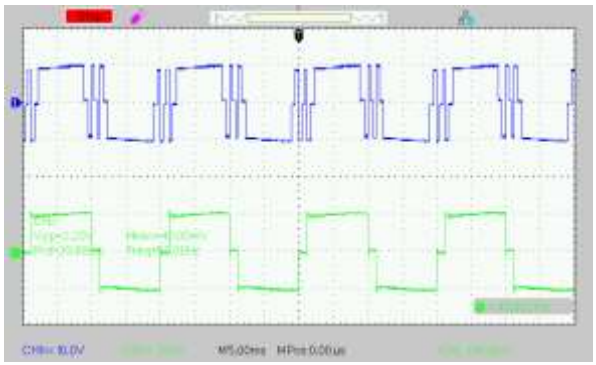


(c). Voltage appears across individual bridges

Fig. 29: HHM Results (Nine-level)

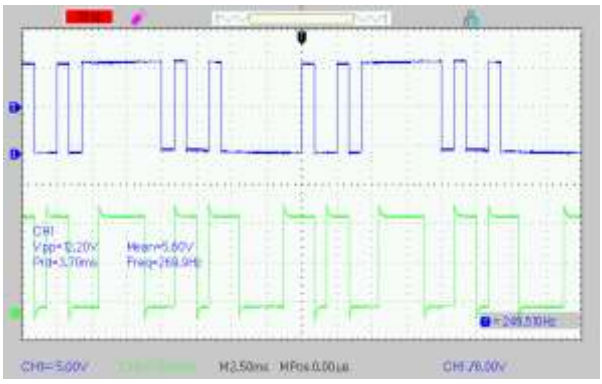


(a). Output Voltage and Current

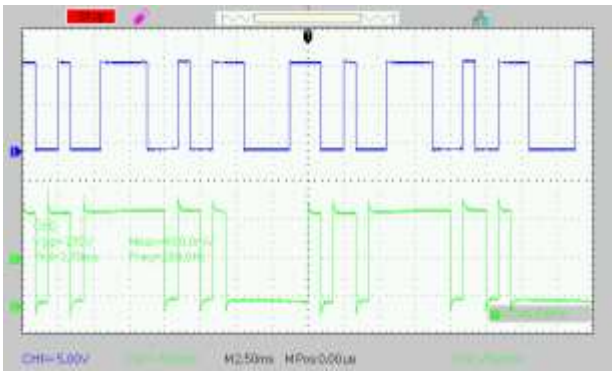


(b). Voltage appears across individual bridges

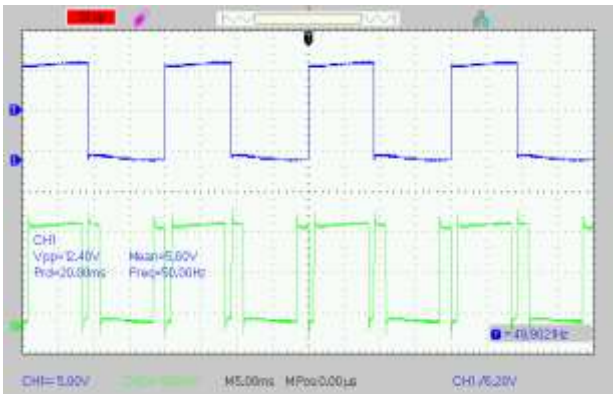
Fig. 30: FFM Results (Nine-level)



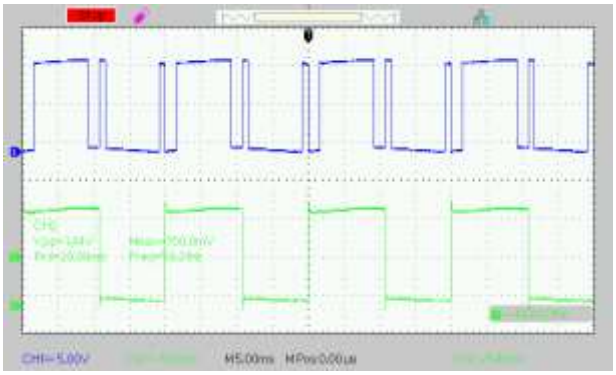
(a).(S_{1a}-S_{2a})



(b). (S_{3a}-S_{4a})



(c). (S_{1b}-S_{2b})

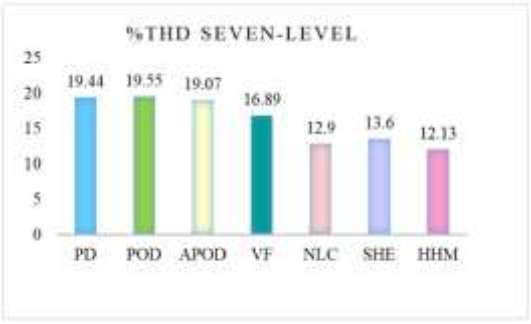


(d). (S_{3b}-S_{4b})

Fig. 31: Switching pulses of HHM(Nine-level)

5 Comparison

Figure 32(a) represents the %THD of various modulation techniques simulated for asymmetrical seven-level topology. In Figure 32 PD (Phase Disposition), POD (Phase Opposition Disposition), APOD (Alternate Phase Opposition and Disposition) and VF (Variable Frequency) are methods that come under High frequency (HF) modulation scheme respectively. The remaining methods like NLC (Nearest Level Control), SHE (Selective Harmonic Elimination), and HHM (Half Height Method) are Low-frequency modulation schemes respectively. In contrast to the HF scheme LF scheme gives a better %THD but based on the application respective control scheme is utilized for respective configurations.



(a). Seven-level Topology

(b). Nine-level Topology

Fig. 32: %THD of various control schemes

Table 6.Calculated %THD of seven-level and nine-level topology

Level Of Operation	Switches Count		%Reduction of Switches Count
	Symmetrical Configuration	Asymmetrical Configuration	
Seven-level	12	8	33.33
Nine-level	16	8	50

In LF schemes comparison to other methods %THD is the minimum for the HHM scheme. The method of implementation of HHM is easily computed in a simulation environment. In the same fashion, Figure 32(b) represents %THD of distinct schemes for asymmetrical nine-level configuration. For this case also HHM method also gives the best results concerning %THD consideration. Table 6 indicates a reduction of the switch count of the asymmetric configuration in contrast to the symmetrical configuration. For instance, the switches count for seven-level operation corresponds to symmetric and asymmetric are 12 and 8 respectively. Therefore % reduction of switch count is 33.3% in comparison to symmetric configuration. As mentioned in Table 6, for nine-level operation reduction of switch count is 50%. As the level of operation rises asymmetrical configuration requires minimum switches, therefore cost factor reduces for asymmetrical configuration.

6 Conclusion

In this work mitigation techniques are implemented for seven and nine-level of the asymmetric CHB topology. The mathematical equations utilized by all the methods are presented. In comparison to other harmonic mitigation methods, the real-time as well as simulation results indicate that the HHM offers the lowest THD. Furthermore, the HHM achieves superior RMS output voltage and current with precise maximum output voltage and current results. The suggested structure leads to a smaller size, minimum component losses, along with lower costs for installation. By using PLECS software total losses are measured. In addition, the suggested configuration has reduced conduction and switching losses for accomplishing unique criteria in terms of cost factor and effectiveness. Generally, photovoltaic panels through appropriate control methods are capable of being incorporated with the proposed topology for showing execution of the grid either in on or off issues via an effective layout.

References:

[1] J. Rodríguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, Aug. 2002, doi: 10.1109/TIE.2002.801052.

[2] S. Kouro, Malinowski, Gopakumar.K, Josep Pou, L.G. Franquelo, BinWu, J. Rodriguez, Parez, Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp.2553–2580, Aug.2010, doi:10.1109/TIE.2010.2049719.

[3] S. De, D. Banerjee, K. Siva Kumar, K. Gopakumar, R. Ramchand, and C. Patel, "Multilevel inverters for low-power application," *IET Power Electronics*, vol. 4, no. 4, pp. 384–392, Apr. 2011, doi: 10.1049/iet-pel.2010.0027.

[4] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters State of the art, challenges, and requirements in Industrial applications," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2581–2596, Aug. 2010, doi: 10.1109/TIE.2010.2043039.

[5] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 7. pp. 2197–2206, Jul. 2010. doi: 10.1109/TIE.2009.2030767.

[6] A. Salem, H. Van Khang, K. G. Robbersmyr, M. Norambuena, and J. Rodriguez, "Voltage Source Multilevel Inverters with Reduced Device Count: Topological Review and Novel Comparative Factors," *IEEE Trans Power Electron*, vol. 36, no. 3, pp. 2720–2747, Mar. 2021, doi: 10.1109/TPEL.2020.3011908.

[7] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Transactions on Power Electronics*, vol. 31, no. 1. pp. 135–151, Jan. 01, 2016. doi: 10.1109/TPEL.2015.2405012.

[8] P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano, and G. Panda, "Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation," *IEEE Access*, vol. 7, pp. 54888–54909, 2019, doi: 10.1109/ACCESS.2019.2913447.

[9] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson, "A General Review of Multilevel Inverters Based on Main Submodules: Structural Point of View," *IEEE Trans Power Electron*, vol. 34, no. 10, pp. 9479–9502, Oct. 2019, doi: 10.1109/TPEL.2018.2890649.

[10] H. P. Vemuganti, D. Sreenivasarao, S. K. Ganjikunta, H. M. Suryawanshi, and H. Abu-Rub, "A survey on reduced switch count multilevel inverters," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 80–111, 2021, doi: 10.1109/OJIES.2021.3050214.

[11] V. K. N. V. and G. T, "A comprehensive survey on reduced switch count multilevel inverter topologies and modulation techniques," *Journal of Electrical Systems and Information Technology*, vol. 10, no. 1, Jan. 2023, doi: 10.1186/s43067-023-00071-8.

[12] A. Poorfakhraei, M. Narimani, and A. Emadi, "A Review of Modulation and Control Techniques for Multilevel Inverters in Traction Applications," *IEEE Access*, vol. 9., pp. 24187–24204, 2021. doi: 10.1109/ACCESS.2021.3056612.

[13] J. Napoles, Alan J. Watson, JoseJ.Padilla, JoseI.Leon, LG. Franquelo, PW. Wheeler, M.A. Aguirre, "Selective Harmonic Mitigation Technique for Cascaded H-Bridge Converters with Nonequal DC Link Voltages," in *IEEE Transactions on Industrial*

Electronics, vol. 60, no. 5, pp. 1963-1971, May 2013, doi: 10.1109/TIE.2012.2192896.

[14] J. N. Chiasson, L. M. Tolbert, Z. Du, and K. J. McKenzie, "The use of power sums to solve the harmonic elimination equations for multilevel converters," *EPE Journal (European Power Electronics and Drives Journal)*, vol. 15, no. 1, pp. 19–27, 2005, doi: 10.1080/09398368.2005.11463578.

[15] M. S. A. Dahidah, G. Konstantinou, and V. G. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications," *IEEE Trans Power Electron*, vol. 30, no. 8, pp. 4091–4106, 2015, doi: 10.1109/TPEL.2014.2355226.

[16] H. Taghizadeh and M. Tarafdar Hagh, "Harmonic elimination of multilevel inverters using particle swarm optimization," 2008 *IEEE International Symposium on Industrial Electronics*, Cambridge, UK, 2008, pp. 393-396, doi: 10.1109/ISIE.2008.4677093.

[17] H. Taghizadeh and M. Tarafdar Hagh, "Harmonic elimination of cascade multilevel inverters with nonequal dc sources using particle swarm optimization," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 11, pp. 3678–3684, Nov. 2010, doi: 10.1109/TIE.2010.2041736.

[18] K. El-Naggar and T. H. Abdelhamid, "Selective harmonic elimination of new family of multilevel inverters using genetic algorithms," *Energy Convers Manag*, vol. 49, no. 1, pp. 89–95, Jan. 2008, doi: 10.1016/j.enconman.2007.05.014.

[19] F. A. Silva, "Advanced DC/AC Inverters: Applications in Renewable Energy (Luo, F.L. and Ye, H.; 2013) [Book News]," *IEEE Industrial Electronics Magazine*, vol. 7, no. 4, pp. 68–69, Dec. 2013, doi: 10.1109/mie.2013.2289564.

[20] J. I. Guzman, P.E. Melin, J.R. Espinoza, L.A. Moran, C.R. Baier, J.A. Munoz, G.A. Guinez, "Digital Implementation of Selective Harmonic Elimination Techniques in Modular Current Source Rectifiers," in *IEEE Transactions on Industrial Informatics*, vol. 9, no. 2, pp. 1167-1177, May 2013, doi: 10.1109/TII.2012.2210232.

[21] F. Ait bellah, A. Abouloifa, S. Echalih, Z. Hekss, K. Naftahi, I. Lachkar, Control Design of a Seven-Level Packed U Cell Inverter, *IFAC-PapersOnLine*, Vol. 55, Issue 12, 2022, Pages 677-682, ISSN: 2405-8963, https://doi.org/10.1016/j.ifacol.2022.07.390.

[22] A. M. Rao, V. Srinivas, and B. Srividya, "Seven-Level Single Phase Inverter for Multistring Photovoltaic Applications," *2020 IEEE International Conference on Power Electronics, Smart Grid and Renewable Energy (PESGRE2020)*, Cochin, India, 2020, pp. 1-6, doi: 10.1109/PESGRE45664.2020.9070361.

[23] E. Parimal Sundar, S. Jayakumar, P. Nagajothi, V. S. Chandrika, T. Devaraju, and K. Suresh, "Enhanced Design and Performance Analysis of a Seven-Level Multilevel Inverter for High-Power Applications," *2023 Second International Conference on Augmented Intelligence and Sustainable Systems (ICAISS)*, Trichy, India, 2023, pp. 1862-1868, doi: 10.1109/ICAISS58487.2023.10250516.

[24] D. K. Patel, N. K. Dewangan, D. Kumar and A. Rathore, "Seven-Level Single-Phase Reduced Device Count Multilevel Inverter," *2023 IEEE International Students' Conference on Electrical, Electronics and Computer Science (SCEECS)*, Bhopal, India, 2023, pp. 1-5, doi: 10.1109/SCEECS57921.2023.10063035.

[25] J. A. Lone and F. I. Bakhsh, "Design and Analysis of Cascaded H Bridge Nine-Level Inverter in Typhoon HIL," *IOP Conf Ser Mater Sci Eng*, vol. 804, no. 1, p. 012049, Apr. 2020, doi: 10.1088/1757-899X/804/1/012049.

[26] A. Sarwar, M. I. Sarwar, M. S. Alam, S. Ahmad, and M. Tariq, "A Nine-Level Cascaded Multilevel Inverter with Reduced Switch Count and Lower Harmonics," in *Lecture Notes in Electrical Engineering, Springer Verlag*, 2019, pp. 723–738. doi: 10.1007/978-981-13-6772-4_62.

[27] P. K. Chamarthi, V. Agarwal, M. El Moursi, and V. Khadkikar, "Novel 1-φ Dual Input Nine-Level Inverter Topology With Generalized Modulation Technique," *IEEE Transactions on Energy Conversion*, vol. 37, no. 3, pp. 1789–1802, Sep. 2022, doi: 10.1109/TEC.2022.3140232.

[28] D. Niu, F. Gao, P. Wang, K. Zhou, F. Qin, and Z. Ma, "A Nine-Level T-Type Packed U-Cell Inverter," *IEEE Trans Power Electron*, vol. 35, no. 2, pp. 1171–1175, Feb. 2020, doi: 10.1109/TPEL.2019.2931523.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The authors equally contributed to the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The authors have no conflicts of interest to declare.