

# Power Loss Analysis with Dispersed Generation in Multifunction Power Conditioner Design to Improve Power Quality

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*Abstract:* - The recent modification in utilizing Multifunction Power Conditioner (MPC) such as Unified Power Quality Conditioner devices in power systems has led to different degrees of power losses, owing to electronic power impacts. This paper presents a detailed comparison of power loss analysis in various configurations of MPC, that is, the conventional unified power quality conditioner (UPQC) and the UPQC with distributed generation ( $UPQC_{DG}$ ). The independent losses based on inverter design and distributed generation interfacing to the distribution form the basis for each configuration case. The investigation considered conventional UPQC as the base case for power losses, and the study was extended to  $UPQC_{DG}$  at steady state operating condition. In all configurations, Switching Losses (SL) and conduction losses were considered using simulation studies carried out in MATLAB/SIMULINK, and the results obtained in all cases were used for comparative studies. Finally, the outcome indicates that the losses in  $UPQC_{DG}$  is more than conventional UPQC based on simulation results in all cases.

*Keywords:* - Multifunction Power Conditioner (MPC), Switching Losses (SL), Distributed Generation (DG), Active power filter, Photovoltaic (PV) solar, Unified Power Quality Conditioner (UPQC)

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## 1 Introduction

The advancement of power electronic technology enables the realization of numerous types of Flexible Alternating Current Transmission Systems Devices (FACTSD) to obtain high-quality electrical energy and improve power system control in which Unified Power Quality Conditioner (UPQC) is inclusive [1]. The UPQC can improve power quality at the point of common coupling of distribution systems, [2], [3]. Nevertheless, owing to the recent universal use of non-linear loads and the laborious progress of power electronics devices application, many power quality (PQ) challenges are experienced in power systems resulting in power losses, lack of efficiency, and reduction in the life span of equipment, [4], [5], [6], resulted to the

economic degradation and the cost of maintenance of distribution apparatus, [6].

Most of the electronic equipment used is microprocessor-based and extremely sensitive to power quality. Power quality issues such as voltage swell, sag, interruptions, and different kinds of harmonics pose a challenge to utilities. However, UPQC appears to be a comprehensive solution for PQ amelioration [7], though they come in various configurations and diverse control architectures.

A good algorithm design is necessary for any power electronics-based device for overall system efficacy. Various algorithms/control systems have been devised to control, compensatory custom devices. In the case of UPQC, it offers some varieties of control approaches such as Power Angle Control (PAC), [8], [9], Synchronous reference

strategy is considered in [10], the technique of unit vector format production is employed in, [11], model predictive regulator (MPR) in, [12] are common in literature. All these control methods have proved effective for different configurations.

The UPQC design allows for electric charge and potential difference correction via a parallel/series active power filter, [13]. The electric charge-associated issues, such as the proportion of real power consumed by the load to the apparent power flowing through the network and unbalanced electric charges flow, are being taken by shunt inverter that act as current sources while series inverter functions as a voltage source to mitigate voltage-related challenges such as voltage dip and swell. The UPQC also takes the advantage offered by distributed generation as an alternative source connected via the DC link to compensate for PQ issues [14], [15].

The pairing of multifunction power conditioners with distributed energy resources has the potential to transfer imaginary energy assistance to a distributed network. In comparison to fundamental UPQC, the UPQC link with DG has too numerous advantages such as better DC link regulation that offer improved PQ compensation, exclusion of dear grid integration inverter demand for DG, capacity to ameliorate for source voltage interruptions, the flexibility of shunt and series inverter control, and it fosters clean energy production.

The various configurations of UPQC suffer from different degrees of power losses, regardless of the numerous advantages they offer, and it must be quantified in order for its overall performance to be assessed. The UPQC power losses have been investigated for different control architectures in, [16], [17] and  $UPQC_{DG}$ . Power losses are given in, [9]. The concept of UPQC and  $UPQC_{DG}$  in the literature are discussed extensively nevertheless, the power loss quantification that comprises switching and modeling losses are not considered. This is due to recent modification in utilizing Multifunction Power Conditioner (MPC) such as Unified Power Quality Conditioner devices in power systems, which has led to different degrees of power losses, owing to electronic power impacts and DG integration.

When evaluating the effectiveness of a multifunction power conditioner in alleviating PQ problems in a network with DGs connected, it is worthwhile to investigate energy losses/dissipation across the distribution grid. This study attempted to compare the energy losses generated when employing MPC to alleviate power quality in a traditional network and when renewable distributed

generation is connected to the network. The power losses have been investigated for several operational scenarios, including steady-state, voltage dip, swell, the stochastic nature of irradiation, and load change. A non-linear load is considered in this study. All investigations of the designs were carried out in MATLAB/Simulink when series inverter of a UPQC compensates for voltage while its shunt counterpart compensates for reactive power. The research findings are summarized below:

- The calculation of power loss of conventional UPQC and  $UPQC_{DG}$  installation in a distribution network.
- The calculation of the power losses resulting from DG integration using a UPQC and DC-DC converter.
- The advantages that conventional UPQC has over  $UPQC_{DG}$  owing to the losses.

Therefore, the major contribution of this study is the application of power angle control in shunt inverters to enable them to participate in voltage amelioration, while the percentage loss per PV integration is kept at reasonable level as well.

The remainder of the paper is organized as follows: The MPC circuit construction, configurations of UPQC,  $UPQC_{DG}$ , and controls are considered in Section 2. The power loss evaluation details were presented in Section 3. Finally, MATLAB/Simulink results presented power loss comparisons in Section 4. Section 5, which wraps up the investigation and results, completes the paper.

## 2 Construction and Control

The single-phase wire type of UPQC is considered for the study because the bulk of alternating current energy is managed by employing a one-phase approach. The concept of  $UPQC_{DG}$  is displayed in Figure 1. Following is a discussion of the design and control schemes for UPQC and  $UPQC_{DG}$ .

### 2.1 Fundamental UPQC

The parallel active power filter (APF) named (DSTATCOM) is integrated across the load side in this configuration to address current-related issues, and the series active power filter is linked across the sending end to regulate the potential difference associated issues. Both APF (shunt and series inverter) necessitate a stable potential difference in the direct current connection to complete those activities. To achieve an error-free signal generated by a parallel connected inverter, a direct current-link

voltage is made greater than twice the maximum alternating current network voltage, [18]. Shunt APF's main job is to regulate the direct current-link voltage at a predetermined stage.

Dynamic voltage restorer (DVR) infuses voltage using single-phase transformers to maintain this same load voltage somewhere at the reference level. Figure 2 depicts the phasor illustration of the UPQC in the dip disorder, [19], when the dip/swell disorder occurs, the voltage is infused in series with the sending end voltage.

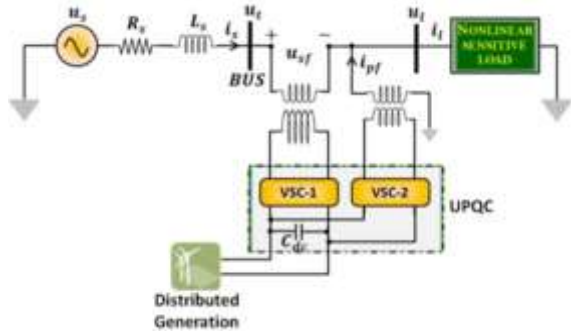


Fig. 1: Structure of UPQC and distributed generation [20]

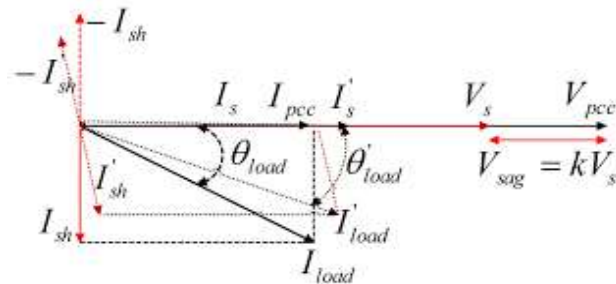


Fig. 2: A UPQC schematic phasor illustration

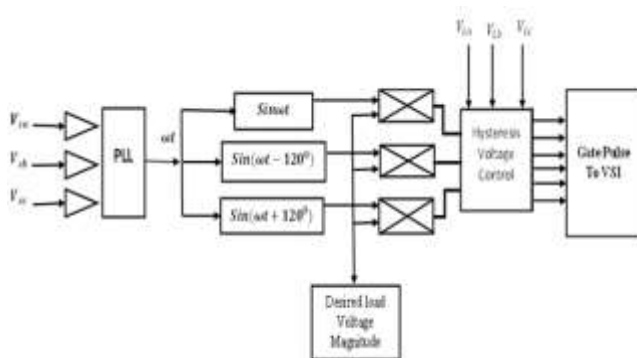


Fig. 3: Control framework for series APF [13]

This section describes the series active filter's control strategy. Unit direction pattern production is the control approach applied to monitor the DVR. A reference voltage signal is produced, which is displayed in Figure 3. To regulate the error voltage generated at the Connection Point (PC),

countersignals are created to block a large part of external error sources resulting in the correct voltage magnitude at the PC. The series active power filter regulates sags of different levels for varying durations. To accomplish supply voltage synchronization, the phase lock loop is utilized.

Two quadrature unit vectors are produced as the PLL's output, and they are synchronized with sine and cosine. Using the equations below, this outcome is employed to calculate the input synchronization for the three-unit vectors ( $V_a$ ,  $V_b$ , and  $V_c$ ) that are  $120^\circ$  out of phase, [20], [21].

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & -\sqrt{\frac{3}{2}} \\ -\frac{1}{2} & \sqrt{\frac{3}{2}} \end{bmatrix} \times \begin{bmatrix} \sin\theta \\ \cos\theta \end{bmatrix} \quad (1)$$

Equation (1) computed unit vectors multiply by the intended PCC peak voltage ( $V_m$ ), which is regarded as the standard PCC voltage.

$$\begin{bmatrix} V_{la} \\ V_{lb} \\ V_{lc} \end{bmatrix} = V_m \times \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \quad (2)$$

Comparing the reference voltage calculated using the control method to the detected PCC voltage ( $V_{la}$ ,  $V_{lb}$ ,  $V_{lc}$ ) will provide distortion that is supplied to the regulator of the lagging between input and output in the system upon a change in direction (hysteresis). The output of the regulator produces the gate pulse for the series converter. The regulator determines how switching sequences occur, and the DVR infuses potential differences appropriately. The following expression can be used to compute the amount of injected voltage derived from Figure 4.

$$V_{injected} = V_{load} - V_{source} \quad (3)$$

$V_{injected}$  denote converter-infused voltage,  $V_{load}$  load voltage,  $V_{source}$  Source Voltage.

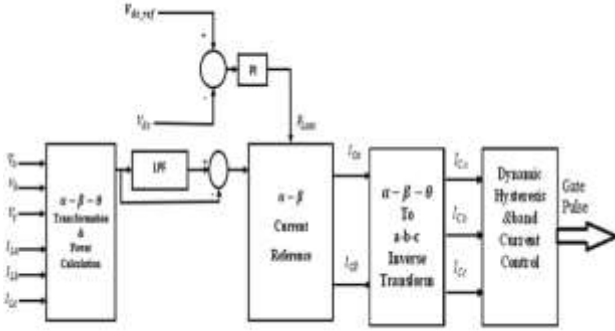


Fig. 4: Block of parallel APF controller

## 2.2 The UPQC<sub>DG</sub>

As depicted in Figure 1, a direct current-to-direct current Boost Converter is employed to link the Photovoltaic module to the DC link. The load is connected to the parallel active power filter, while the sending end is integrated with the series active power filtering circuit. It is anticipated to enhance the UPQC performance because the UPQC can use the electricity provided by the PV array to make up for power outages and because the feed-forward gain enhances the DC-link response. To satisfy the energy demand by the loads, ameliorating currents ( $I_{Ca}^*$ ,  $I_{Cb}^*$ ) are needed. The a-b-c coordinates of these amelioratory currents are converted from the  $\alpha - \beta$ -coordinate using Equation (4).

$$\begin{bmatrix} I_{Ca} \\ I_{Cb} \\ I_{Cc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \times \begin{bmatrix} I_{C\alpha}^* \\ I_{C\beta}^* \end{bmatrix} \quad (4)$$

The Boost Converter (BC) causes interference with the PV array DC link. The highest allowable voltage and current from the photovoltaic systems are used while increasing the voltage at the output terminal. A less complex method known as the Incremental conductance (IC) approach is utilized to access the peak power point as indicated in equation (5), [20]:

$$\frac{dI}{dV} = \frac{-I}{V} \quad (5)$$

The BC is designed in such a way that the output is nearly equivalent to the direct current link controller set point, while the parallel active power filter resists the maximum power generated by the Photovoltaic modules.

## 3 Power Loss Calculation

There are 12 active switches on each of the two voltage source inverters, and together they make up

the 3- $\theta$ , 3-wire UPQC. One more active boost converter switch is present in the UPQC<sub>DG</sub> configuration. The conduction losses are produced by the device's current and the reduction in voltage along the line. Conduction losses are also significantly influenced by the total series resistor (TSR) of passive elements and the resistance of semiconductor switches in their on-state. Also directly related to these losses is the duty cycle. SL is yet another substantial contributor to losses in addition to conduction losses.

The active behaviour of IGBTs, the full wave rectifier, and the BC diode, are considered when calculating power loss. The UPQC and UPQC<sub>DG</sub> combined power losses include:

- Power electronics conduction losses with diode energy dissipation.
- Semiconductor device and antiparallel rectifier switch losses.
- Forward voltage drops cause on-state power losses in switches.
- Elements of RC filters, power losses.

Apart from the losses in the switching sequence, all the power shortfalls are discovered through simulations. Using an analytical method, the volt/amp measured from the simulation is used to calculate SL. To obtain the full performance analysis, the simulated energy structure has been made quite feasible by using the real arithmetic quantities of forward voltage and forward rectifier voltage of the insulated-gate bipolar transistor from the information pane. The following represents the IGBT switching energy dissipation formula [14].

$$E_{Sc} = E_{ScRef} \times \left(\frac{I}{I_{Ref}}\right)^{Ki} \times \left(\frac{V_{cc}}{V_{ccRef}}\right)^{Kv} \times (1 - TC_{Sc}) \quad (6)$$

where  $Ki$  is the current dependent exponential  
 $Kv$  is the voltage-dependent exponential  
 $TC_{Sc}$  is the SL temperature coefficient

Nevertheless, the IGBT's switching energy ( $E_{Sc}$ ) is reliant on the dissipation of turn-on and turn-off energy ( $E_{Toff}$ ) is expressed as;

$$E_{Sc} = E_{Ton} + E_{Toff} \quad (7)$$

The turn-on energy dissipation expression can be stated as follows in accordance with the IEC 60747-9 standard:

$$E_{Ton} \int_{t_2}^{-t_1} P_v(t) dt = \int_{t_2}^{-t_1} V_{ce}(t) \times i_c dt \quad (8)$$

The integral lower and upper limits are set at 2% of  $V_{cc}(t_2)$  and 10% of  $V_{g(on)}(t_1)$  respectively. It is possible to define the formula for  $E_{Toff}$  as follows, with integral bounds of 90% of  $V_{g(on)}(t_3)$  and 2% of  $I_c(t_4)$ :

$$E_{Toff} = \int_{t_4}^{-t_3} P_v(t) dt = \int_{t_4}^{-t_3} V_{ce}(t) \times i_c dt \quad (9)$$

Table 1. Simulation Parameters

Supply Parameters	Voltage	415 V
	Frequency	50 Hz
	Impedance	$R_s = 0.05 \Omega$ $L_s = 0.6 mH$
DC Link Parameters	Capacitor	$C_{DC} = 5500 \mu F$
	Reference DC Voltage	700 V
Series APF Parameters	Inductance	1.22 mH/phase
	Resistance and Capacitance	$R = 300\Omega/phase, C = 75\mu F/phase$
	Injection Transformer	2 kVA
Photovoltaic array	Peak Power	15.3 kW
	Peak volt	547 V
	Peak amp	28.8 A

Table 1 depicts  $UPQC$  and  $UPQC_{DG}$  configurations. The heat/power losses for the 6-switching devices from the DVR and the distribution static compensator combined are indicated. When compared to DSTATCOM switches, it has been found that DVR inverter switches dissipate more energy. Similar to Table 1, Table 2 lists the losses as a result of the switching sequence in the BC of the  $UPQC_{DG}$ . Using Eq. (6), the SL is calculated from the dissipation of the energy rate of the switch.

## 4 Results and Discussion

### 4.1 Performance during Voltage Sag

The simulation parameters are shown above in Table 1. All the parameters kept the same for all the three scenarios. The  $UPQC_{DG}$  dynamic performance under voltage dip is displayed in Figure 5 (a). At time  $t=0.45s$ , a voltage dip occurred, and it is observed that DVR was injecting voltage to keep the load voltage level constant. Additionally, there is a noticeable rise in source current. Similar circumstances are observed in Figure 5 (b) for  $UPQC$ . The DC link voltage is kept constant by the PI controller to account for voltage dip. Active electricity from the PV array maintains the direct current link voltage. It was chosen because of stochastic nature of renewable energy source. The direct current link waveform does, however, experience a brief transient alteration at the dip time. But within 0.1s, the PI controller maintains the value at the desired level.

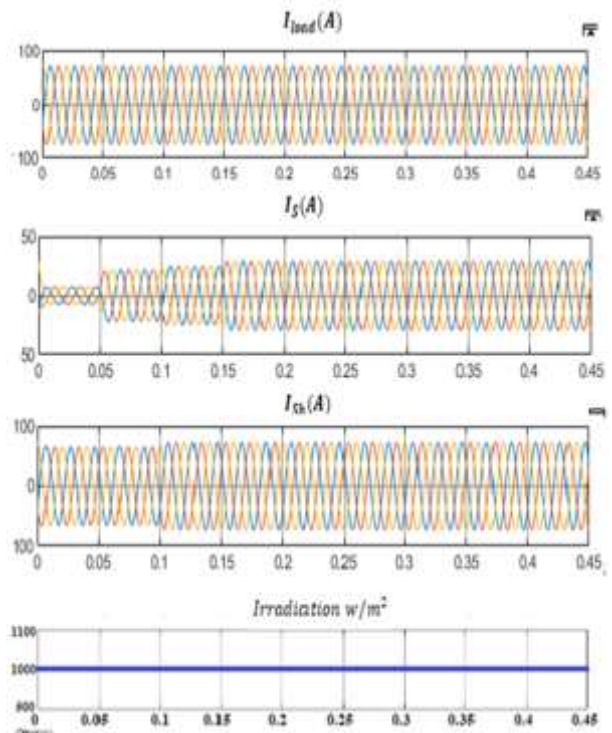


Fig. 5 (a): The currents and irradiation of  $UPQC_{DG}$  shunt inverter in 35% dip

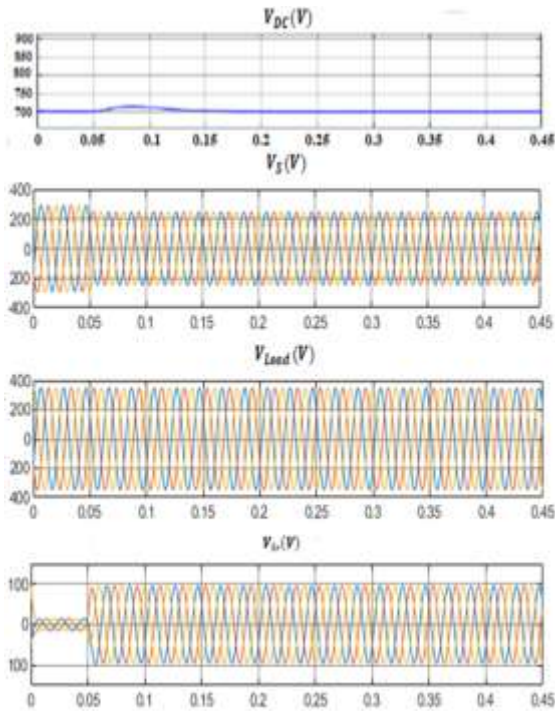


Fig. 5 (b): The voltages of  $UPQC_{DG}$  series inverter in 35% dip

At time  $t=0.45s$ , a voltage swell occurred between  $t=0$  to  $0.05s$ , and it is observed that DVR was injecting voltage to keep the load voltage level constant. Additionally, there is a noticeable rise in source current. Similar circumstances are observed in Figure 6 for  $UPQC$ . The DC link voltage is kept constant by the PI controller to account for voltage.

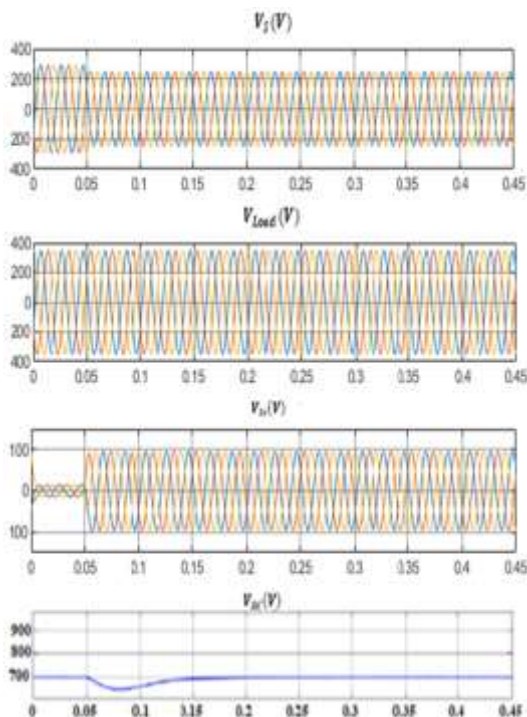


Fig. 6: UPQC representation 30% dip  $V_s(V)$

#### 4.2 The Effectiveness during a Voltage Surge

The  $UPQC_{DG}$  dynamic performance during a voltage surge is displayed in Figure 7. The signals generated are the DC link, the signal generated from the loads, the DVR signal, and the voltage dip. The load voltage is regulated at a constant magnitude while the voltage surge is reduced by DVR. The power loss due to voltage variation is 3.09% in  $UPQC_{DG}$  and 1.84% in UPQC. In comparison to the source depicted in Figure 8, the input current is smaller. In a situation of a voltage swell, DVR injects voltage that is out of phase with the provided voltage. In less than 0.05 seconds, the undershoot that occurred during the swell is likewise stabilized.

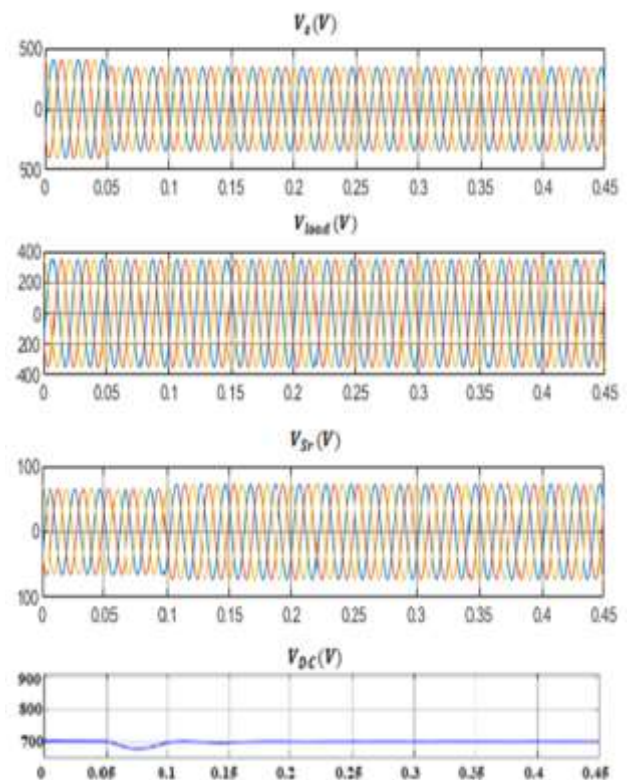


Fig. 7:  $UPQC_{DG}$  waveform during voltage surge (30%)

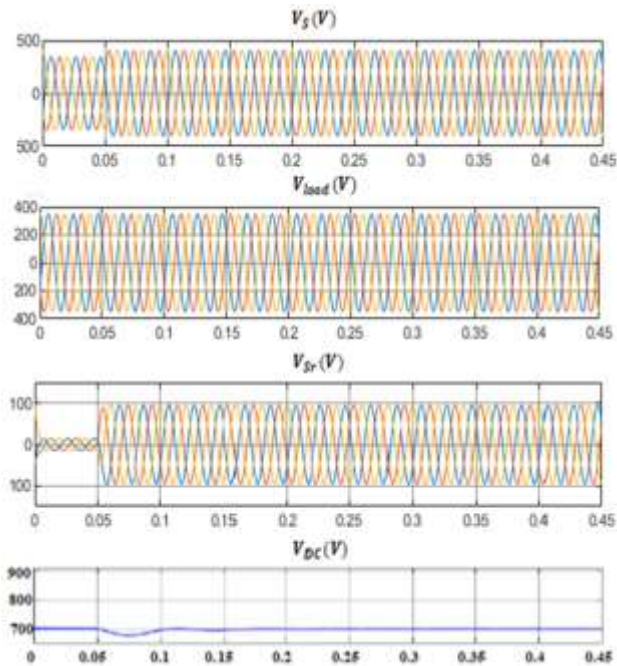


Fig. 8: UPQC representation in 35% dip

### 4.3 Performance during Varying Irradiation

Figure 9 depicts the appropriate behaviour of *UPQC DG* over the period of irradiation. PV was chosen because of stochastic nature of its source. The signals generated are the current flows in the load ( $I_{load}$ ), input current ( $I_s$ ), inrush current ( $I_{sh}$ ), solar insolation, direct current link voltage ( $V_{dc}$ ), input voltage ( $V_s$ ) and the voltage across the load ( $V_{load}$ ). The decline in PV power output is brought on by a shift in Photovoltaic irradiation from  $1000 \text{ W/m}^2$  to  $600 \text{ W/m}^2$ . When a load is applied, the source current's direction changes to the network. The magnitude of the direct current-link voltage and the voltage output are kept at the optimum consistency, while both *UPQC<sub>DG</sub>* and BC are operational, a loss of 1.43% is discovered.

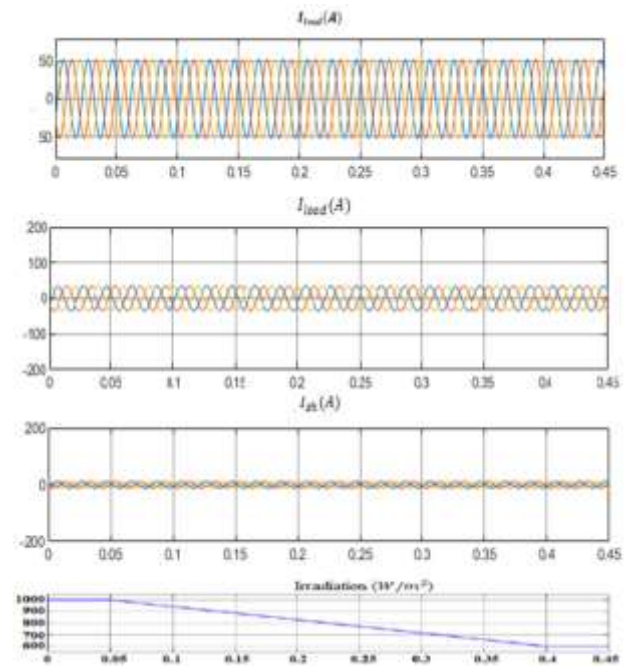


Fig. 9: UPQC-DG signal as PV irradiation changes (40%)

### 4.4 Comparison of Power Loss Analysis under Various Conditions

The data in Table 2 compares the power losses experienced by *UPQC<sub>DG</sub>* with regular UPQC. It consists of PV output power ( $P_{PV}$ ) of various conditions exposed to *UPQC<sub>DG</sub>* and UPQC, as well as input power ( $P_s$ ), load power ( $P_l$ ), total power losses ( $W$ ), and so forth.

- Every condition has a  $t = 0.05 \text{ s}$  simulation time. The system's performance in a steady state is assessed for 0.05 s in the first scenario. Under steady-state conditions, no electricity is absorbed or provided. Power from the PV system is seen to exceed load requests. In this situation, *UPQC<sub>DG</sub>* experiences a 3.04% power loss, while UPQC experiences a 2.13% loss.
- In the second scenario, both systems are subject to a 30% dip. The PV output power exceeds the load requirement, as indicated by the source power's negative sign, and power flows to the grid from the load. Related events occur under a variety of circumstances. The amounts of losses generated through the dip in case of *UPQC<sub>DG</sub>* activation is higher than the situations put on the system. In *UPQC<sub>DG</sub>* and UPQC, the voltage dip losses are respectively 3.4 and 2.51%. The shunt APF ameliorates for real/imaginary power as well as harmonic removal of load current under all these circumstances.
- The variance in PV array irradiation is introduced in Table 2 in the 5<sup>th</sup> row of *UPQC<sub>DG</sub>*

causing a fall in the output of the photovoltaic resulting in a reduction in the amount of current drawn by the network.

- In the table's final row, a conjunction of all circumstances is applied to both schemes. The network is simulated for 4 seconds. At 0.1 seconds, the system undergoes a voltage surge of 35%, while at 0.2 seconds, a voltage dip of about 35% occurred. At 2 seconds, the system experience stable equilibrium under full load. Between 2.7 and 3.7 s, a steady state with half of load 1 is added, followed by a stable condition with half of load 2 for 0.8 s. Additionally, the system is subjected to a 40% decline in irradiation for 0.4 s. When compared to traditional UPQC,  $UPQC_{DG}$  has greater overall losses.

Table 2.  $UPQC_{DG}$  and UPQC losses in Diverse Circumstances

Cases	Time (s)	Load Power (kW)	UPQC		$UPQC_{DG}$		
			Source Power (kW)	Losses (kW)	Source Power (kW)	PV Power (kW)	Losses (kW)
$SS_{FL}$	0.45	32.56	32.091	595.30	10.500	44.162	97.82
$SS_{FL} Dip @30\%$	0.45	31.90	32.703	803.01	11.819	45.061	1076.10
$SS_{FL} Swell @30\%$	0.45	33.21	33.603	611.40	10.929	45.097	1009.67
Overall (Dip/Swell)	0.45	29.13	27.490	590.10	14.467	44.274	780.09

Table 3. Comparison of percentage power loss analysis with previous works.

	PV input kW	UPQC	$UPQC_{DG}$	% Loss Reduction	% Loss/PV Integration ( $kW^{-1}$ )
E. Ozdemir (2011)	-	987.10	-	-	-
V. Khadkikar (2011)	30	802.10	499.72	3.90%	0.130
Sisir Kumar (2022)	36	778.09	522.03	3.03%	0.084
P. Shah (2022)	37	790.09	760.70	2.99%	0.081
Current Work	45.09	590.10	780.09	2.13%	0.047

#### 4.5 Comparison of Power Loss Analysis with Previous Work

The previous research done on the effectiveness of different operating conditions of UPQC with respect to their power loss compared with the current approach indicated that under PAC control of UPQC both inverters are put into optimum use. Also, the PAC control algorithm was able to effectively ameliorate the current and voltage along with the integration of solar PV better than existing

approach used. Table 3 below shows the summary of this comparison. Table 3 shows the past works and losses percentage reduction and there is a clear indication that previous work losses reduction is not as good as what is obtainable this work. It can also be seen from Table 3 that the loss percentage/ PV integration is at its lowest in this study compared to previous work. The overall power loss for  $UPQC_{DG}$  is 2.68%, whereas it is 2.12% for UPQC.



## 5 Conclusion

This study examines the level of power loss in several UPQC configurations, referred to as PAC of UPQC, and a version integrated with distributed generation energy sources, in which both the parallel and series active power filters portion of the load imaginary energy requirement. The investigation is proven by carrying out a rigorous simulation on MATLAB/SIMULINK. With the incorporation of solar PV, the algorithms used were able to enhance the voltage and current parameters. In the instance of  $UPQC_{DG}$ , the combined losses of the parallel/series inverter and direct current to direct current BC exceed the losses of the UPQC in the case of  $UPQC_{DG}$ .

Overall power loss for  $UPQC_{DG}$  is 2.68%, whereas it is 2.12% for UPQC. Losses are seen to be higher in  $UPQC_{DG}$  due to the use of two inverters and one converter. Regardless of the outcome, the study also assesses the benefit of  $UPQC_{DG}$ . It boosts the grid electricity supply, usage of renewable, clean energy, and removes harmonics. Experimental validation of the work shall be carried out in future work.

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### Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.

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