A Low Impedance Current-Reuse Path for UWB-PA to Improve Efficiency and Gain

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Abstract: - Current-reuse circuit with a low impedance current-reuse path has been proposed to enrich high flat gain, high efficiency, and high output power across the operating band. While an inductor-capacitor (LC) interstage is employed to improve the linearity of the proposed PA. In the second stage, the shunt peaking design in a common-source circuit is employed to improve the power gain, while a network of reactance compensation is adopted at the output of the second stage to overcome the parasitic capacitance's impact on the active device. The post-layout simulation using the TSMC 65 nm CMOS process is carried out on the entire frequency range from 3.1 GHz to 10.6 GHz. The post-layout simulation achieved ±42 ps group delay variation, 32% power-added efficiency (PAE), and 32-dB power gain. Matching input and output of less than −10 dB has been achieved over the operating band, and it achieved an output power of 18.3 dBm.

Key-Words: - class-E, power amplifier, ultra-wideband, current-reuse, reactance compensation.

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1 Introduction

Ultra-wideband (UWB) technology has received significant attention in the scholarly community and has become a hot topic in industrial applications, [1]. UWB brings wireless communication, Wireless communications mobility, and comfort to high-speed interconnects in devices used in the digital office and home environments. Power amplifiers (PAs) in mobile devices consume the highest amount of power in the transmitter, so the PA for UWB should have the following characteristics: high efficiency, good linearity, high flat gain, and a small area, [2], [3]. Many topologies, such as the resistive shunt feedback, have been used to obtain flat Gain, [4]. With these technologies, wideband input matching and flat Gain have been realized. However, the Gain of the circuit in the feedback direction has reduced. Two resonance networks with active RC feedback are adopted, [5], to realize linearity enhancement, good broadband matching, bandwidth extension, and flat gain. The maximum Gain and high efficiency will be achieved by common source inductive degeneration, as in, [6], but it requires a large area, and the increased match was not as effective as it might have been. Three-stage amplifiers have been revealed by the stagger-tuning design, [7], where each stage was tuned to a particular frequency enabling broadband operation and flattening Gain. However, this resulted in excessive power consumption. The distributed amplifier in [8] realized high gain and wideband operations. However, it consumed a significant amount of power and required a large area depending on the placement of many amplifying stages and the transmission lines linking them. A common source power amplifier was designed to achieve good linearity and high gain, but the design resulted in poor power-added efficiency (PAE), [9]. The two-stage cascade common source power amplifier proposed in [10] provided high gain and good linearity, but the circuit achieved a low PAE. The UWB–PA design uses a current-reuse topology to achieve low power consumption, [11]. This design provides better isolation, reduces group delay (GD), and improves gain flatness, but it also introduces poor matching and low power gain. In this work, a PA with a low impedance current-reuse path is designed to achieve a high flat Gain over the operating band and to meet all ultra-wideband requirements. Furthermore, it used the reactance compensation technique to compensate for reduction in efficiency caused by the parasitic capacitance of the active devices, which appeared at high frequencies. The simulation results showed that our design achieved high PAE, low GD variation, good input and output matching, and high output power. The proposed UWB power amplifier design is discussed in Section 2 in terms of its principles

and analysis. The simulation results and a table of recent publication PAs have presented in Section 3. Finally, The conclusion of the paper is presented in Section 4.

2 Circuit Design

The proposed circuit consists of two stages. The first stage is the current-reuse circuit with a low impedance current-reuse path, as shown in Fig. 1. The inductor L_3 has a high impedance, which prevents the output signal of transistor M_1 from passing to the source of transistor M_2 and passing to M_2's gate through the C_2 path, which has a low impedance as this path consists of only one capacitor instead of using a capacitor and an inductor in previous researches. Using only one capacitor in the current-reuse path reduces the impedance of the current-reuse path, which increases the gain, improves the efficiency, reduces the size of the design, and increases the output power. At the same time, the capacitor C_2 is used to resonate with the gate-to-source parasitic capacitance of the transistor M_2.

Shunt RC feedback is employed to produce a good flat gain, a broadband input match, and a low noise figure (NF) at the same time. The operating bandwidth is increased but the gain is decreased when the feedback resistor (R_f) is set to a low value. To meet the matching and gain demands, the value of the R_f should be carefully chosen. Capacitor C_1 and inductor L_1 were used to enhance wideband input matching. The circuit of the current mirror formed by R_{b1}, R_{b2}, and M_{b2} is employed to bias transistors M_2. As shown in Fig. 2, the output voltage of the current-reuse stage can be expressed as the following:

$$V_{out2} = g_{m2} V_{gs2} (SL_4 /\!/ r_{o2}) \quad (1)$$

$$V_{gs2} + V_{C_2} - V_{L_3} = 0 \quad (2)$$

$$V_{gs2} = V_{L_3} - V_{C_2} \quad (3)$$

$$V_{out2} = g_{m2} (V_{L_3} - V_{C_2}) (SL_4 /\!/ r_{o2}) \quad (4)$$

Where g_m, V_{gs}, A_v, and r_o represent the trans-conductance, gate-source voltage, voltage gain, and output resistance of the transistor respectively.

From Equations (4), we can deduce that reducing the impedance of the current-reuse path using capacitor C_2 only reduces the voltage drop in the current-reuse path, which increases the output voltage of the transistor M_2 , increasing the total gain without increasing the power consumption.

Figures 3, 4, and 5 show the impact of lowering the current-reuse path on gain, PAE, and output power respectively, indicating that lowering the impedance of the current-reuse path improved the performance of the designed UWB–PA.

To obtain a wideband operation, the stagger tuning technique is used, as shown in Fig. 6. In this technique, the current-reuse stage is tuned to resonate at 6.2 GHz, which is the high frequency of the desired band, and the class-E (the main stage) is tuned to resonate at 4.6 GHz, which is the low frequency of the desired band, [12].

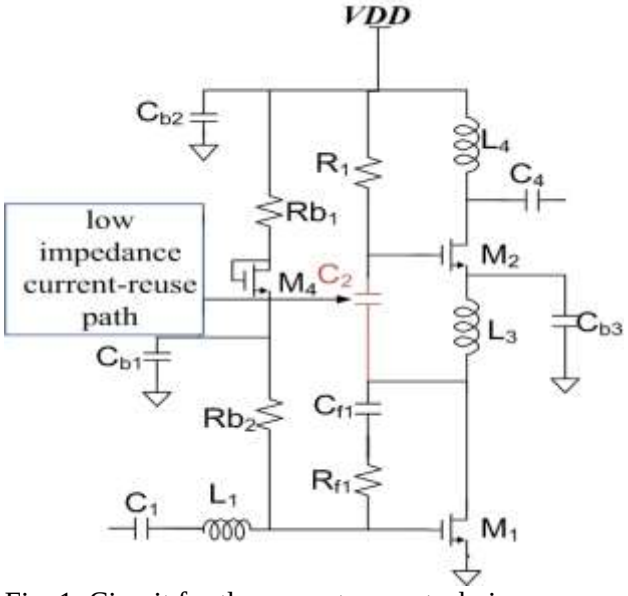

Fig. 1: Circuit for the current-reuse technique.

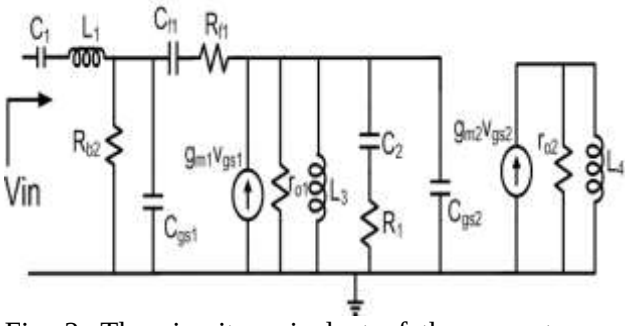

Fig. 2: The circuit equivalent of the current-reuse circuit.

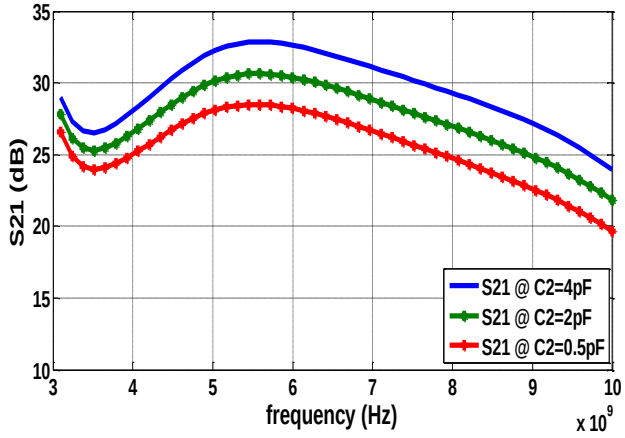

Fig. 3: The impact of lowering the current-reuse path on gain.

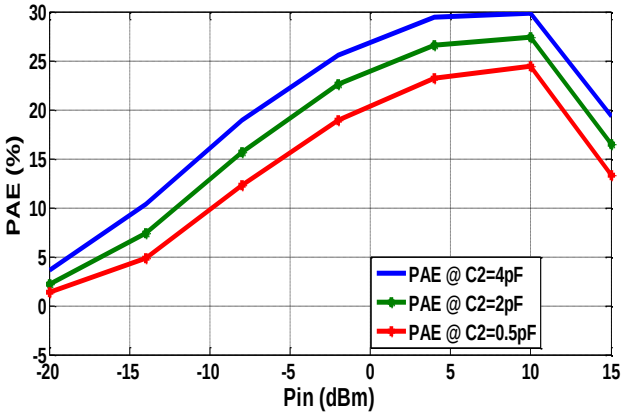

Fig. 4: The impact of lowering the current-reuse path on PAE.

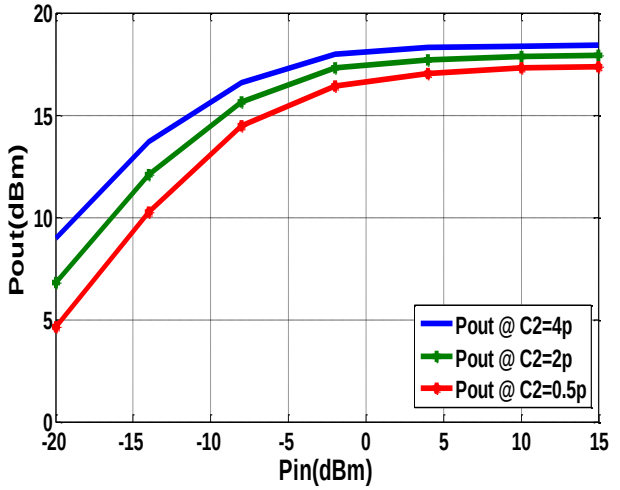

Fig. 5: The impact of lowering the current-reuse path on output power.

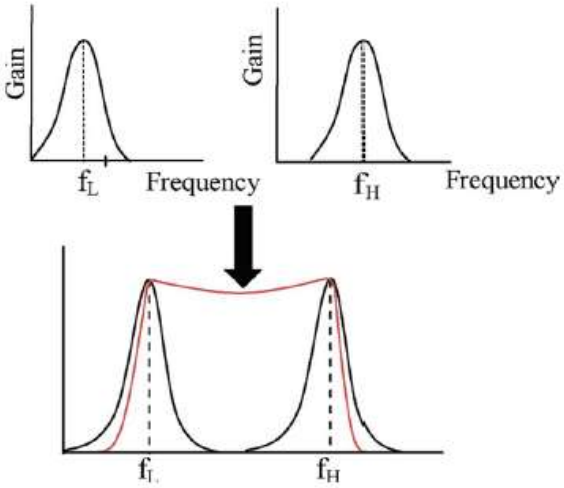

Fig. 6: Technique of stagger tuning.

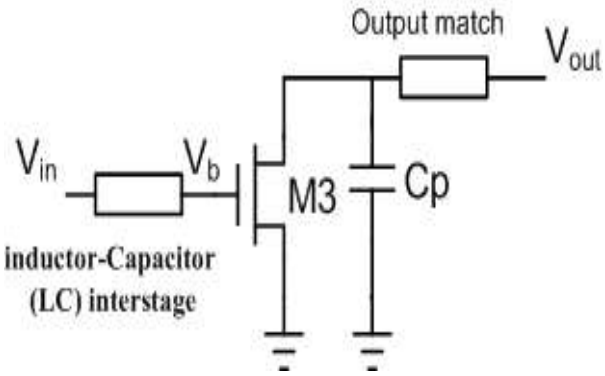

Fig. 7: Inductor-Capacitor (LC) interstage on the PA.

One drawback of the class-E PA is its low linearity. Nonlinearity is characterized as the presence of higher-order harmonics; the inductor-capacitor (LC) interstage produces an anti-phase between the input and the output signals, canceling out the undesired signals produced by the PA. From Fig. 7, the PA's input and output voltages can be given as follows, [13].

$$v_{out} = a_0 + a_1 v_b + a_2 v_b^2 + a_3 v_b^3 \quad (5)$$

$$v_b = b_0 + b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3. \quad (6)$$

While $a_{1,2,3}$ and $b_{1,2,3}$ are the coefficients for the fundamental, second, and third harmonics of the voltage V_b and V_{in} respectively. a_0 and b_0 are the D.C components, also V_{out} is the output voltage while V_b is the gate voltage. By substituting Equation (6) into Equation (5) and considering the third-order components and fundamentals as follows:

$$V_{out} = a_1(b_1 v_{in} + b_3 v_{in}^3) + a_3(b_1 v_{in} + b_3 v_{in}^3)^3 = a_1 b_1 v_{in} + (a_1 b_3 + a_3 b_1^2) v_{in}^3 + 3a_3 b_1^2 + 3a_3 b_3^2 b_1 v_{in}^7 + a_3 b_3^3 \quad (7)$$

By eliminating the part of the third order components which is:

$$a_1 b_3 + a_3 b_1^3 = 0 \quad (8)$$

$$b_3 = -\frac{a_3 b_1^3}{a_1} \quad (9)$$

Substituting the fundamental amplitudes of a_1 and b_1 to be unity, will give the following Equation:

$$b_3 = -a_3 \quad (10)$$

The PA's third intermodulation distortion (IMD3) is canceled by Equation (10). Thus, for Equation (10) to be satisfied, we used the proposed interstage circuit that is formed by inductor L_6 and capacitor C_6 between the current-reuse stage and the class-E (main stage). Therefore, the linearity of the circuit is improved. Fig. 8 shows the effect of LC interstage on the GD variations. The values of L_6 and C_6 are adjusted several times simultaneously to improve the GD variations. L_6, and C_6 values are enhanced and proposed to be L_6 = 1.8nH and C_6 = 1pF.

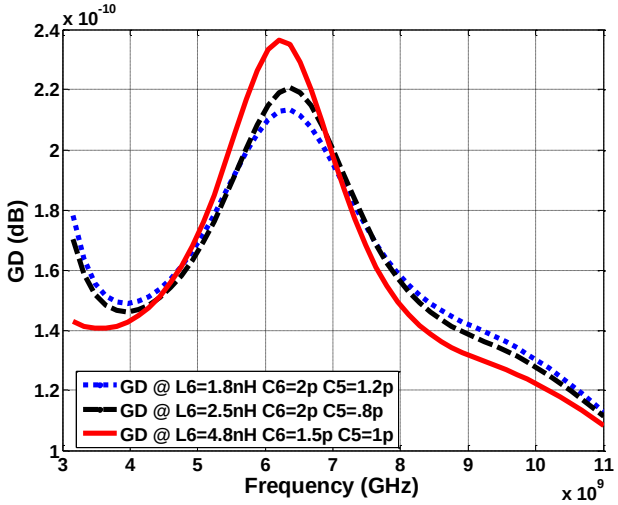

Fig. 8: Effect of L6, and C6 on group delay variation.

The second stage of the proposed circuit is the class-E PA, which is used as the main stage, as shown in Fig. 9, class-E PA is used because it is the most appropriate for RF applications, [14], [15]. It has a simple load network, and a satisfying output even with a non-optimal drive. In addition to the potential for high-efficiency operations, it has high efficiencies at RF, [16], [17]. However, the current-reuse circuit and the class-E structure suffer from the parasitic capacitances of their active devices. The effect of these parasitic capacitances increases at high frequencies, reducing PA gain, efficiency, and operating band performance. To improve the efficiency and increase the operating band of the proposed UWB–PA, a reactance compensation network was employed, [18]. The reactance compensation network consists of the series L_s, C_s, and the shunt L_p, C_p as shown in Fig. 10. The parallel capacitance C_p was used to account for the parasitic capacitances C_{gd} and C_{ds} of the transistor M_3. The peaking properties of L_p allow it to extend the bandwidth and lower the output return loss. Increasing the value of L_p improves the GD performance but reduces the PAE. In contrast, increasing the value of C_s increases the PAE and the output matching but reduces the performance of the GD. From the previous explanation, we can conclude that L_p, C_p, and L_s have a large influence on the GD performance, output matching, PAE, and gain. The values of L_p, C_p, and L_s are tuned several times at the same time to increase PAE, reduce GD variations, and achieve a wide flattened gain as shown in Figures 11, 12, and 13. The values of L_p, C_p, and L_s are enhanced and designated to 364 pH, 1.2 pF, and 544 pH, respectively. The Equations for the LC resonators are as follows, [19]:

$$L_p = 0.73\left({}^{R_L}/_{\omega_0}\right) \quad (11)$$

$$C_o + C_p = {}^{0.69}/_{\omega_o R_L} \quad (12)$$

$$L_s = 1.03\left({}^{R_L}/_{\omega_0}\right) \quad (13)$$

$$C_s = 1/\omega_0^2 L_s \quad (14)$$

Where ω_0 represents the resonant angular frequency, and C_0 represents the output capacitance of the transistor.

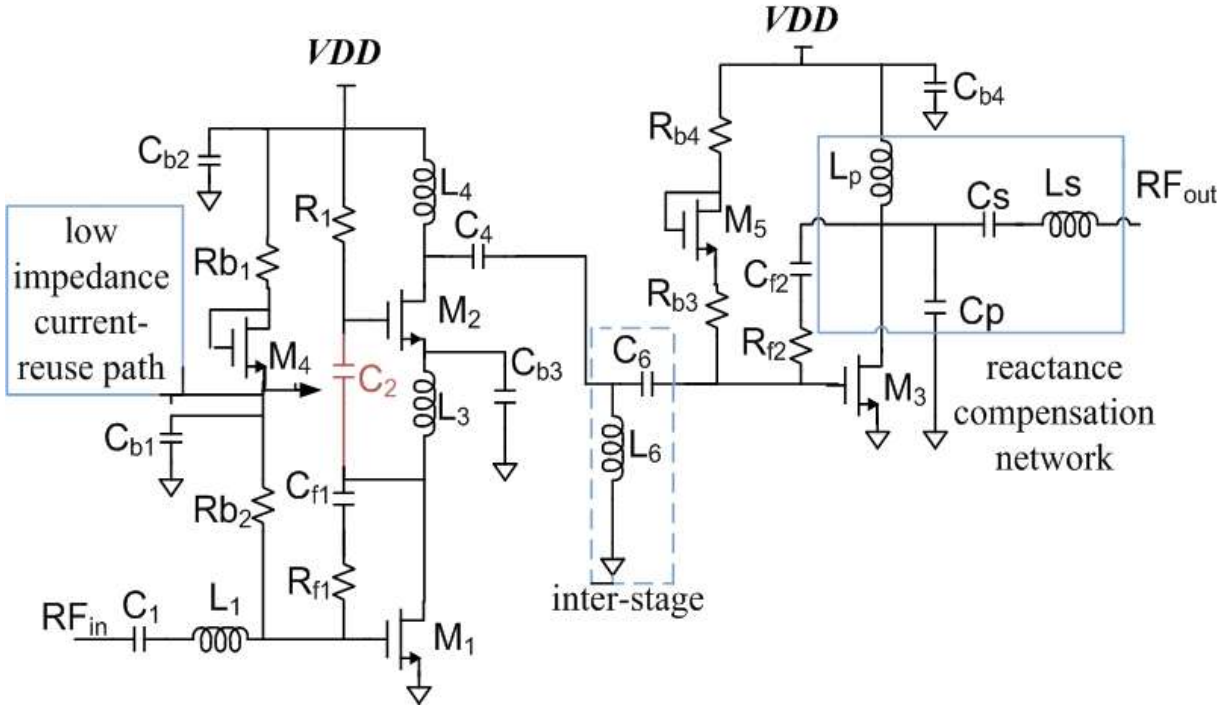

Fig. 9: The proposed UWB- PA.

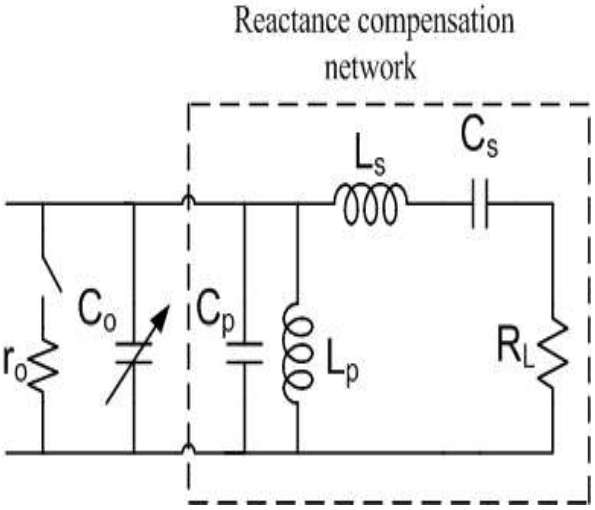

Fig. 10: The circuit of reactance compensation.

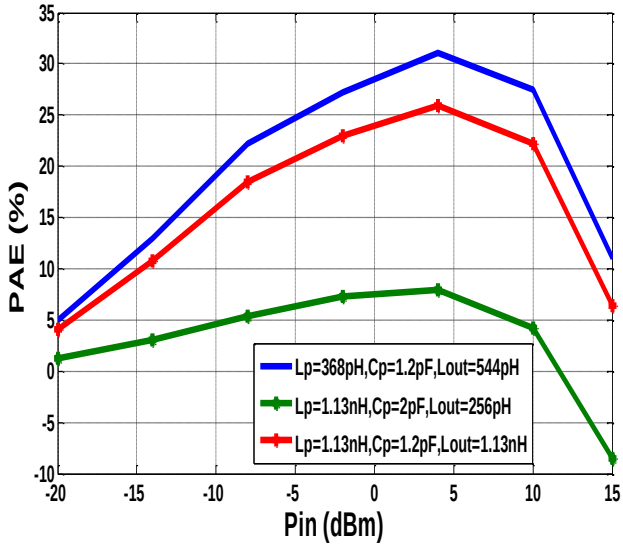

Fig. 11: Effect of L_p, C_p and L_s on PAE.

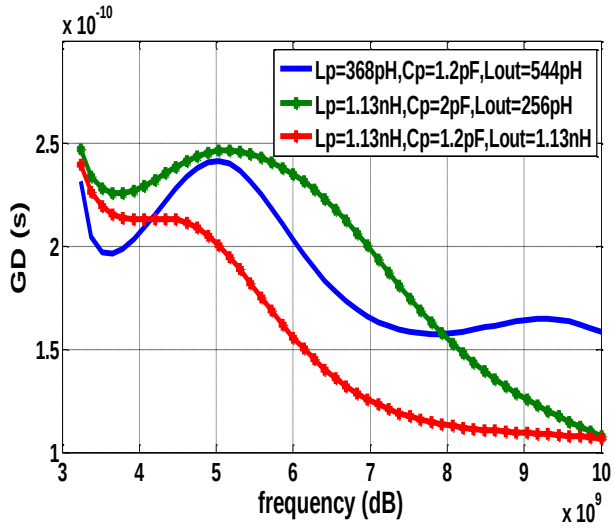

Fig. 12: Effect of L_p, C_p and L_s on GD.

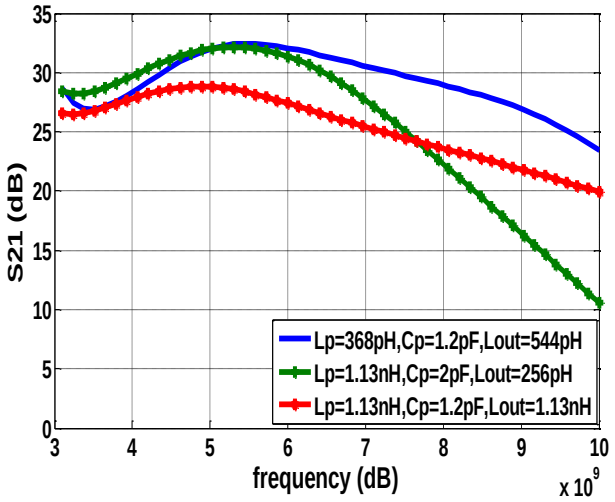

Fig. 13: Effect of L_p, C_p and L_s on S21

3 The Simulation and Discussions

To simulate the proposed circuit using (TSMC 65nm) technology, we used the Cadence Spectre simulator. The PAE is a critical parameter for assessing the performance of the PA; thus, it is enhanced using a low-impedance current-reuse path and a reactance compensation network. Fig. 14 shows the simulation of the PAE as a function of input power at different frequencies of the proposed band, achieving maximum PAEs of 32%, 29%, and 24.6% at 8, 10, and 6 GHz, respectively. The PAE as a function of frequency is plotted in Fig. 15 across the band from 3 to 11 GHz. The PAE is maximum at 8GHz and has good results for the range from 6 GHz to 10 GHz.

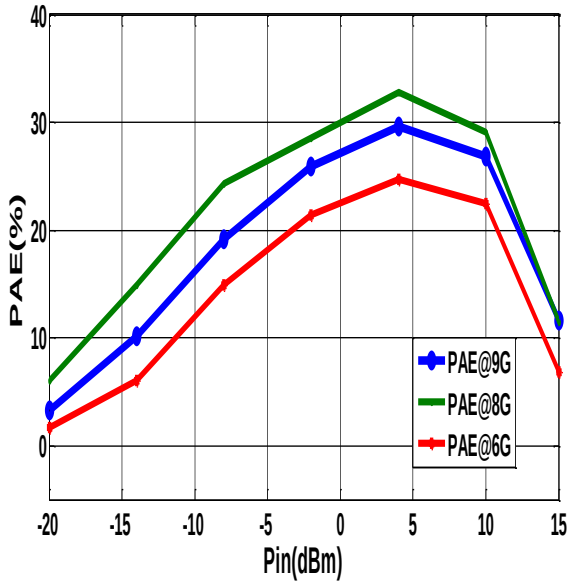

Fig. 14: Power-added efficiency at different frequencies.

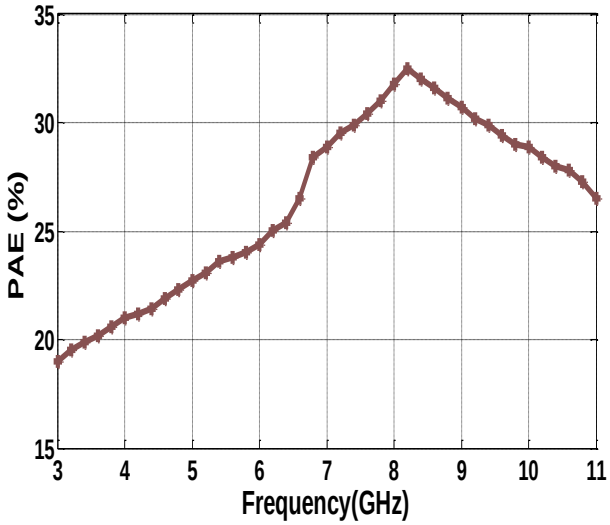

Fig. 15: Simulation of PAE as a function of frequency.

Fig. 16 shows the ratio of output power to input power. It can be seen in the figure that the circuit achieved a maximum output power of 18.3, 17.9, and 16.6 dBm at 8, 10, and 6 GHz, respectively. Also, the output power as a function of frequency is plotted in Fig. 17 across the band from 3 to 11 GHz. The output power is maximum at 8 GHz.

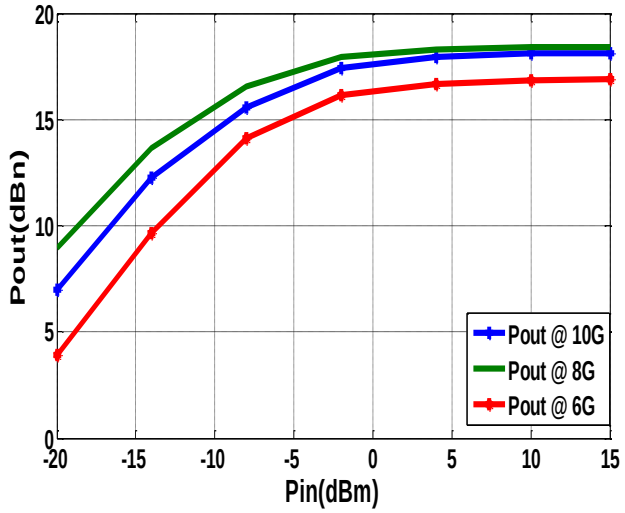

Fig. 16: Output power at different frequencies.

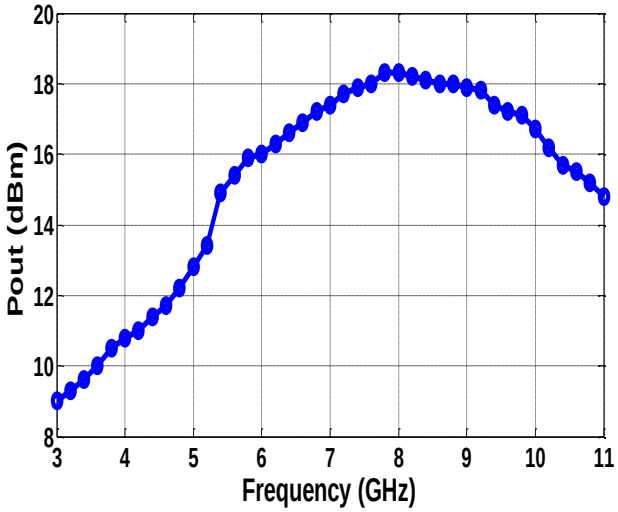

Fig. 17: Simulation of output power as a function of frequency.

GD has a substantial effect on the design performance because it is a significant measure of signal distortion in the time domain. The time domain signal distortion occurs when the GD varies with frequency; nonetheless, keeping the GD unchanged and stable in all operating bands is ideal. Minimizing frequency domain changes protects the time domain-amplified signal from distortion. Furthermore, high GD variations indicate more phase distortion, and the output does not retain its original input. Small GD variations of ±42 ps are attained over the operating band, as shown in Fig. 18.

Fig. 19 shows the S-parameters simulation of the proposed UWB–PA, where the average S21 is 30 dB, and S12 is less than −60 dB. The proposed circuit achieved good input (S11) and output (S22) matching over the 3.1 to 10.6 GHz band. The designed circuit stability is determined using the Kf and B1f tests, as shown in Fig. 20. Kf is greater than one, and B1f is less than one over the full desired band, indicating that the designed PA is permanently stable. Fig. 21 shows the layout of the proposed PA, which covers a chip area of 1280 x 1010 um.

Table 1 shows a comparison between the designed circuit and the previously published work. Clearly, the circuit improved all ultra-wideband requirements significantly in the frequency operating band.

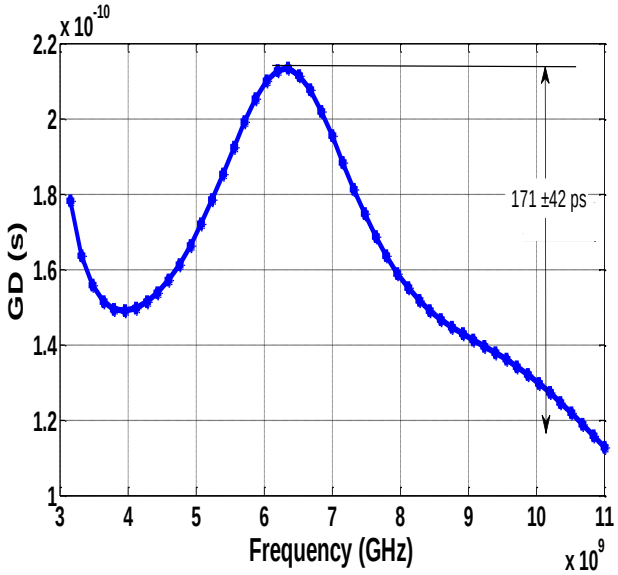

Fig. 18: Post-layout simulation of group delay.

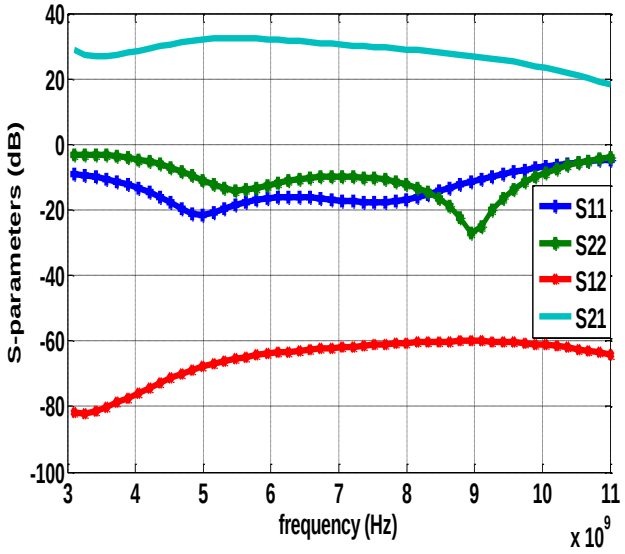

Fig. 19: Post Layout simulation of S-parameters.

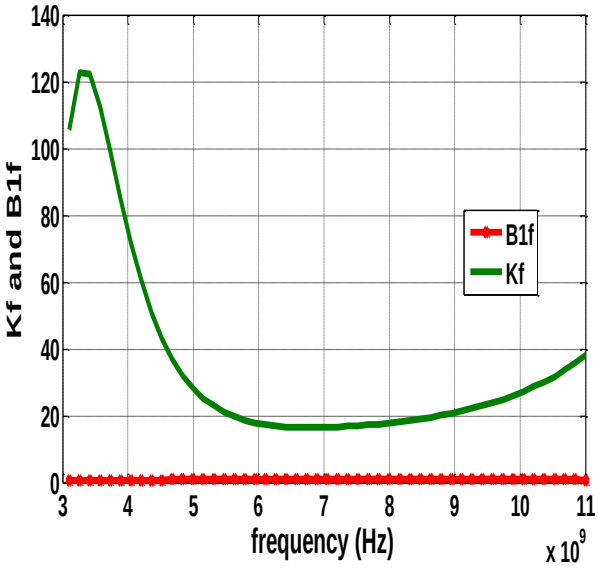

Fig. 20: Simulation of K f and (B1 f).

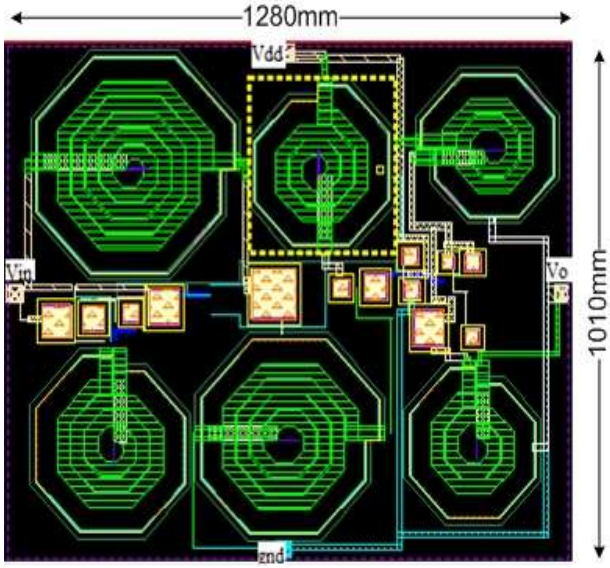

Fig. 21: The proposed PA's layout.

Table 1. Comparison of the designed techniques to previous research

Ref.	Tech.[nm]	Freq. GHz	GD	Max. output dBm	Gain dB	S11dB	S22 dB	Max. PAE%
[20]*	180	3 -5	±75	13	16.2	<-6	<-0.5	47
[21]**	65	3-10	±21.5	16	12.65	<-10	<-10	20.15
[22]**	130	7.8-11.5	N/A	12	8	<-9	<-5	20
[23]*	180	3.1-10.6	±50	11	12.5	<-4.5	<-8.5	32.5
[24]*	180	3.1-10.6	N/A	4	15	<-6	<-7	22
[25]*	130	8-12	N/A	13	10	<-8	<-7	27
[26]*	180	3-10.6	±68	9	11.5	<-8	<-8	26
This work*	65	3.1-10.6	±42	18.3	32	<-8	<-11	32

*Simulation results
** Measurements

4 Conclusion

In this paper, UWB class-E PA in which a current-reuse circuit with a low impedance current-reuse path is proposed to enrich high flat gain, high efficiency, and high output power across the operating band without increasing the power consumption. An LC interstage was used to increase the linearity of the proposed PA. A reactance compensation network was employed to overcome the influence of the parasitic capacitance of the active device. Post-layout simulation of the proposed circuit was designed using a TSMC 65-nm CMOS process with a 1.2 V supply voltage. Using the proposed circuit, the full bandwidth of UWB from 3.1 to 10.6 GHz was covered, and 18.3-dBm output power at 8 GHz, 32% maximum PAE at 8 GHz, a small GD variation of ±42, and 32-dB power gain was achieved. For the covered frequency range, our model realized good power gain and PAE. Moreover, our proposed model achieved the best performance compared with state-of-the-art technologies. The proposed power amplifier is aimed to satisfy the requirements of 5G NR at 3.5GHz in terms of linearity, power-adding

efficiency, and output power. Also, it aimed to satisfy the requirements of imaging systems that go through the wall. The circuit has some limitations such as the number of inductors which increases the size of the circuit, in future work we will try to reduce the number of inductors at the same time achieve good performance.

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There is no conflict of interest.

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