Design of a Low-Power Low-Noise ECG Amplifier for Smart Wearable Devices Using 180nm CMOS Technology

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Abstract: - Wearable biomedical devices for recording electrocardiograms (ECG) are becoming more and more popular as they provide clinicians with a comprehensive view of a patient's diagnosis. ECG signals are characterized by low amplitude and are susceptible to many kinds of noise, so high gain and high common mode rejection ratio (CMRR) are essential to suppress them, while ultra-low power low noise (AFE) is used for Analog front-end for ECG signal acquisition, based on a Drive Right Leg (DRL) circuit that combines common-mode feedback with high CMRR and a notch filter band with a cutoff frequency of 50, implemented in CMOS 180 nm technology. According to the simulation results, this front-end circuit can yield a mid-band gain of 50.75 dB at -3dB bandwidth from 100mHz to 100 Hz, a Power Supply Rejection Ratio (PSRR) of 113 dB, and a Common Mode Rejection Ratio (CMRR) of 102 dB, exhibit an input-referred noise (IRN) of 1.47 µVrms from 0.1 Hz to 1kHz, corresponding to a noise efficiency factor (NEF) of 2.74. The AFE consumes 1.08 µW from the 1.8V supply voltage.

Key-Words: - ECG, CMOS Amplifier, CMRR, IRN, DRL Circuit, Low-power, Low-noise, NEF, Power Line Interference.

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1 Introduction

The artificial intelligence health care technologies have concentrated on smart wearable devices in recent years because they are commonly utilized to monitor an individual's heart status for early diagnosis of cardio-vascular disorders including cardiac arrhythmia and heart failure. In an ECG sensor, the recording amplifier is one of the most significant components in terms of power, noise, and linearity performance [1].The electrocardiogram (ECG) signal is critical in the monitoring and diagnosis of heart health problems. The electrical activity of the heart is interpreted by an electrocardiogram (ECG). Results of the ECG are characteristic signals composed of components such as the P-wave, QRS complex and T-wave. The atrial depolarization is represented by the P-wave, the ventricular depolarization is modeled by the QRS complex, and the ventricular repolarization is reflected by the T-wave [2]. A typical ECG signal of a healthy person is illustrated in Fig. 1.

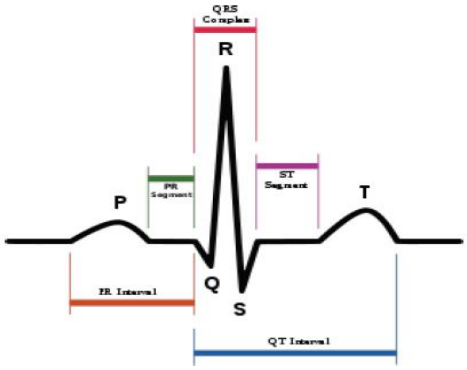


Fig. 1: ECG of a heart in normal mode.

The ECG equipment uses two electrodes on the patient's chest to record the heart electrical activity and connected to the differential input nodes of the proposed amplifier while the third electrode is connected at the right leg of the subject. An AFE amplifier that amplifies the ECG signal, filters it, and converts it to digital data for analysis, and a display monitor to keep track of the patient's heart on a frequent basis [3]. The block diagram of a typical ECG monitoring system design is shown in Fig. 2.

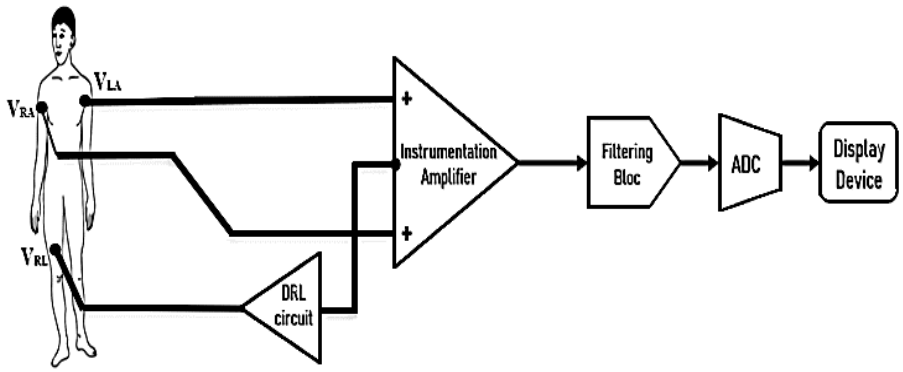


Fig. 2: Block diagram of ECG monitoring system.

The ECG signal has a very weak amplitude and low frequency in the range of 100μV to 8mV and ≤1kHz [4], so The AEF amplifier is required to increase this weak signal into a desirable voltage level. At low frequencies, as the heart signal is ranging from 0.1Hz to 100Hz, thermal noise and flicker noise, collectively known as input-referred noise, noise will affect the real biomedical signal [1]. Flicker noise predominates in biomedical signals due to their low frequency, and it has a considerable impact on the WL product of a CMOS transistor [5]. To reduce the 1/f noise, it is advisable to model the input-referred noise and the power spectral density (PSD) of the drain current 1/f noise in saturation as well as in subthreshold [6]. To improve noise-power efficiency, the suggested preamplifier employs a current-reused OTA with an inverter-based differential input stage for low noise and a class-AB output stage for wider output range and high gm/I efficiency [7].

Electrode contact noise is caused by either a loss of contact between the electrode and the skin or the electrode's movement away from the contact area on the skin; contrarily, the artifact noise results from the electrical activity of the driver's muscle contractions [8]. That well being led to unstable input offsets causing the amplifier to be saturated. Baseline wander, powerline interference, EMG noise, and electrode motion artifacts are the most common types of artifacts in ECG signals. These noises and offset influence the preciseness of the wearable monitoring system [9].

Study of the Recent research activities reveals the significance preamplifier design improving OTA performance in power, noise and linearity for ECG recording applications. The design of [10] has adopted a degeneration technique in a double recycle folded cascode operational transconductance amplifier architecture to achieve higher transconductance for more energy efficient low noise. With a low-power, low-noise capacitive feedback amplifier based on the current OTA topology used for ECG recordings, the design of [7] achieves an excellent power noise figure that uses differential pairs based on an inverter in the first stage to reduce noise efficiency, and class AB output stage to improve *gm/I* efficiency to further reduce power consumption. Another method to improve low frequency noise performance has been used in [11], it uses a chopper stabilization technique as an AC coupled chopper stabilized amplifier to reduce 1/f noise and a tunable MOS capacitor and a tunable pseudo-resistor to control the bandwidth.

In this paper, AFE for the ECG system is designed and simulated by using a 180nm CMOS technology with a power supply of 1.8V. The signal is sent from two sensing electrodes on opposing sides of the chest to a difference amplifier, where it is combined with PLI. A driven-right-leg circuit (DRL) offers negative feedback via a third electrode placed on the right leg to counteract the influence of common-mode interference.

The remainder of this work is organized as follows. Section 2 gives an overview of the proposed ECG acquisition System design as well as the schematics of the building blocks. Simulation results and comparisons are presented in section 3. Finally, Section 4 describes the conclusion and future work.

2 Problem Formulation

2.1 Instrumentation Amplifier

IA is used to extract the heart's ECG signal from a subject, amplify it, and produce larger differential gain by removing noise. This study outlines a new method for creating a low-noise, high-gain CMOS instrumentation amplifier for ECG monitoring. This technique is used to introduce the capacitor network to perform better in the OTA [7]. The capacitive

feedback amplifier utilizes capacitors to set the mid-band gain to reject DC offset from the skin-electrode and to set up the cut-off frequency with pseudo-resistor [12]. The schematic design of the proposed AFE is shown in Fig. 3.

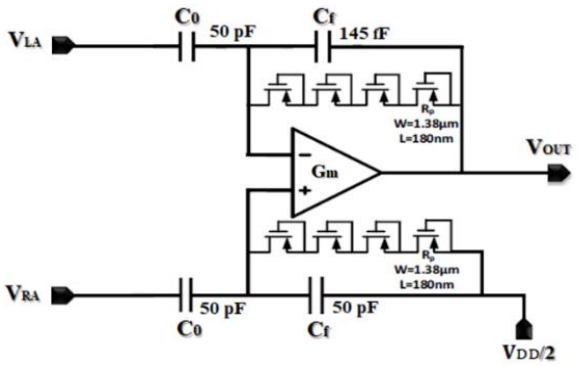


Fig. 3: Schematic design of proposed AFE

Our AEF uses an OTA amplifier and capacitive feedback in parallel with resistive feedback to produce low-noise operation and to reject high dc offsets at electrode-tissue interfaces. The resistor in the feedback circuit is implemented using MOS-BJT transistors and is referred to as a pseudo-resistor which occupy a small area whose value is in the order of Tera ohms ($10^{12}\Omega$) [7]. The mid-band gain of the amplifier, G_m, is set by the ratio between the input capacitor C_0 and the feedback capacitor Cf [10]. Without considering electrode-tissue interface, the gain of the preamplifier employing capacitive feedback network and the Miller compensation is expressed as

$$Av(s) \approx \frac{-C_0}{Cf}\left[\frac{1 - s\frac{Cf}{g_{m,st2}}}{\left(1+\frac{1}{s.Rf.Cf}\right)\left(1+s\frac{Cc.C_0}{Cf.g_{m,st1}}\right)}\right] \quad (1)$$

Assuming that g_m finite and ignoring Rf, we can express the transfer function as

$$Av(s) \approx \frac{-C_0}{Cf}\left[\frac{1 - s\frac{Cf}{g_{m,st2}}}{\left(1+s\frac{(Cf.C_0+Cf.Cc+Cc.C_0)}{Cf.g_{m,st1}}\right)}\right] \quad (2)$$

For large g_m, we obtained the transfer function as

$$Av(s) \approx \frac{-C_0}{C_f} \quad (3)$$

To not affect the mid-band gain of the amplifier, the pseudo-resistor Rf must be large. The lower cutoff frequency, fL, depends on the feedback capacitance Cf and the pseudo- resistor Rf. Whereas the higher cutoff frequency, fH, depends on the transconductance of the first stage $g_{m,st1}$ and the Miller compensation capacitor Cc and be expressed as

$$f_L = \frac{1}{2\pi.R_f.C_f} \quad (4)$$

$$f_H = \frac{g_{m,st1}}{2\pi.A.Cc} \quad (5)$$

The combination of Cf and the MOS pseudo-resistor Rf has created a high pass filter with a cutoff frequency at a few hundred Hz introduces low-frequency noise due to the noise currents at the gates of the input transistors. The filter pole formed by Cf and the pseudo-resistor Rf is at a very low frequency Because the Rf has a significantly larger impedance than a weak-inversion MOS transistor [13]. The input-referred noise is one of the most important specifications for ECG recording amplifiers. $C_{p,in}$ is used to define parasitic gate capacitances at the gain-stage OTA input terminals. The input referred-noise of the OTA is modeled as a $V_{n,OTA}$. As reported in [14], The relationship between the input-referred noise density of the overall capacitor feedback amplifier, $V_{n,A}$ and the IRN density of the OTA, $V_{n,OTA}$ is written as

$$V^2_{n,A} = \left(\frac{C_0 + C_{p,in} + C_f}{C_0}\right)^2 V^2_{n,OTA} \quad (6)$$

To achieve an ECG system with low power consumption and low noise performance, it is necessary to design an OTA having input-referred noise with low power consumption.

2.2 Main OTA Amplifier

The two-stage Millar OTA is one of the most commonly used in bio-medical applications for its wider output swing and better linearity. Our design achieves a very efficient power–noise factor because the OTA employs an inverter-based differential input stage, which is exploited to double the transconductance under the same bias current, for low noise used in [15]. The transconductance of the OTA must be maximized for a given total current. To ensure the loop stability, Miller-compensation capacitor (Cc) and nulling active resistor (Rz) are added to achieve a phase margin larger than 60 degrees. The schematic of our low-noise OTA is shown in Fig. 4.

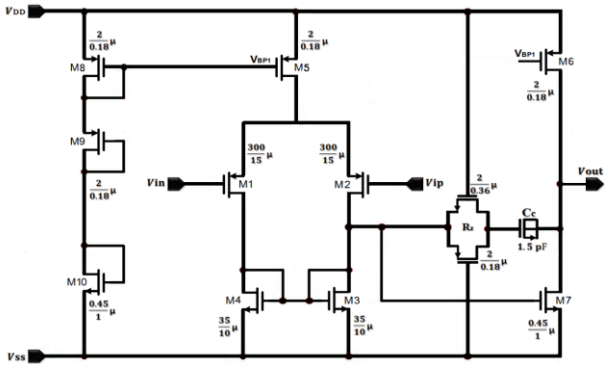


Fig. 4: Schematic of the proposed OTA with aspect ratios (W/L).

Subthreshold biasing of transistors reduces transistor noise and power consumption by allowing the minimum operating voltage to be reached. Exponential current behavior is observed in MOSFETs in the weak inversion [16]. In other words, the gate-source voltage increases exponentially with the biasing current of a MOSFET in weak inversion. To model the threshold-voltage mismatch, we use the current equation in weak inversion [17],

$$I_D \approx I_{D0} \frac{W}{L} \; e^{q\left(\frac{Vgs-Vth}{\eta KT}\right)} \tag{7}$$

$$I_{D0} \approx \mu C_{ox} \frac{W}{L} \left(\frac{KT}{q}\right)^2 e^{-\left(\frac{qVth}{\eta KT}\right)} \tag{8}$$

Where I_{D0} is the current at threshold-voltage and is depending on the process and geometry of the device, Vth is the threshold voltage, η is the transistor's subthreshold swing coefficient, which is greater than 1, C_{ox} is the gate-oxide capacitance per unit area. Knowing that the transistor operating in the saturation region, illustrated in (7). For transistors operating in the subthreshold region, the EKV model can be applied to estimate the transconductance [18],

$$g_m = \frac{\partial Id}{\partial Vgs} \approx \sqrt{2\beta Id} \tag{9}$$

$$g_m = \frac{\partial Id}{\partial Vgs} \approx \frac{q}{\eta KT} \; e^{q\frac{Vgs}{\eta KT}} \approx \frac{qId}{\eta KT} \approx \frac{Id}{\eta V_T} \tag{10}$$

Where Id is the drain current through the MOS transistor, V_T is equal to KT/q , referred as thermal voltage of 26 mV at absolute temperature T of 300 K, where q is the electron charge, k is Boltzmann's constant. It shows that the transconductance increases exponentially with low supply and biasing voltages, we can say that it is linearly proportional to the biasing current I_D. It is preferable to operate the inverter-based input pairs in the subthreshold region in order to get a high transconductance value and flicker noise suppression in the signal bandwidth. As a result, a bigger input transistor size ratio contributes to a higher gain since the transconductance gm is directly contributing to the gain of the amplifier, to decrease flicker noise and enhance the CMRR as much as feasible, for extracting excellent ECG signal quality [15].

2.1.1 Noise Analysis of OTA and Noise Efficiency Factor

The efficiency of the noise-to-power ratio is dependent on the biasing of the input transistors in the weak inversion region [10-19]. The input-referred noise is inversely proportional to gm according to the following relation,

$$V^2_{ni}/\Delta f = \frac{1}{g_{m1}{}^2}[4KT\eta gm_1 + 4KT\eta gm_4 + 8KT\gamma gm_8]$$

$$V^2_{ni}/\Delta f = \frac{16KT}{3.gm_1}\left[\eta\frac{3}{4} + \eta\frac{3}{4}\frac{gm_4}{gm_1} + \frac{gm_8}{gm_1}\right] \tag{11}$$

If gm_1 is much greater than $g_{m4,8}$ so,

$$V^2_{ni}/\Delta f \approx \frac{4KT\eta}{gm_1} \tag{12}$$

The input-referred noise voltage of the OTA where the MOS transistor operating in the weak inversion is expressed using (10) and (14) as,

$$V_{ni,rms} = \sqrt{\frac{4KT.V_T.\eta^2}{I_D}.\frac{\pi}{2}.BW} \tag{13}$$

Using the power spectral density (PSD) of noise current of MOSFET operating in the subthreshold region expressed as,

$$i^2_{ni} = 2KT\eta gm$$
$$i_{ni} = \sqrt{2KT\frac{I_D}{V_T}} \tag{14}$$

Because the spectrum density of flicker noise is inversely related to the transistor area, WL, and frequency, the flicker noise is decreased by utilizing input transistors with a wide width and length in (13). The 1/f voltage noise density in a MOS can be written as,

$$V^2_n = \frac{1}{f}\frac{K}{C_{ox}WL} \tag{15}$$

The noise efficiency factor (NEF) is defined in [20] and is used to determine how effectively a

capacitive-feedback amplifier uses its bias current to minimize noise,

$$NEF = V_{ni,rms}\sqrt{\frac{2I_{tot}}{\pi.V_T.4KT.BW}} \quad (16)$$

where $V_{ni,rms}$ is the IRN voltage, I_{tot} is the total current, V_T is the thermal voltage, k is Boltzmann's constant, T is the temperature in Kelvins (body temperature =300K), and BW is the -3dB bandwidth of the capacitive-feedback amplifier in Hz.

2.3 Driven-Right-Leg (DRL) Circuit

To decrease the effect of common-mode interference voltage caused by combining ECG signals with PLI [1]. A Driven Right Leg Circuit (DRL) is added to the instrumentation amplifier (IA) to sense the common-mode signal then put it as an input in auxiliary inverting amplifier, inverts it and then drives it back to the body via the right leg electrode. With this active grounding (DRL), actively canceling the electromagnetic interference from the 50Hz electrical power lines that are picked up by the patient's body. This picked-up interference is what generates the common-mode voltage V_{CM}, which cancels to increase the CMRR in order to generate a clean electrical measurement of the patient's body [21]. The output voltages of the amplified input voltages of the two signal electrodes are averaged by a resistive divider built using two identical resistors R_D. The DRL circuit is simplified by isolating the new parts of the configuration shown in Fig. 5.

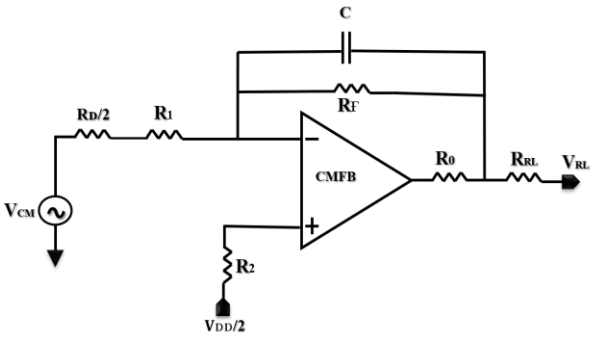


Fig. 5: Driven Right Leg Circuit (DRL) Configuration.

The reduction of the common-mode voltage V_{CM} is proportional to the gain of the feedback loop, this is why the CMFB was designed with a stable and almost zero gain to avoid oscillation, otherwise sufficient phase margin cannot be guaranteed and lead to potential oscillation. The DRL circuit can also provide some electrical safety to the patient. To clarify, R_0 is included to protect the patient and the instrument from a possible short-circuit. It acts to limit the current during a possible short-circuit [22], which would lead to a saturated the op-amp (+Vsat= V_{DD}). If there is a short circuit, the output of the op-amp will be short circuited to V_{DD}, consequently the patient will be electrocuting, so there must be at least a resistance between this short circuit and the body which will limit the amount of current. Therefore, the DRL allows us to safely ground the body, especially with the current limiting resistor R_0.

$$I_{short} = \frac{+Vsat}{R_0} = \frac{V_{DD}}{R_0} \quad (17)$$

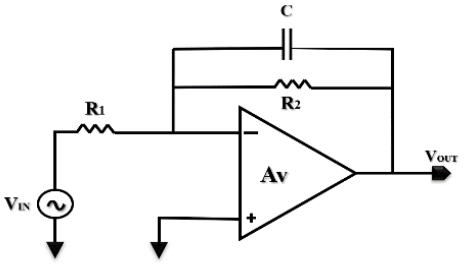
Where I_{short} is the current of the short circuit, +Vsat is the saturation voltage of the op-amp powered between power supply V_{DD} and ground, and R_0 is the protection resistance.

The role of the capacitor C in the feedback loop is to ensure stability by increasing the phase margin to prevent oscillation.

2.4 Filters Circuits

The amplified ECG signal is passed through a filter to remove the noises in the recording. The power-line interference is narrow-band noise centered around 50Hz, making it more difficult to analyze and interpret the ECG. To remove it, a notch filter with a cutoff frequency of 50 Hz is utilized [5]-[8]. However, these signals are odd multiple and can be filtered using a Low Pass Filter with a cutoff frequency of 100Hz.

While, to remove the other ECG contaminants like the Motion Artifacts, as well as, the Baseline Wandering and EMG noise, a Second order High Pass Filter with a cutoff frequency of 0.5 Hz can be used to filter out noises with a frequency range of 0.5 Hz [8]-[9]. Hence, we can have an ECG signal from 0.5Hz to 100Hz, but our main major intention is to find out the BPM (Beats Per Minute). To compute the BPM, QRS complexes are used by counting the numbers of QRS peaks are getting in a minute. In general, the frequency of the QRS peak is about 20Hz [23].



(a)

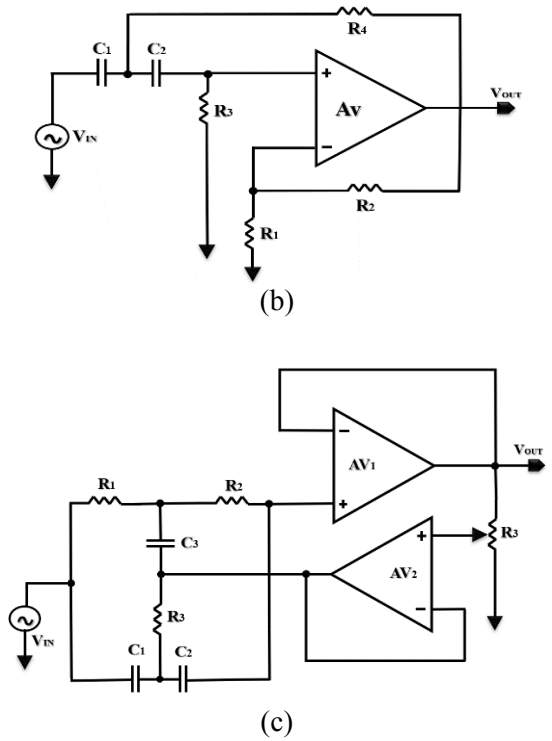


Fig. 6: Filtering bloc (a) Low Pass Filter (b) High Pass Filter (c) Notch Filter.

3 Problem Solution

The Smart Wearable ECG Amplifier is implemented in a 0.18µm CMOS technology. The proposed ECG acquisition system is simulated using Cadence Spectre environment for a total bias current of 600 ηA for a power consumption of 1.08 µW at the supply voltage of 1.8V

The Ac response of the system can be observed in the following Fig. 7(a). The amplifier was designed to give a gain of 345 by setting the value of C_0 to 50 pF and Cf to 145 fF. The mid-band gain of the amplifier is 50.75 dB, which gives satisfaction that our system is able to amplify weak signals with reduced noise. The gain value is specified at 20 Hz which is achieved at the −3dB bandwidth ranges from 0.077 to 255 Hz. The simulated high-pass cutoff frequency is slightly lower than the declared value of the main signal. This difference is caused by the feedback network of the OTA, and besides the frequency of the QRS peaks is around 20Hz. The mid-band gain of the CMFB shown in Fig. 7(b) is set to 0 dB to avoid oscillation.

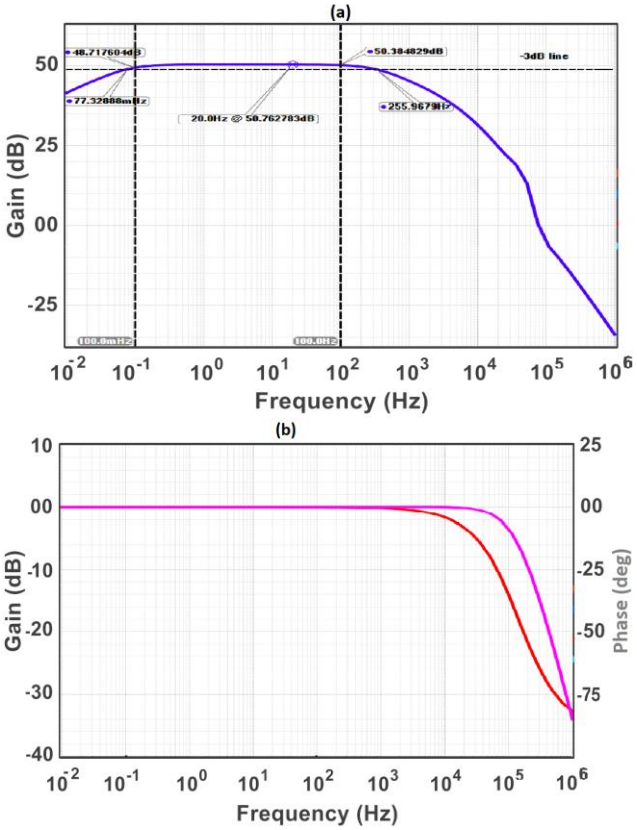


Fig. 7: AC response (a) The mid-band gain of ECG amplifier (b) The CMFB gain

Fig. 8 shows the simulated output noise power spectral density of the proposed amplifier. The total IRN is 1.47 µVrms integrated from 100mHz to 1KHz, which is obtained by dividing the output noise spectrum by the mid-band gain of the amplifier. The output noise power spectral variation according to the input amplitude changes specified at 20 Hz is shown in Fig. 9.

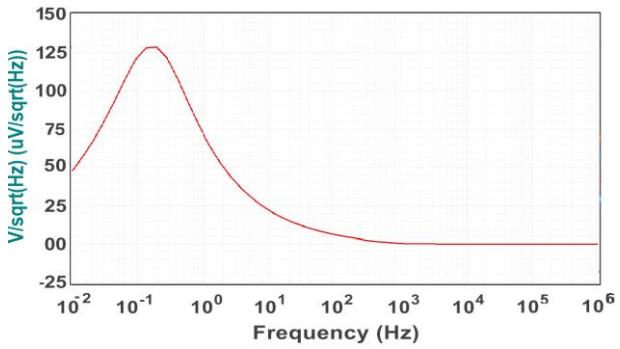


Fig. 8: Output noise power spectral density.

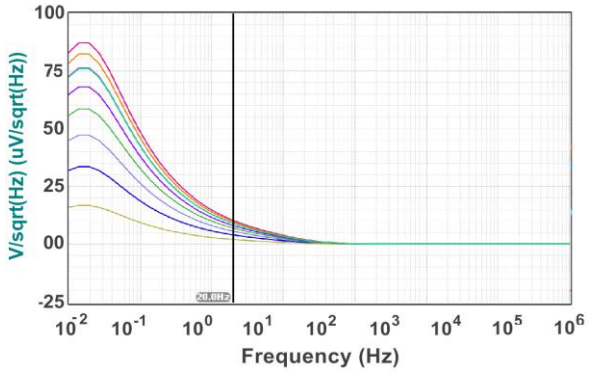


Fig. 9: Output noise power spectral with input amplitude changes at 20 Hz.

Figs. 10(a) and 10(b) presents the plot of common-mode gain, which illustrate the effect with and without the DRL circuit. CMRR is calculated as the ratio of the differential-mode gain to the common-mode gain. PSRR is calculated as the ratio of the differential-mode gain to the gain from the power supply to the output, which indicates the ability of a circuit to eliminate any ripple in the circuit power supplies. Fig.11 shows the measured PSRR of the ECG amplifier. The measured CMRR and PSRR exceed 101.4 dB and 112.38 dB over the range of 0.1 to 100 Hz, respectively.

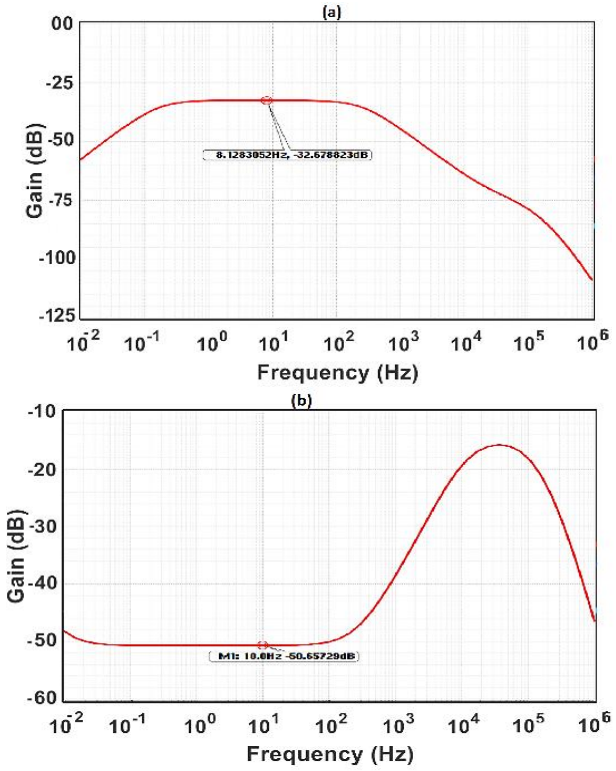


Fig. 10: Common-mode gain simulation (a) without DRL (b) with DRL circuit.

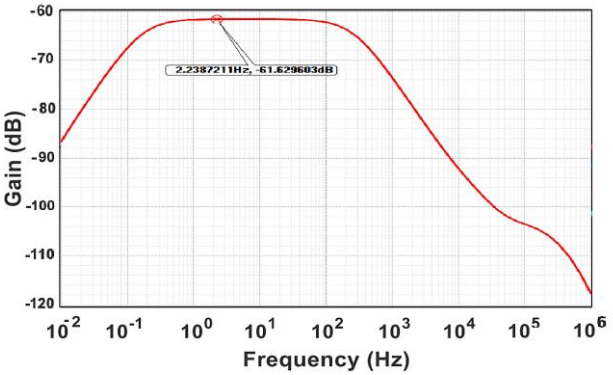


Fig. 11: Supply coupling to the output (PSRR) simulation result.

The notch filter is used to limit the impact of AC powerline interference, which can have a big impact on weak ECG signals. The magnitude frequency response of the notch filter is shown in Fig. 12(a). Furthermore, the transient simulation of a signal with a frequency of 50hz used, this input signal is clipped respectively, as shown in Fig. 12(b).

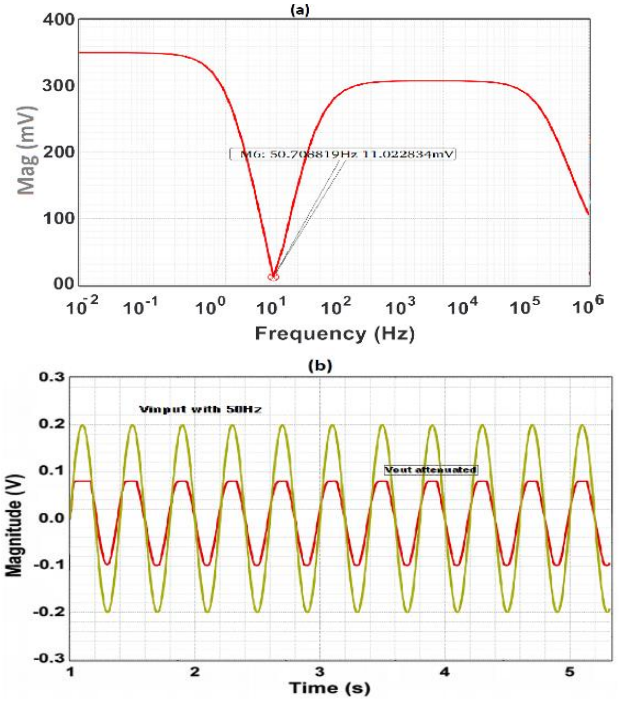


Fig. 12: Notch filter Simulation (a) The magnitude frequency response (b) The transient simulation.

Fig. 13 shows the simulation transient response of an ECG signal without a DRL circuit, which is typically affected by a powerline interference and electromagnetic interference. Fig. 14 illustrates an ECG signal interfered by an electrode contact noise (Motion Artifacts) and muscle artifacts (EMG noise).

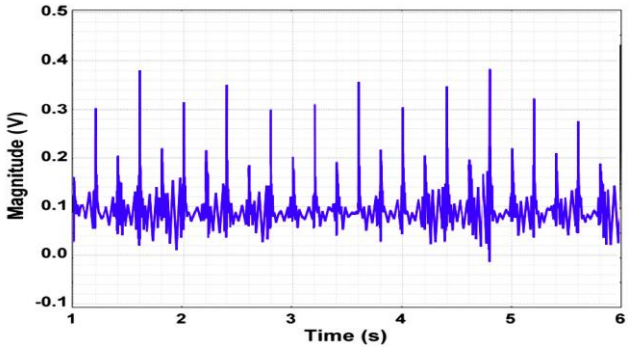


Fig. 13: ECG affected by powerline (50Hz) interference and electromagnetic noise.

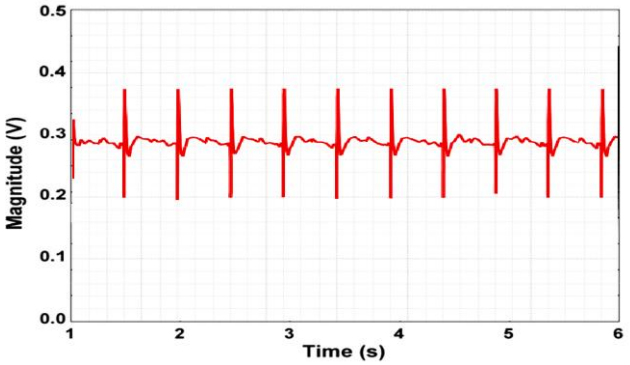


Fig.14: ECG signal with electromyographic (EMG) noise and affected by electrode motion artifacts.

These noises are suppressed using filter stages. Accordingly, a high-pass filter with a 0.5 Hz cutoff frequency was used to remove muscle artifacts and other ECG contaminants, while a notch filter with a cutoff frequency of 50Hz was used to eliminate PLI, and a DRL circuit was added to suppress the common-mode interference produced by the body. The simulated transient response of the proposed ECG signal amplifier is shown in Fig. 15, which proves that the amplifier performs well for the recording of ECG signals.

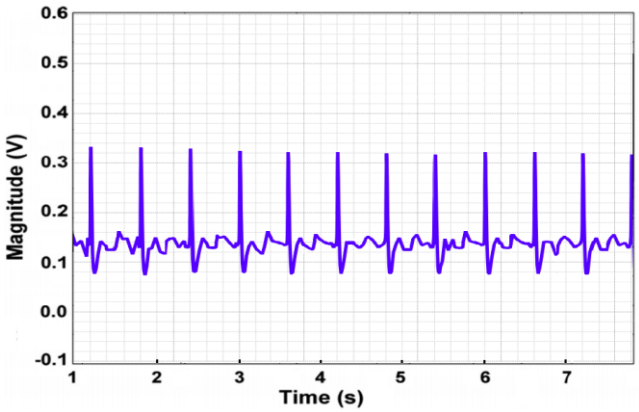


Fig. 15: Simulated transient response of ECG signal amplifier with noises removed.

The proposed amplifier's NEF is evaluated to be 2.74. The power-efficiency factor (PEF) that includes the supply voltage V_{DD} is also an important parameter to evaluate the power efficiency for biomedical amplifiers. As given in [24],

$$PEF = NEF^2.V_{DD} \quad (18)$$

The measured performances of the amplifier are summarized in Table 1, with a comparison to other related works. Over the last years, remarkable work has been done in this field. Our amplifier exhibits the lowest power consumption compared to previous work [15, 25-26]. Although the proposed amplifier achieves the best IRN among the the results in the comparison table. Comparing the NEF, we noticed that our measured NEF is a little larger than the other amplifiers quoted in the measurement results. Therefore, the PEF for this work is not the best one, but it is better than the designs in [15] and [26] which are fabricated in similar technologies.

4 Conclusion

The electrocardiogram (ECG) machine monitors the heart rhythm and electrical activity of the patient. A micropower low-noise ECG recording amplifier is presented in this study, which is developed in a 0.18µm CMOS process with a DRL circuit to reduce PLI and a filtering bloc to remove ECG impurities. The OTA employs inverter-based differential pairs in the first stage to improve the power-to-noise efficiency. The system can amplify weak signals with a gain of 50.75 dB, CMRR of 101.4 dB and input-referred noise of 1.47 µVrms thereby reducing noise efficiency factor (NEF) to 2.74. However, when compared to comparable state-of-the-art designs, this design's NEF is adequate. The total power consumption was 1.08 µW with a power supply voltage of 1.8 V. The measurement results shows that the amplifier achieves good performance in terms of linearity, power and noise and has the ability to record ECG signals, but the constraint is the offset problem. In future designs, a more optimized OTA topology is required to reduce noise and reduce overall power consumption as well as correct for the offset obtained.

Table 1. Measured performances summary and comparison

Parameters	This Work	[7]	[10]	[11]	[15]	[25]	[26]
Tech. (μm)	0.18	0.35	0.18	0.18	0.5	0.18	0.18
V_{DD} (V)	1.8	2	1.8	1.5	2.8	1.8	1.8
Power (μW)	1.08	0.32	1.53	0.855	7.56	4.5	8.4
Gain (dB)	50.75	39.8	40.02	47.6	40.85	34.5	49.52
Bandwidth (Hz)	0.077∼255	0.2∼200	5.69∼5.45k	0.64∼500	45∼5.32k	1.7∼352	98.4∼9.1k
NEF	2.74	2.26	1.58	2.91	2.67	2.99	4.9
PEF	13.51	10.2	4.5	10.16	19.96	16.09	43.2
IRN (μVrms)	1.47 0.1∼1kHz	2.05 0.1∼10k	3.27 5.69∼5.45k	2.24 0.5∼500	2.67 10∼98k	3.69 0.5∼350	5.6 98.4∼9.1k
CMRR (dB)	102	65	66.55	105.6	66	174	50
PSRR (dB)	113	70	54.99	NA	75	80	50

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