Improved positive output voltage super-lift Boost converter

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Abstract: - Starting from the positive output voltage-lift Boost converter, which has a higher voltage transformation ratio and reduced voltage stress across the semiconductors, the additional losses caused by the periodic recharging of the intermediate capacitor are analyzed. An additional inductor improves the efficiency of this converter. The dimensioning of this improved converter, its dynamic behavior, the inrush-current and a feed-forward control are treated. The considerations are supported by simulations.

Key-Words: - DC-to-DC converter, feedforward control, boost converter, dynamics, simulation, Bode plots

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1 Introduction

The starting point of this investigation was the paper [1] describing a Boost converter (Fig. 1) with reduced voltage stress at the electronic switch. One can find this converter also in [2]. The original source is treated in [3]. A comprehensive review of voltage-boosting techniques with a reference list of 309 items can be found in [4]. Basics are discussed in the text books e.g. [5, 6]. In [7] about hundred DC-to-DC converters are constructed. Six self-lift DC-DC converters are presented in [8]. Other interesting papers which all have further references are e.g. [9-13].

The converter consists of one electronic switch (S), two diodes (D_1, D_2), and two capacitors (C_1, C_2) and is shown in Fig. 1.

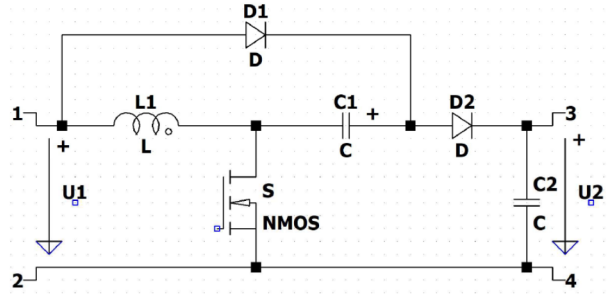

Fig. 1. Basic converter (positive output voltage-lift Boost converter).

2 Discussion of the basic converter

2.1 Basics

The converter has two modes in the continuous conduction mode. During mode M1 the electronic switch S and the first diode D_1 are conducting. When S is turned off, the current through the inductor L commutates into D_2 and supplies the output. For the basic analyses we assume that the capacitors are large enough, so that the voltage across them is nearly constant. Furthermore, we provide ideal devices and steady-state mode. Inspecting the circuit, one can easily see that when S is turned on, the series connection of diode D_1 and C_1 is in parallel to the input voltage U_1. Therefore, the voltage across C_1 must be equal to the input voltage (remember an ideal diode D_1). When the switch is turned off, the current through L_1 commutates into C_1 and D_2. C_1 loses energy and the voltage across it decreases. When the switch is turned on again in the next switching period, the capacitor is again recharged up to the input voltage. For the stationary case we can therefore write

$$U_{C1} = U_1 \,. \tag{1}$$

The voltage-time balance for L_1 leads to

$$U_1 d = \left|U_1 - U_2 + U_{C1}\right|(1-d) \,. \tag{2}$$

The voltage transformation ratio is therefore

$$M = \frac{U_2}{U_1} = \frac{2-d}{1-d} \tag{3}$$

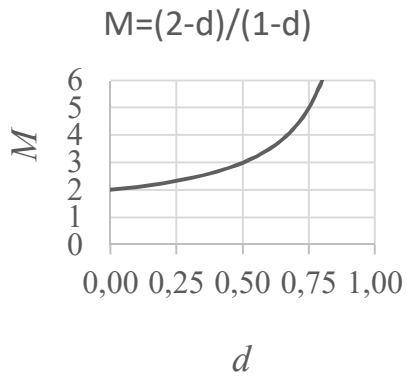

Fig. 2. Voltage transformation ratio.

Fig. 2 shows the voltage transformation ratio.
The converter is especially useful for a step-up ratio of three or more. This is achieved by a duty cycle of equal to or greater than 0.5.
The voltage stress across the active switch is reduced to

$$U_S = U_2 - U_1 . \tag{4}$$

The stress of D_2 is also reduced by the same value.
The voltage across D_1 is also only

$$U_{D1} = U_1 - U_2 \ . \tag{5}$$

All semiconductors have to withstand only the output voltage reduced by the input voltage. For the normal Boost converter, the stress is equal to the output voltage.

A disadvantage of this concept is the fact that the capacitor C_1 is charged abruptly when the active switch is turned on. During the off-time of the transistor, this capacitor is discharged by the inductor current through L_1 and the voltage across it decreases to a value lower than the input voltage. Summing up all parasitic resistors (of the electronic switch, of the diode, of the capacitor, of the input source, and of the wiring) to R one can write, when the switch is turned on and the voltage across C_1 is U_1 minus ΔU_{C1}, the mesh equation

$$U_1 = Ri + \frac{1}{C_1}\int_0^t idt + U_1 - \Delta u_{C1} \ . \tag{6}$$

It is better to include also the knee-voltage V_D of the simple diode model. Therefore, one can write for the charging current of C_1

$$U_1 = Ri + V_D + \frac{1}{C_1}\int_0^t idt + U_1 - \Delta u_{C1} , \tag{7}$$

$$\Delta u_{C1} - V_D = Ri + \frac{1}{C_1}\int_0^t idt . \tag{8}$$

Laplace transformation results in

$$\frac{\Delta u_{C1} - V_D}{s} = R \cdot I(s) + \frac{1}{C_1}\cdot\frac{1}{s}\cdot I(s) \tag{9}$$

$$I(s) = \frac{\Delta u_{C1} - V_D}{R}\frac{1}{s + \frac{1}{C_1 \cdot R}} . \tag{10}$$

Transformation into the time-domain leads to,

$$i(t) = \frac{\Delta u_{C1} - V_D}{R}\exp\left(-\frac{1}{C_1 \cdot R}t\right) . \tag{11}$$

Keep in mind that this current flows through the transistor additional to the current through L_1.
The additional peak current is therefore

$$\hat{I} = \frac{\Delta u_{C1} - V_D}{R} \tag{12}$$

and the time constant is

$$\tau = C_1 \cdot R \tag{13}$$

During the on-time of the electronic switch the recharge process should be completed. So the minimal on-time of the transistor has to be about five times of the time constant

$$T_{\min} = 5 \cdot \tau = 5 \cdot C_1 \cdot R . \tag{14}$$

2.2 Losses of the recharge process

Fig. 3 shows the input current, the current through the coil, the load current, also the output and the input voltage and the gate signal of the original converter. The input current is only limited by the parasitic resistances of the diode, of the first capacitor and the transistor. This leads to an efficiency of 94.8 %.

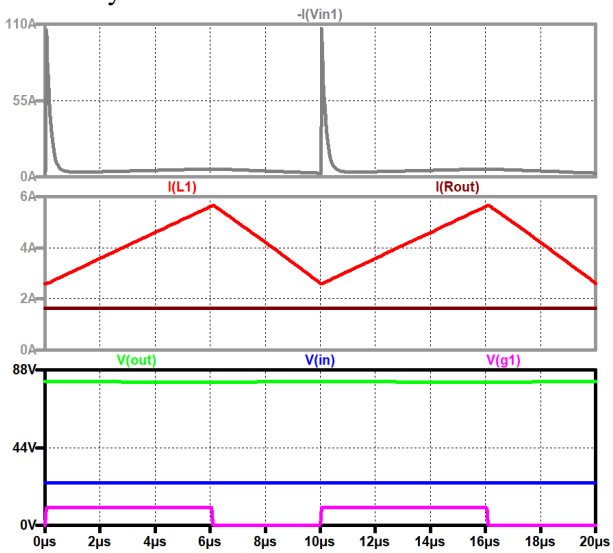

Fig. 3. Original converter up to down: input current; current through the coil, load current; output voltage, input voltage, control signal.

Supposing that the time constant is smaller than a fifth of the duration of mode M1, one can write for the energy which is transformed within the resistor into heat (one can use infinity as upper limit of the integral, making only a negligible error) (15)

$$W_R = \int_0^\infty u_R i dt = \int_0^\infty Ri^2 dt = \int_0^\infty R\frac{\left(\Delta u_{C1} - V_D\right)^2}{R^2}\exp\left(-\frac{2}{C_1 \cdot R}t\right)dt$$

$$W_R = \frac{C_1 \cdot \left(\Delta u_{C1} - V_D\right)^2}{2} \ . \tag{16}$$

The dissipated losses across R are therefore

$$P_R = f\frac{C_1 \cdot \left(\Delta u_{C1} - V_D\right)^2}{2} \tag{17}$$

The important fact is: the losses are independent of the value of the resistor. Using the best possible devices does not reduce them!
With these findings one can design a resistor, so that the current peak does not exceed a maximum value

$$R \geq \frac{\Delta u_{C1} - V_D}{\hat{I}} \ . \tag{18}$$

On the other side the resistor must be smaller than

$$R \leq = \frac{T_{\min}}{5 \cdot C_1} \tag{19}$$

to recharge the capacitor. In R are now included the parasitic resistors and the additional current limiting resistor, which has to be connected in series with diode D_1.

Inserting a resistor to reduce the charge impulse the efficiency (now 95.2 %) increases a little, due to the nonlinear characteristics of the diode. Fig. 4 shows the same signals as Fig. 3.

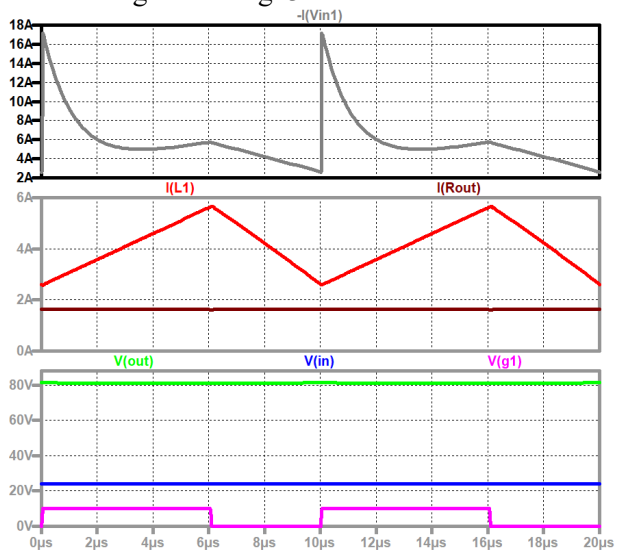

Fig. 4. Original converter with damping resistor, up to down: input current; current through the coil, load current; output voltage, input voltage, control signal.

3 Improvement of the converter

The main drawback of the discussed converter is the fact that the input voltage is periodically applied to the capacitor C_1 and it is always recharged. When the parasitic resistors are small, the peak current is high. To reduce this peak current a resistor can be included in series to diode D_1. The losses are not increased and the efficiency is not reduced. A small change in the converter topology (Fig. 5), however, can improve the efficiency of the converter.

3.1 Resonant recharging

Another concept which has fundamentally no losses (for ideal devices; the recharging with the e-function has principally always losses according to (17) independent of the quality of the devices) is charging C_1 with a resonant circuit. In this case a small resonant inductor L_2 has to be connected in series to the diode D_1 instead of a current limiting resistor. The circuit is shown in Fig. 5.

When the transistor is turned on, the following mesh exists

$$U_1 = L_2 \frac{di}{dt} + Ri + V_D + \frac{1}{C_1}\int_0^t idt + U_1 - \Delta u_{C1} \tag{20}$$

$$\Delta u_{C1} - V_D = L_2 \frac{di}{dt} + Ri + \frac{1}{C_1}\int_0^t idt \ . \tag{21}$$

In the resistor R again all parasitic resistors of the loop are subsumed.

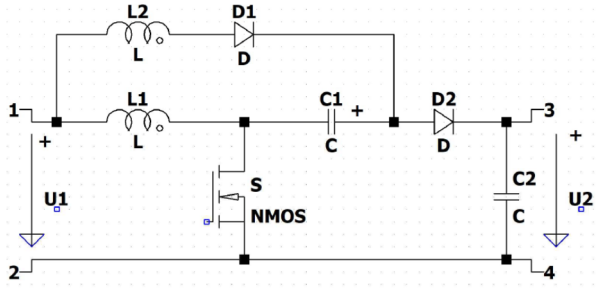

Fig. 5. Improved converter.

Laplace transformation leads to

$$I(s) = \frac{(\Delta u_{C1} - V_D)}{L_2\left[\left(s + \frac{2R}{L_2}\right)^2 - \frac{4R^2}{L_2^2} + \frac{1}{C_1 L_2}\right]} \ . \tag{22}$$

The recharging occurs as a damped sinus-wave (23)

$$i(t) = \frac{\Delta u_{C1} - V_D}{L_2\sqrt{\frac{1}{C_1 L_2} - \frac{4R^2}{L_2^2}}} \exp\left(-\frac{2R}{L_2}\right) \sin\left(\sqrt{\frac{1}{C_1 L_2} - \frac{4R^2}{L_2^2}}\, t\right) \ .$$

Neglecting the small parasitic resistor R, one obtains a pure sinus current wave

$$i(t) = (\Delta u_{C1} - V_D)\sqrt{\frac{C_1}{L_2}} \sin\left(\sqrt{\frac{1}{C_1 L_2}}\, t\right) \ . \tag{24}$$

The charging current has the maximum value

$$\hat{I} = (\Delta u_{C1} - V_D)\sqrt{\frac{C_1}{L_2}} \ . \tag{25}$$

The period of the ringing can be calculated with the equation

$$\omega = 2\pi f = \frac{2\pi}{T} = \sqrt{\frac{1}{C_1 L_2}} \ . \tag{26}$$

The current reaches zero after a half-period. Therefore, the minimal on-time must be

$$T_{on,\min} = \pi\sqrt{C_1 L_2} \tag{27}$$

Fig. 6 shows the input current, the current through the coil, the load current, also the output and the input voltages and the gate signal of the improved converter. The charging current now has a sinusoidal form and the dissipation is again reduced and the efficiency has increased to 97.2 %. The main part of the losses is produced by the diodes. Therefore, more emphasis should be placed on the selection of the diode.

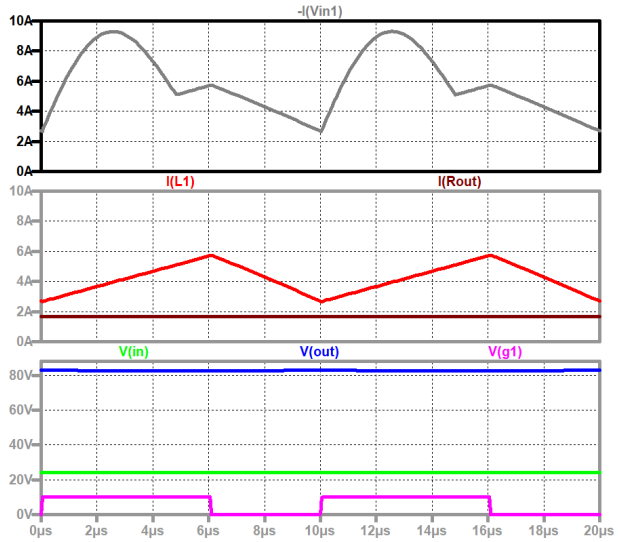

Fig. 6. Improved converter up to down: input current; current through the coil, load current; output voltage, input voltage, control signal.

4 Dimensioning of the converter

The converter is especially useful for a step-up ratio of about three to five. So the duty cycle is more than 50%. The recharge of C_1 can therefore last half of the switching period.

The output capacitor has to supply the load when the transistor is turned on. The voltage across it decreases with the nearly constant load current according to

$$\Delta u_{C2} = \frac{1}{C_2}\int_0^{d\cdot T} I_{Load}\,dt = \frac{I_{Load}\cdot d\cdot T}{C_2} \quad . \tag{28}$$

Using the switching frequency instead of the switching period leads to a capacitor value of

$$C_2 = \frac{I_{Load}\cdot d}{\Delta u_{C2}\cdot f} \quad . \tag{29}$$

To get a dimensioning equation with the input and the output voltages as parameters one can insert

$$d = \frac{U_2 - 2U_1}{U_2 - U_1} \quad . \tag{30}$$

Now one gets the formula

$$C_2 = \frac{U_2 - 2U_1}{U_2 - U_1}\cdot\frac{I_{Load}}{\Delta u_{C2}\cdot f} \quad . \tag{31}$$

The main inductor can be designed as in a normal boost converter. During the on-time of the active switch S, the input voltage is applied to L_1 and the current increases by ΔI_{L1}, leading to the equation

$$U_1 = L_1\frac{\Delta I_{L1}}{d\cdot T} \, . \tag{32}$$

Rearranging and including again (30) leads to

$$L_1 = \frac{U_1\cdot d\cdot T}{\Delta I_{L1}} = \frac{U_2 - 2U_1}{U_2 - U_1}\cdot\frac{U_1}{\Delta I_{L1} f} \quad . \tag{33}$$

Now one has to design the resonant circuit. It is obvious that C_1 should not be too large, because the resonant process can last only half of the switching period. When the transistor is turned off, the inductor current flows through C_1 and discharges it by the value ΔU_{C1}

$$\Delta u_{C1} = \frac{1}{C_1}\int_{d\cdot T}^{T} \bar{I}_{L1}\,dt = \frac{\bar{I}_{L1}\cdot(1-d)\cdot T}{C_1} \quad . \tag{34}$$

The mean value of the inductor current and the load current can be found from the charge balance of capacitor C_2 in steady-state according to

$$I_{Load}\cdot d = \left(\bar{I}_{L1} - I_{Load}\right)(1-d) \tag{35}$$

$$\bar{I}_{L1} = \frac{I_{Load}}{1-d} \, . \tag{36}$$

This leads to

$$\Delta u_{C1} = \frac{1}{C_1}\int_{d\cdot T}^{T} \bar{I}_{L1}\,dt = \frac{I_{Load}\cdot}{C_1\cdot f} \tag{37}$$

$$C_1 = \frac{I_{Load}\cdot}{\Delta u_{C1}\cdot f} \quad . \tag{38}$$

With the frequency of the converter and assuming a minimal duty cycle in the steady-state of 0.5, one gets the minimal on-time (during which C_1 has to be recharged) and therefore the inequality

$$L_2 \le \frac{T_{on,\min}^2}{\pi^2 C_1} \quad . \tag{39}$$

Now one chooses the amplitude of the resonance wave and obtains a second inequality for L_2

$$L_2 \ge \frac{\left(\Delta u_{C1} - V_D\right)^2 C_1}{\hat{I}^2} \quad . \tag{40}$$

5 Turn on of the input voltage

It is always an interesting question: “what happens when the converter is applied to the input source?”. When the output capacitor C_2 is discharged and the input voltage is applied, both diodes turn on. L_2 and C_2 form now a series resonance circuit causing a high current peak which charges the output current. This input peak current can be estimated according to

$$\hat{I}_{INL2} = U_1\sqrt{\frac{C_2}{L_2}} \quad . \tag{41}$$

In reality it will a bit lower caused by the parasitic elements, especially the resistor of the input source (which is in the steady-state shunted by an input capacitor) and of the diodes. At the same time a second resonance occurs. The resonance circuit consists of the main inductor L_1 and the series

connection of C_1 and C_2. The additional input current has the amplitude

$$\hat{I}_{INL1} = U_1 \sqrt{\frac{C_1 C_2}{L_1 (C_1 + C_2)}} \quad , \tag{42}$$

which is much lower, because the effective capacity is lower and the inductor is larger. During the first half-period the voltage across C_1 starts at first in the negative direction. When D_2 turns off, the voltage across C_1 is still negative and the resonance circuit is charged. Now the effective resonant circuit consists of the series circuit of L_1 and L_2 and of C_1. The resonant angular frequency is now

$$\omega_{on3} = \sqrt{\frac{1}{C_1 (L_1 + L_2)}} \quad . \tag{43}$$

The resonance inductor L_2 is much smaller than the converter coil L_1. The angular frequency can be approximated by

$$\omega_{on3} \approx \sqrt{\frac{1}{C_1 L_1}} \quad . \tag{44}$$

A high frequency ringing can occur during this time after the blocking of diode D_2 and across the active switch S caused by the parasitic capacitance of the semiconductor devices. If necessary, they can be damped by small snubbers.

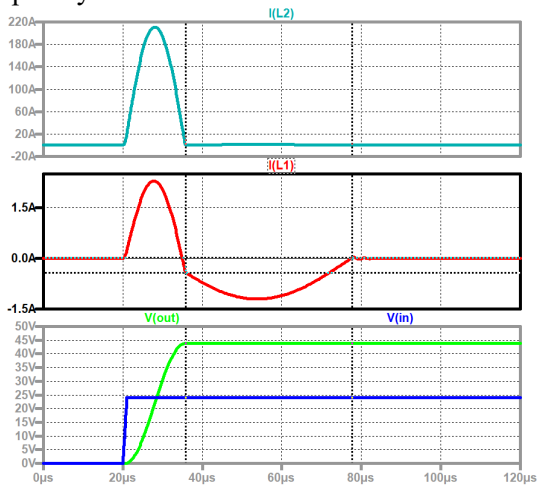

Fig. 7. Turn on of a low impedance input source, up to down: current through L_2; current through L_1; output and input voltages.

Fig. 7 shows the simulation of the inrush currents. The main peak appears through D_1 and a much smaller through the main inductor L_1 (compared to the current through L_2 it can be neglected). If the source is e.g. a battery of a car, a big inrush current will occur. In this case a current limiting device may be necessary. The simplest way would be to connect a resistor between the input source and the converter, so the charging would occur by an e-function. After the output voltage has reached a steady state, this resistor has to be short-circuited, e.g. by a mechanical contact of a relay. When the input source has current limiting behavior (e.g. a solar generator or fuel cells), the capacitor will be charged by a constant current and no extreme inrush current occurs.

5 Feedforward control

With the reference value U_2^* one can calculate the control law according to

$$d = \frac{U_2^* - 2U_1}{U_2^* - U_1} \quad . \tag{45}$$

Fig. 8 shows the feedforward controlled converter. When the input voltage is applied, there is an overshot of the output voltage. For soft-start the reference value increases with a ramp; when the reference voltage reaches double the input voltage the output voltage starts to increase and within half of a millisecond the output voltage follows the reference value. The difference between the reference value and the output voltage is caused by the non-exact control law which was calculated from the ideal voltage transformation ratio. From 10 ms on till 20 ms the reference stays constant. At 20 ms there is a reference value step of 10 V down. Some ringing occurs at the output. 10 ms later an input voltage step occurs. As the input voltage is included in the control, the output voltage reaches nearly the same value as before after a short ringing.

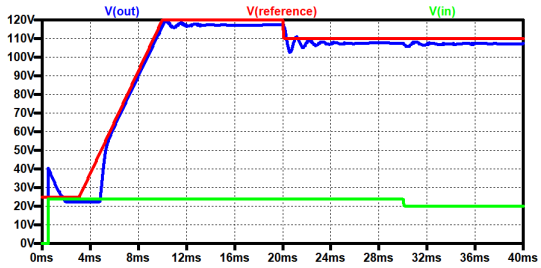

Fig. 8. Feedforward controlled converter: reference value (red), output voltage (blue), input voltage (green).

5 Dynamics of the converter

For treating the dynamic behavior of the converter the inductor L_2 and the intermediate capacitor C_1 can be omitted, due to the facts that within each period the capacitor is recharged to the input voltage and that the current through L_2 reaches zero at the end of the recharging process. So we can write for the state equations during mode M1 (the input voltage lies across the inductor, and the output capacitor supplies the load)

$$\frac{di_{L1}}{dt} = \frac{u_1}{L_1} \tag{46}$$

$$\frac{du_{C2}}{dt}=\frac{-u_{C2}/R}{C_2} \quad . \tag{47}$$

In mode M2 (diode D_2 is conducting) we have

$$\frac{di_{L1}}{dt}=\frac{2u_1-u_{C2}}{L_1} \tag{48}$$

$$\frac{du_{C2}}{dt}=\frac{i_{L1}-u_{C2}/R}{C_2} \quad . \tag{49}$$

Combining these equations with the help of the state-space averaging leads to

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix}=\begin{bmatrix} 0 & \frac{d-1}{L_1} \\ \frac{1-d}{C_2} & -\frac{1}{C_2R} \end{bmatrix}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix}+\begin{bmatrix} \frac{2-d}{L} \\ 0 \end{bmatrix}(u_1) \quad . \tag{50}$$

Linearizing this nonlinear differential equation results in (51)

$$\frac{d}{dt}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix}=\begin{bmatrix} 0 & \frac{D_0-1}{L_1} \\ \frac{1-D_0}{C_2} & -\frac{1}{C_2R} \end{bmatrix}\begin{pmatrix} \hat{i}_{L1} \\ \hat{u}_{C2} \end{pmatrix}+\begin{bmatrix} \frac{2-D_0}{L_1} & \frac{U_{C20}}{L_1} \\ 0 & -\frac{I_{L10}}{C_2} \end{bmatrix}\begin{pmatrix} \hat{u}_1 \\ \hat{d} \end{pmatrix}$$

and to the stationary equations for the working point according to

$$U_{C20}=\frac{2-D_0}{1-D_0}U_{10} \tag{52}$$

$$I_{L10}=\frac{U_{C20}}{R}\frac{1}{1-D_0} \quad . \tag{53}$$

Now one can Laplace transform the linearized differential equation according to (54)

$$\begin{bmatrix} s & \frac{1-D_0}{L_1} \\ -\frac{1}{C_2} & s+\frac{1}{RC_2} \end{bmatrix}\begin{pmatrix} I_{L1}(s) \\ U_{C2}(s) \end{pmatrix}=\begin{bmatrix} \frac{2-D_0}{L_1} & \frac{U_{C20}}{L_1} \\ 0 & -\frac{I_{L10}}{C_2} \end{bmatrix}\begin{pmatrix} U_1(s) \\ D(s) \end{pmatrix}$$

and can calculate transfer functions. The transfer functions between output voltage and duty cycle and the transfer function between current and duty cycle can now be written according to

$$\frac{U_{C2}(s)}{D(s)}=\frac{-\frac{I_{L10}}{C_2}s+\frac{U_{C20}(1-D_0)}{L_1C_2}}{s^2+s\frac{1}{RC_2}+\frac{1}{L_1C_2}} \tag{55}$$

$$\frac{I_{L1}(s)}{D(s)}=\frac{\frac{U_{C20}}{L_1}s+\left(\frac{U_{C20}}{L_1C_2R}+\frac{I_{L10}(1-D_0)}{L_1C_2}\right)}{s^2+s\frac{1}{RC_2}+\frac{1}{L_1C_2}} \quad . \tag{56}$$

As expected for a step-up converter, it is a non-minimum phase-system.

The transfer functions between the state-variables of the converter and the input voltage as disturbance lead to

$$\frac{U_{C2}(s)}{U_{L1}(s)}=\frac{(1-D_0)(2-D_0)}{L_1C_2}\frac{1}{s^2+s\frac{1}{RC_2}+\frac{1}{L_1C_2}} \tag{57}$$

$$\frac{I_{L1}(s)}{U_1(s)}=\frac{\frac{2-D_0}{L_1}s+\frac{2-D_0}{L_1C_2R}}{s^2+s\frac{1}{RC_2}+\frac{1}{L_1C_2}} \quad . \tag{58}$$

Fig. 9 shows the Bode diagrams between the output voltage and the duty cycle and the input voltage, respectively.

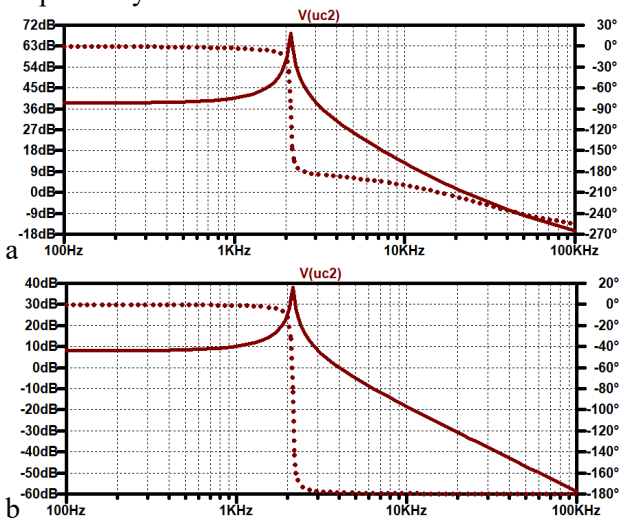

Fig. 9. Bode diagrams for the output voltage of the idealized converter: a. referred to the duty cycle, b. referred to the input voltage.

6 Simulations

All simulations are done with LT-Spice. The parameters are for the basic converter: L_1=47 µH, C_1=4.7 µF, C_2=47 µF, R=50 Ω, U_1=24 V, f=100 kHz, D_0=0.6; the additional inductor is L_2=0.5 µH; the parasitics are: R_{C1}=R_{C2}=10 mΩ, R_S=20 mΩ, R_D=67 mΩ, V_D=0.84 V, R_{L1}=4 mΩ.

6.1 Steady State

In section 2.1 the behavior of the converter is treated in the steady state mode. Here the important voltage and current signal forms are shown.

Fig. 9 depicts the voltages across the semi-conductors (all of them are reduced compared to the standard Boost converter) and in the last picture the output voltage, the input voltage and the gate signal are shown. The change of the voltage across C_1 can be seen at the voltage of D_2 and at the active switch S. The blocking voltage across the active switch increases because of the discharging of C_1 during the off-time of the transistor.

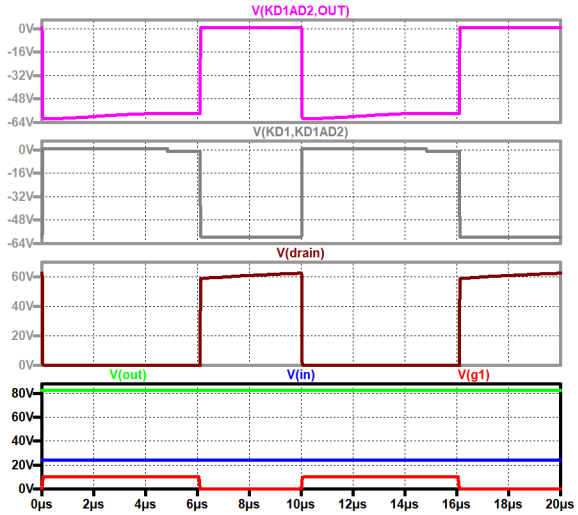

Fig. 9. Steady state, up to down: voltage across D_2, voltage across D_1, voltage across the active switch; output voltage (green), input voltage (blue), gate signal (red).

Fig. 10 shows the current through D_2, the current through D_1, and the current through the active switch S. In the last picture one can again see the output voltage, the input voltage, and the gate signal.

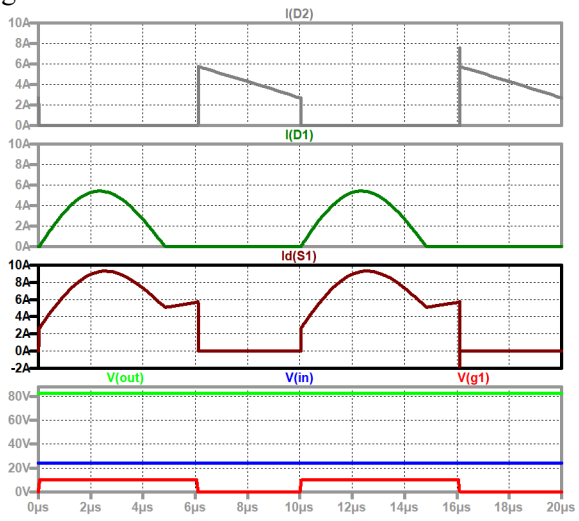

Fig. 10. Steady state, up to down: current through D_2, current through D_1, current through the active switch; output voltage (green), input voltage (blue), gate signal (red).

6.2 Dynamic Behavior

The dynamic behavior of the converter is analyzed with the help of the idealized state-space description (50). Compared to the circuit oriented simulation a pronounced ringing can be observed. The simulation is done by integrating the derivatives of the state variables (represented by currents) with a capacitor of the value 1 F. Therefore, the state variables are represented by voltages. Fig. 11 shows the start-up, an input voltage step, and a duty cycle step of the idealized converter.

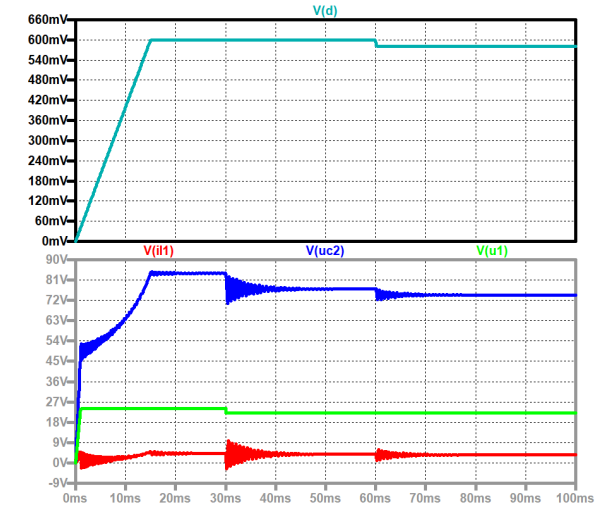

Fig. 11. Idealized model, up to down: duty cycle, output voltage (blue), input voltage (green), current through the converter coil L_1 (red).

Therefore, it is better to use a more realistic model by including the parasitic resistors. Calculation leads to (59)

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} = \begin{bmatrix} -\dfrac{R_{L1}+R_S\cdot d+(1-d)\cdot(R_{C1}+R_{D2}+R\,//\,R_{C2})}{L_1} & \dfrac{R\cdot(d-1)}{L_1(R+R_{C2})} \\ \dfrac{(1-d)\cdot R}{C_2(R+R_{C2})} & -\dfrac{1}{C_2(R+R_{C2})} \end{bmatrix} \cdot \begin{pmatrix} i_{L1} \\ u_{C2} \end{pmatrix} + \begin{bmatrix} \dfrac{2-d}{L_1} \\ 0 \end{bmatrix} \cdot (u_1) + \begin{pmatrix} \dfrac{(d-1)V_{D2}}{L_1} \\ 0 \end{pmatrix}.$$

This will be shown for the feedforward control in Fig. 12. The results are in good correspondence with the result achieved with the circuit-oriented simulation in Fig. 8 but achieved much faster.

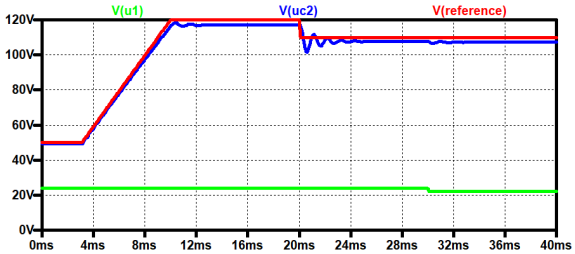

Fig. 12. Feedforward controlled converter, calculated with the improved model: reference value (red), output voltage (blue), input voltage (green).

With this refined model one can easily calculate the Bode diagrams. Compared to those which are calculated or simulated with the idealized model, the resonance is more damped. The plots are shown in Fig. 13 and Fig. 14.

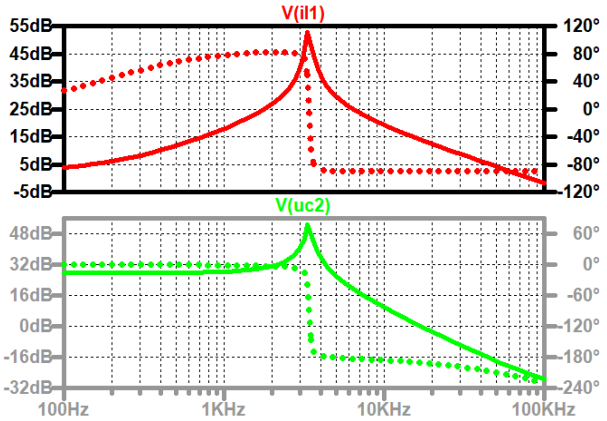

Fig. 13. Bode diagram: current through the converter coil (red) and output voltage (green) dependent on the duty cycle.

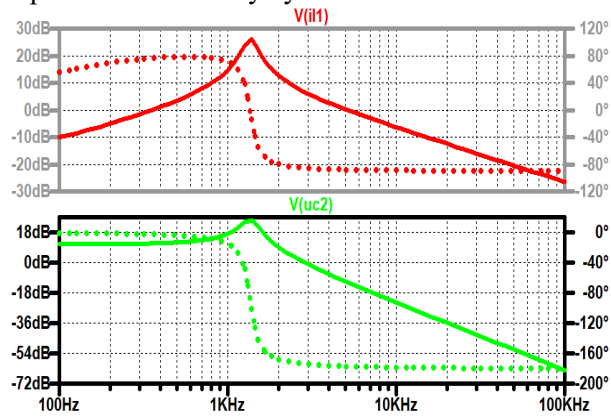

Fig. 14. Bode diagram: current through the converter coil (red) and output voltage (green) dependent on the input voltage.

When a feedforward control is not enough, the controller has to be designed for the plant with the control law included. This leads to the Bode plots (Fig. 15) from which now the controller has to be designed.

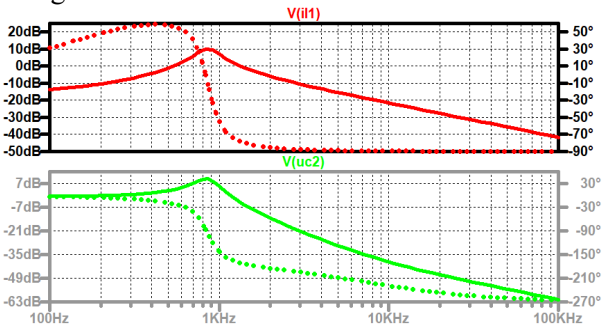

Fig. 15. Bode diagram for feedforward controlled converter: current of the converter coil (red) and output voltage (green) dependent on the duty cycle.

7 Conclusion

The here-described converter has several interesting aspects:

- High voltage transformation ratio
- Lower voltage stress across the semiconductors compared to other Boost converter topologies.

These aspects concern also the original positive output voltage super-lift Boost. The improved converter has some additional advantages:

- Improved efficiency
- Better EMC.

The converter is useful, when higher voltages are necessary from a positive input voltage e.g. renewable sources, fuel cells and to generate an intermediate circuit for a DC-to-AC converter. In spite of this that the converter has two capacitors and two coils, for the controller design it is only a second order non-phase-minimum system. For simple applications one can use only a simple control law to achieve a stable output voltage.

References:

[1] L. Colalongo, G. Duina, A. Richelli and Z. M. Kovacs-Vajna, A Modular Boost Converter with Low Switch Stress and High Conversion Ratio for Automotive Applications, *2018 International Conference of Electrical and Electronic Technologies for Automotive*, 2018, pp. 1-4.

[2] R. Marquez and M. A. Contreras-Ordaz, The Three-Terminal Converter Cell, Graphs, and Generation of DC-to-DC Converter Families, *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7725-7728, Aug. 2020.

[3] Fang Lin Luo and Hong Ye, Positive output super-lift converters, *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 105-113, Jan. 2003.

[4] M. Forouzesh, Y. P. Siwakoti, S. A. Gorji, F. Blaabjerg and B. Lehman, Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications, *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9143-9178, Dec. 2017.

[5] F. Zach: Power Electronics, in German: *Leistungselektronik*, Wien: Springer, 6th edition, 2022.

[6] N. Mohan, T. Undeland and W. Robbins: *Power Electronics, Converters, Applications and Design*, 3nd ed. New York: W. P. John Wiley & Sons, 2003.

[7] B. W. Williams, Generation and Analysis of Canonical Switching Cell DC-to-DC Converters, IEEE *Transactions on Industrial Electronics*, vol. 61, no. 1, pp. 329-346, Jan. 2014.

[8] Fang Lin Luo, Six self-lift DC-DC converters, voltage lift technique, *IEEE Transactions on Industrial Electronics*, vol. 48, no. 6, pp. 1268-1272, Dec. 2001.

[9] J. Li and J. Liu, Modeling and analysis of elementary positive output super-lift converter feeding constant power load, *IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1-5.

[10] Hammoda et al., Experimental verification and simulation of two stages positive output cascade boost converter super-lift DC/DC Luo-converter, 2017 4th IEEE International Conference on Engineering Technologies and Applied Sciences (ICETAS), 2017, pp. 1-7.

[11] G. Rohini and V. Jamuna, Dynamic analysis of positive output super lift converter, *IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2012, pp. 1-5.

[12] B. Faridpak, M. Farrokhifar, M. Nasiri, A. Alahyari and N. Sadoogi, Developing a super-lift luo-converter with integration of buck converters for electric vehicle applications, *CSEE Journal of Power and Energy Systems*, vol. 7, no. 4, pp. 811-820, July 2021.

[13] Fang Lin Luo and Hong Ye, Negative output super-lift converters, *IEEE Transactions on Power Electronics*, vol. 18, no. 5, pp. 1113-1121, Sept. 2003.