A Hybrid-Mode LDO Regulator with Fast Transient Response Performance for IoT applications

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Abstract: - A hybrid-mode low-drop out (LDO) voltage regulator with fast transient response performance for IoT applications is proposed in this paper. The proposed LDO regulator consist of two sections. First section is an analog regulator which includes a folded cascode operational amplifier to achieve good PSRR. Second section is current DAC and detectors whitch includes a cource current DAC, sink current DAC, undershoot detectors, and overshoot detectors. The current DAC and detectors are designed to obtain a low drop out and fast transient response. The proposed hybrid-mode LDO voltage regulator has been designed, simulated and layouted in Cadence using TSMC 90 nm CMOS technology. The input range of the LDO regulator is 1.2–2.0 V, and it can produces an output voltage of 1.2V. The LDO regulator achieves 58uA quiescent current, -69 PSRR @ 1 KHz noise frequency and an output voltage drop of around 60mV for a load current step of 100 mA. The final design occupies approximately 0.09 mm^2.

Key-Words: - Hybrid-mode LDO, PSRR, Regulator, Step Response, Transient, IoT.

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1. Introduction

The Internet of Things (IoT) is the interconnect of millions of independent devices to the network. These devices gather data on physical parameters and processes and report them to the network. Some independently, or through network control, supply outputs that control other devices and systems. There are a broad range of applications for IoT devices, including infrastructure, utilities, home automation, personal medical, vehicles, industry and more. However, the full range of potential applications has not been designed. The market for IoT devices will grow exponentially as more applications are developed. Many of these new IoT inventions will be implemented with a single system on a chip (SoC) to provide the highest level of integration and conservation of area. As numerous new companies enter into the market with their own ideas for IoT, many will begin to face the challenges of IoT SoC development.

The high-performance analog and mixed-signal blocks can be an area for customization and differentiation. Most IoT SoC designs are implemented in small geometry processes to take advantage of both power and die area savings. However, there are significant challenges of analog circuit design in small process linewidths due to transistor mismatch and leakage.

LDOs are frequently used for the purposes of supplying the many different voltage rails required on the SoC, and for isolating the internal SoC circuitry from external sources of noise on the circuit board power supply rails [1-7]. This makes LDO regulator design more challenging, particularly because power management applications are also

getting more complex. A basic digital LDO, shown in Fig. 1, includes a programmable size power transistor and a data converter that translates the voltage difference between the output voltage and a reference voltage to a digital code. The number of ON legs in the power transistor is controlled by the digital code. Since the source to gate voltage of the power transistor is large and equivalent to the supply voltage, digital regulators are smaller than analog regulators. Furthermore, because the power transistor is not in saturation, digital regulators do not lose stability when the load current fluctuates, and they can be easily scaled down for advanced technology nodes. However, because the current in the power transistor can only change in discrete steps, digital regulators have larger voltage ripples than analog regulators. In addition, the power supply rejection ratio (PSRR) performance of digital regulators is weak. This is due to the fact that the power transistor is in the linear zone, which means that noise from the power source is not effectively isolated.

In the past few years, there has been significant research to improve the performance of LDO regulators due to modern stringent applications' specifications and cost reduction requirements [8-12]. In [7], a digital LDO regulator is proposed, where both hill-climbing and binary search algorithms are utilized to minimize output voltage ripple and the quiescent current during steady state. Hysteresis mode control and freeze mode control features are also incorporated into the LDO to help improve performance. In [11], a mixed-mode LDO regulator is proposed. A small digital power transistor is added to help improve the regulation and increase the maximum supported load current. A hysteretic current comparator is used to detect the load current. If a high load current is detected, the digital power transistor is enabled and supplies a large current because the source to gate voltage is equal to the supply voltage. This technique helps achieve a high load current capability at reduced area. In [12], a digital LDO regulator that has a 200mA load current capacity is proposed. The circuit does fast coarse tuning utilizing a flash Analogue-to-Digital Converter (ADC) to alter the size of a large PMOS power transistor. The flash ADC reference voltages are adjusted to minimize the error amount with respect to the regulator voltage. Further, the proposed circuit does fine tuning utilizing a 20-bit shift register to address small changes in load current. A digital controller is used to insure proper interaction between the coarse tuning and the fine-tuning operations. In [13], A fully integrated 1.2V LDO regulator that has a 100mA load current is proposed. The circuit utilizing two feedback mechanisms. The first feedback mechanism is the conventional analog regulation that includes an operational amplifier. The second feedback mechanism is based on digitizing any fast change in the output voltage using multiple comparators and subsequently enabling either an NMOS based or a PMOS based current Digital -to-Analog Converter (DAC). However, it provides 3.5us for setting time. In this work, a new hybrid-mode LDO that delivers high PSRR performance, low dorp out, and fast transient response is proposed. The LDO operates without the need of an external capacitor or clocks to control the two feedback techniques.

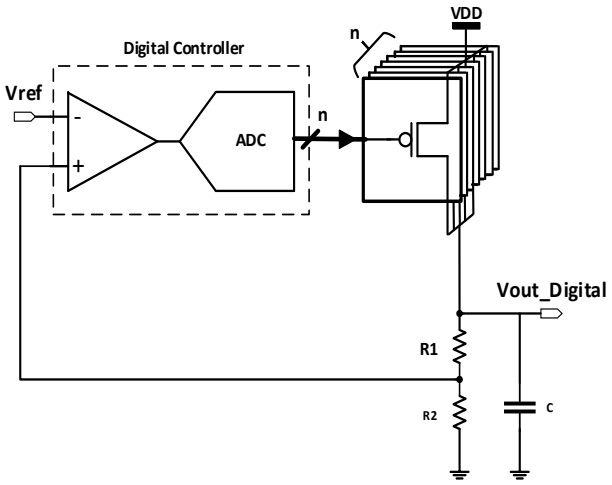

Fig. 1: Basic digital LDO

2. Circuit architecture

The block diagram of the proposed hybrid-mode low-drop out LDO is shown in Fig .2 which consists of an analog regulator, an undershoot detector with hysteresis, an overshoot detector with hysteresis, and a master comparator with hysteresis.

2.1. Analog regualtor LDO section

In this section, we assume that all current sources and detectors in Fig. 2 aren't available. In other words, only the analog regulator is available and the LDO output voltage is $Vout\_Analog$(t). Further, we assume that the bandwidth of the folded cascode amplifier is insufficient to address any rapid fluctuations in load current. The equations below derive the LDO output voltage, $Vout\_Analog$ (t), as a function of time.

$$V_{out_{Analog}}(t) = I_R(t)R\,; \qquad I_R(t) = I_{PMOS}(t) - I_{load}(t) - I_c(t)$$

$$V_{out_{Analog}}(t) = (I_{PMOS}(t) - I_{load}(t) - I_c(t))R\,;$$

$$I_c(t) = C\frac{\partial V_{out_{Anlog}}(t)}{\partial t}$$

$$V_{out_{Analog}}(t) = (I_{PMOS}(t) - I_{load}(t) - C\frac{\partial V_{out_{Anlog}}(t)}{\partial t})R$$

It is assumed that the load current $I_{load}(t)$ changes from 1mA to 100mA in 10nsec. In a 10nsec window frame, the load current can be modeled as linear function with slope as shown in equation (1).

$$I_{load}(t) = \alpha t + \beta \qquad (1)$$

$\alpha = \frac{(100m-1m)A}{10n} = 9.9 * 10^6\left(\frac{A}{Sec}\right)$, and $\beta = 1mA$ whitch results into $I_{load}(t) = 9.9 * 10^6 t + 1mA$

Further, the charge consumed by the load during the sharp rise in current is modeled by equation (2).

$$Q_{Analog\_load} = \int_0^{10n} l_{load}(t)dt = \int_0^{10n}(\alpha t + \beta)dt \qquad (2)$$

This results into a total charge of

$\int_0^{10n}(9.9 * 10^6 t + 1mA)dt$ 560 $pCouloumbs = Q_{Analog\_load}$.

Since the response time of the folded cascode operational amplifier is much slower than 10nsec, the PMOS current $I_{PMOS}(t)$ can be assumed to be a constant value in a 10nsec window frame,

$$I_{PMOS}(t) \Longrightarrow I_{PMOS}.$$

$$V_{out\_Analog}(t) = (I_{PMOS}(t) - (\alpha t + \beta) - C\frac{\partial V_{out\_Analog}(t)}{\partial t})R$$

Rearranging the first order differential equation:

$\frac{\partial V_{out\_Analog}(t)}{\partial t} + \frac{1}{RC}V_{out\_Analog}(t) = -\frac{\alpha}{C}t - \frac{\beta}{C} + \frac{I_{PMOS}}{C}$;

$V_{out\_Analog}(0) = 1.2$. Solving the equation results in

$$V_{natural}(t) = K_1 e^{-t\frac{1}{RC}}\,;$$

$$K_1 = 1.2 - (\alpha R^2 C - \beta R + I_{PMOS}R)$$

$$V_{forced}(t) = K_2 t + K_3\,;$$

$$K_2 = -\alpha tR,\ K_3 = \alpha R^2 C - \beta R + I_{PMOS}R$$

$$V_{out\_Analog}(t) = K_1 e^{-t\frac{1}{RC}} + K_2 t + K_3\,;$$

Assuming the following values:

$$R = 500K\Omega, C = 1nF, \alpha = 9.9 * 10^6\left(\frac{A}{Sec}\right), \beta = 1mA,$$

$I_{PMOS} = 1mA + \frac{1.2V}{500k\Omega} = 1.0024mA$, the K_1, K_2 and K_3 coefficients can be calculated:

$K_1 = -2.475 * 10^9, K_2 = -4.95 * 10^{12}$ and $K_3 = +2.475 * 10^9 + 1.2$.

The analog LDO output voltage can be predicted by equation (3).

$$V_{out\_Analog}(t) = (-2.475 * 10^9 e^{-2000t} - 4.95 * 10^{12}t + 2.475 * 10^9 + 1.2)V \qquad (3)$$

From Fig. 3, it is evident that drops to 0.7V in 10nsec when the load current changes $V_{out\_Analog}(t)$ from 1mA to 100mA, which is very significant

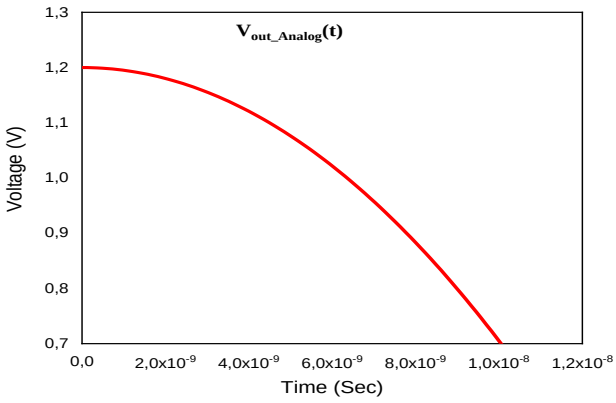

Fig. 2: Analog LDO output voltage response to 1mA to 100mA load current change in 10nsec

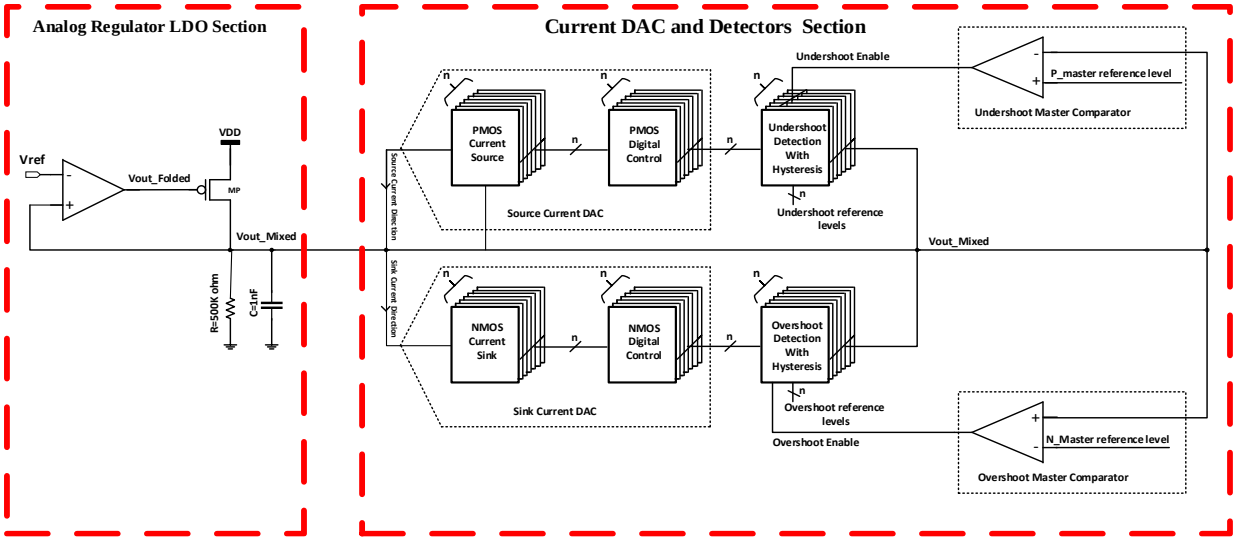

Fig. 3. Block diagram of proposed hybird-mode LDO

2.2. Current DAC and detectors section

In this section, we assume that all current sources and detectors in Fig. 2 are present. A new model for the LDO output voltage will be attempted by taking the added DAC current into account and altering equation (1) accordingly. The DAC current is a sum of the current sources that are enabled depending on the output voltage $V_{out\_mixed}(t)$, as illustrated in Fig. 3. For example, if V_{out_mixed} drops, the Source-Current DAC is enabled and will supply more current reducing the effect of the sharp increase in $I_{load}(t)$. The effective load current seen by the LDO can be modeled of as the difference between $I_{load}(t) - I_{DAC} = I_{load\_eff}$.

$$I_{DAC} = \begin{cases} I_{n1} + I_{n2} + I_{n3} + I_{n4}, & Vout\_Mixed > Vref\_n4 \\ I_{n1} + I_{n2} + I_{n3}, & Vref\_n3 < Vout\_Mixed < Vref\_n4 \\ I_{n1} + I_{n2}, & Vref\_n2 < Vout\_Mixed < Vref\_n3 \\ I_{n1}, & Vref\_n1 < Vout\_Mixed < Vref\_n2 \\ 0, & Vref\_n1 > Vout\_Mixed > Vref\_p1 \\ I_{p1}, & Vref\_p1 > Vout\_Mixed > Vref\_p2 \\ I_{p1} + I_{p2}, & Vref\_p2 > Vout\_Mixed > Vref\_p3 \\ I_{p1} + I_{p2} + I_{p3}, & Vref\_p3 > Vout\_Mixed > Vref\_p4 \\ I_{p1} + I_{p2} + I_{p3} + I_{p4}, & Vout\_Mixed > Vref\_p4 \end{cases}$$

$$I_{load\_eff} = \begin{cases} \alpha t + \beta & , V_{ref\_p1} \le V_{out_{mixed}}(t) \le V_{ref\_n1} \\ \alpha t + \beta - I_{1p} & , V_{ref\_p2} \le V_{out_{mixed}}(t) \le V_{ref\_p1} \\ \alpha t + \beta - I_{1p} - I_{2p} & , V_{ref\_p3} \le V_{out_{mixed}}(t) \le V_{ref\_p2} \\ \alpha t + \beta - I_{1p} - I_{2p} - I_{3p} & , V_{ref\_p4} \le V_{out_{mixed}}(t) \le V_{ref\_p3} \\ \alpha t + \beta - I_{1p} - I_{2p} - I_{3p} - I_{4p} & , V_{out_{mixed}}(t) \le V_{ref\_n1} \end{cases}$$

In Fig. 4, t_1, t_2, t_3 and t_4 represent the times at which the $V_{out\_mixed}(t)$ crosses $V_{ref\_p1}, V_{ref\_p2}, V_{ref\_p3}$ and V_{ref_p4} voltage references, respectively.

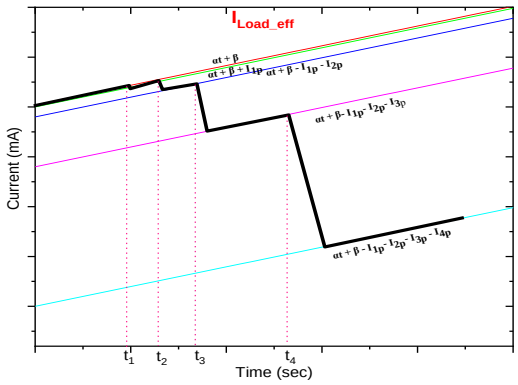

Fig. 4: Plot of source-currents (Ip1, Ip2, Ip3, Ip4) vs. time

The following currents are used as source-currents in the proposed LDO: $I_{1p} = 1mA$, $I_{2p} = 5mA$, $I_{3p} = 25mA$ and $I_{4p} = 70mA$. For the following analysis, it is assumed that the load current changes from 1mA to 100mA in 10nsec, and the source currents are enabled at: $t_1 = 5.6\,nsec$, $t_2 = 5.7\,nsec$, $t_3 = 5.94\,nsec$ and $t_4 = 6.38\,nsec$. To quantify the impact of the Source DAC current that offsets the sharp change in load current, the charge drawn from the LDO can be calculated as follows:

$$Q_{Mixed} = \int_0^{10n} I_{load_{eff}} dt = \int_0^{t_1} (\alpha t + \beta) dt + \int_{t_1}^{t_2} (\alpha t + \beta - I_{p1}) dt + \int_{t_2}^{t_3} (\alpha t + \beta - I_{p1} - I_{p2}) dt + \int_{t_3}^{t_4} (\alpha t + \beta - I_{p1} - I_{p2} - I_{p3}) dt + \int_{t_4}^{10n} (\alpha t + \beta - I_{p1} - I_{p2} - I_{p3} - I_{p4}) dt$$

$Q_{Mixed} = 124pCoulombs$, $Q_{diff} = Q_{analog\_load} - Q_{Mixed} = 436p\ Couloms$, which is the amount of charge supplied by the Source-DAC during the 10nsec. To approximate the voltage drop in $Vout\_mixed$ the charge drawn due the Source-DAC current, is modeled as 38mA constant current source active Q_{diff} during the 10nsec opposite to $I_{load}(t)$. As a result, equations (1) can be altered as shown in equation (4).

$$I_{load\_eff} = \alpha t + \beta_{mixed} = I_{load\_eff} = \alpha t + \beta - 38mA \quad (4)$$

$\beta_{mixed} = \beta - 38mA = 1mA - 38mA = -37mA$. Recalculating the differential equation in the mixedmode case assuming: $R = 500K\Omega, C = 1nF, \alpha = 9.9 * 10^6, \beta_{mixed} = -37mA,\ I_{PMOS} = 1mA + \frac{1.2V}{500K\Omega}$, the K_1, K_2 and K_3 coefficients are : $K_1 = -2.47502 * 10^9$, $K_2 = -4.95 * 10^{12}$, $K_3 = 2.47502 * 10^9 + 1.2$. This leads to equation (5) for the LDO regulator voltage. As shown in Fig. 5, at the end of the 10nsec window, $V_{out\_mixed}(t)$ drops to 1.08V whereas $V_{out\_Analog}(t)$ drops to 0.7V.

$$V_{out\_mixed}(t) = \left(-2.47502 * 10^9 e^{-2000t} - 4.95 * 10^{12} t + 2.47502 * 10^9 + 1.2\right) V \quad (5)$$

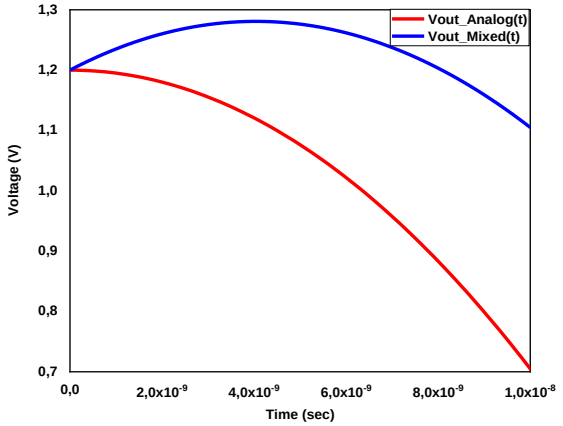

Fig. 5: Response of $V_{out\_mixed}(t)$ & $V_{out\_Analog}(t)$ as load current changes from 1mA to 100mA

3. Detailed circuits' description

This section provides detailed schematics of the proposed LDO. The LDO uses a 1nF bypass capacitance which can be integrated on-chip. It has two feedback loops. The first the loop is the conventional analog loop which provides good PSRR and minimal ripple during steady state operation. The second feedback loop is activated when the LDO output voltage, $V_{out\_Mixed}(t)$ drops below P_master_reference_voltage or increases above the N_master_reference_voltage. The outputs of the master comparators, which consume minimal current, enable either the undershoot detectors or the overshoot detectors. These detectors enable the appropriate number of current sources in the Source Current DAC or the Sink Current DAC. Both DACs cannot be ON simultaneously, because one is enabled during undershoot and the other is enabled during overshoot. All four overshoot detectors and four undershoot detectors have built in hysteresis to achieve a stable operation. Fig. 6 and Fig. 7 detail the circuit implementation of the Source Current DAC and Sink Current DAC, respectively. As shown in Fig. 6 and Fig. 7, the outputs of the detectors control how much current is sourced from the PMOS current sources or sunk from the NMOS current sources. The analog feedback loop will eventually bring the LDO output voltage to the desired value which is greater than P_master_reference_voltage,1.2V – 20mV, and less than N_master_reference_voltage,1.2V + 20mV. This turns off all detectors and both DACs which saves power in steady state operation and keeps all the advantages an analog LDO has like good PSRR and minimum ripple.

Fig. 8 is the schematic of the error amplifier. A folded-cascode topology was picked as it has one dominant pole and can be made stable without difficulty. All detectors, which are based on [13], are shown in Fig. 9, Fig. 10, and Fig. 11. The hysteresis in the detectors was built to be approximately 110mV as will be shown in the results section. The overshoot and undershoot detectors are significantly similar. There is a slight difference in the device that determines the output of the power-down state. In the case of the undershoot detectors, the output voltage during the power-down state is low which disables the corresponding PMOS current source shown in Fig. 6. However, in the case of the overshoot detectors, the output voltage is high during the power-down state which disables the corresponding NMOS current source shown in Fig. 7. The master overshoot and master undershoot comparators are also similar to the regular detectors. But they do consume far less current as they are ON all the time and are never power-down.

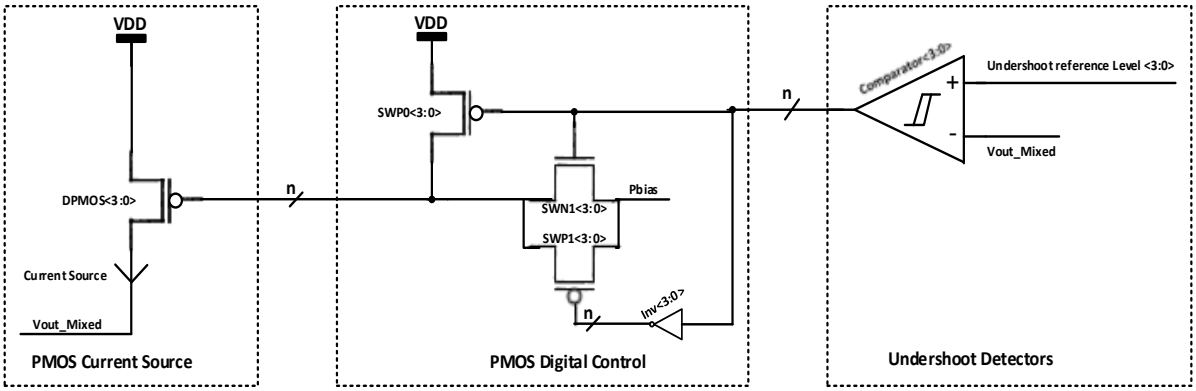

Fig. 6 : Detailed architecture of the undershoot correction

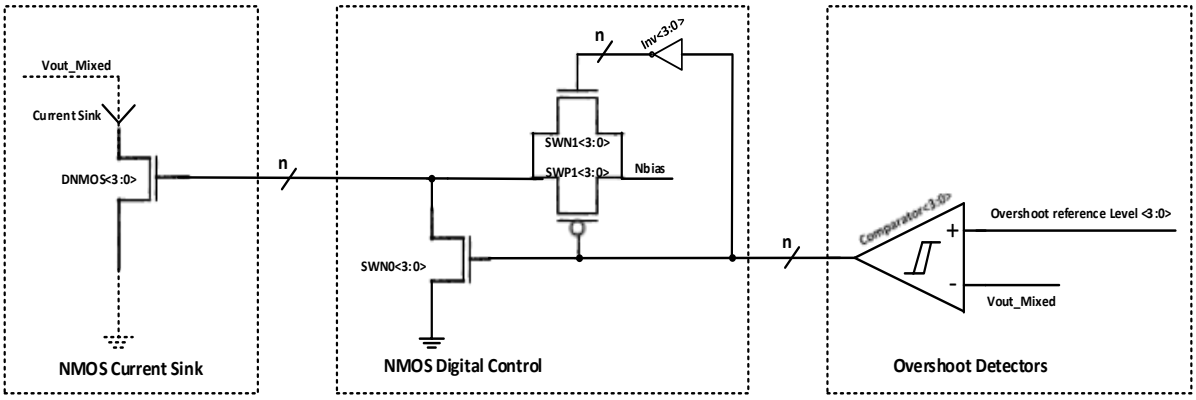

Fig. 7: Detailed architecture of the overshoot correction

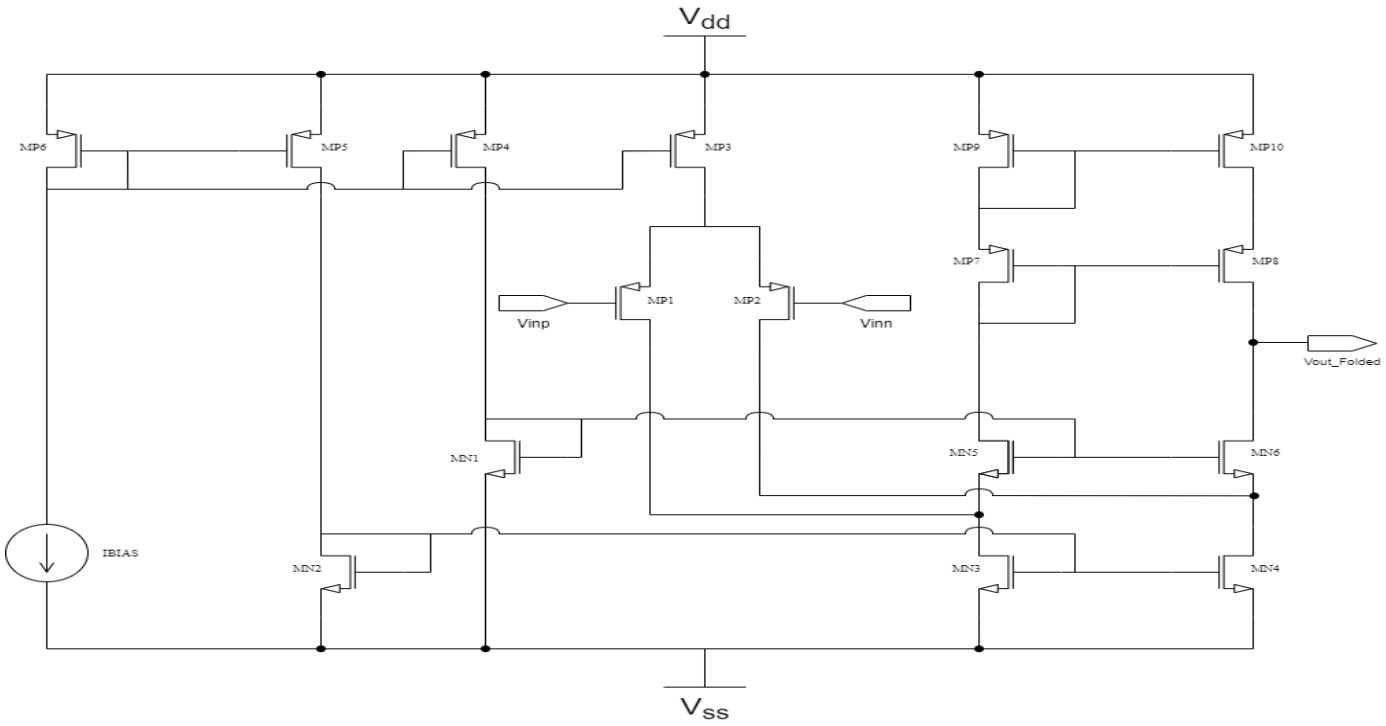

Fig. 8: Folded-cascode schematic

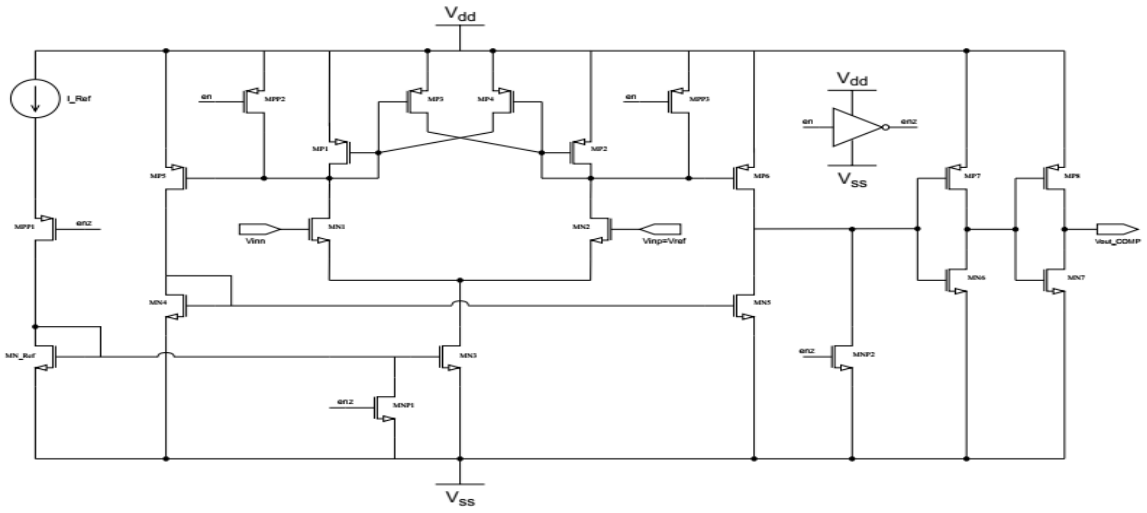

Fig. 9: Undershoot detector with hysteresis schematic

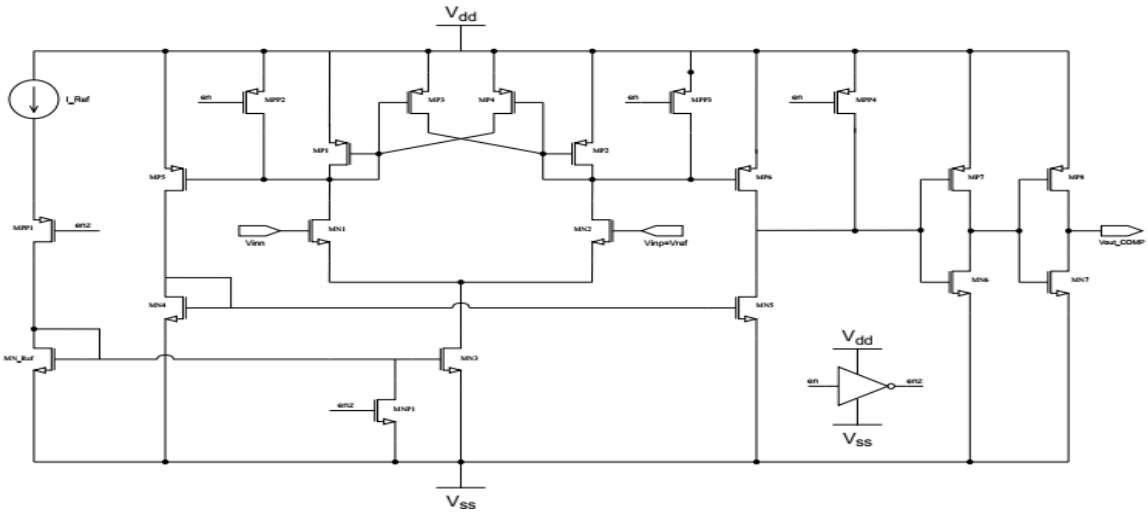

Fig. 10: Overshoot detector with hysteresis schematic

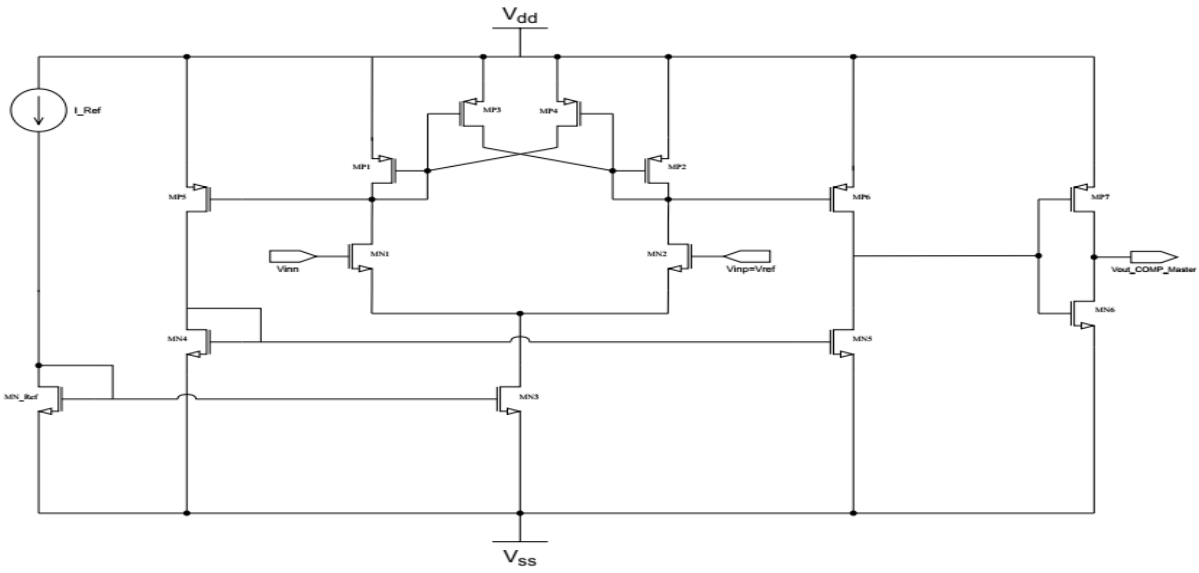

Fig. 11: Master comparator with hysteresis schematic

4. Simulations results

The proposed mixed-mode LDO was simulated using Cadence virtuoso design software and 900nm CMOS device models. The nominal output voltage is 1.2V, and the input voltage range is 1.6V-2.0V. The simulations included block level simulations for the folded-cascode operational amplifier and the overshoot/undershoot detectors. Top level simulations, where sharp increases/decreases in load current were modeled, were also run. Further, PVT simulations were run to demonstrate the robustness of the design.

4.1.Folded-cascode open loop gain

The operational amplifier open loop gain was simulated and is shown in Fig. 12. The gain-bandwidth product of the folded-cascode directly impact the analog feedback loop response time.

4.2.PSRR (Power Supply Rejection Ratio)

Fig. 13 shows the Power Supply Rejection Ratio (PSRR) of the proposed LDO. It is determined by the analog feedback loop only. This is a significant advantage over digital-based LDOs.

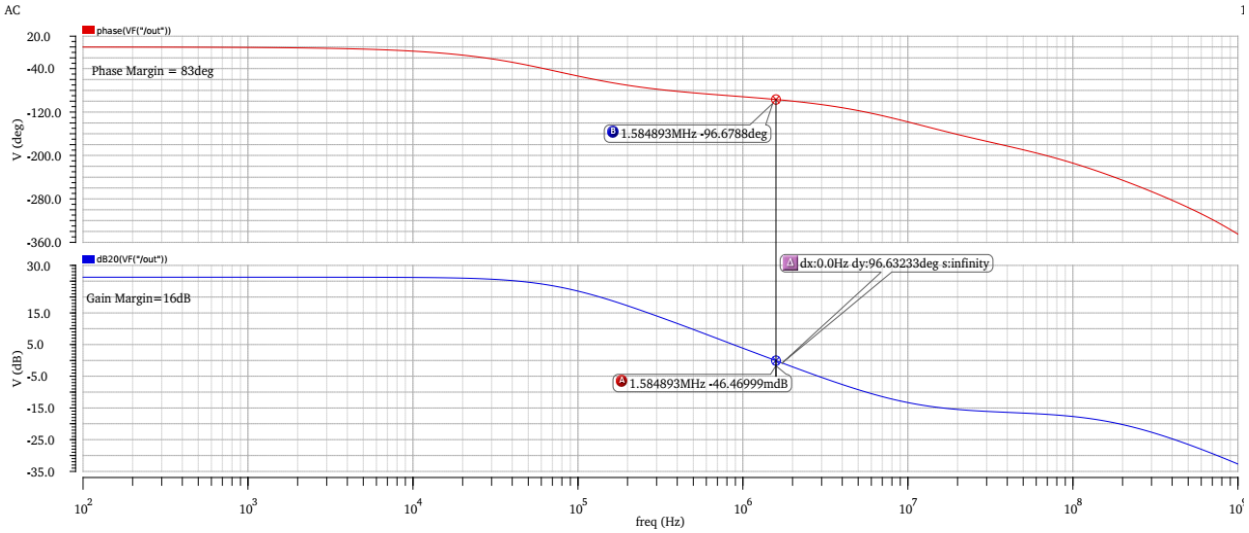

Fig. 12: Folded-cascode open loop gain

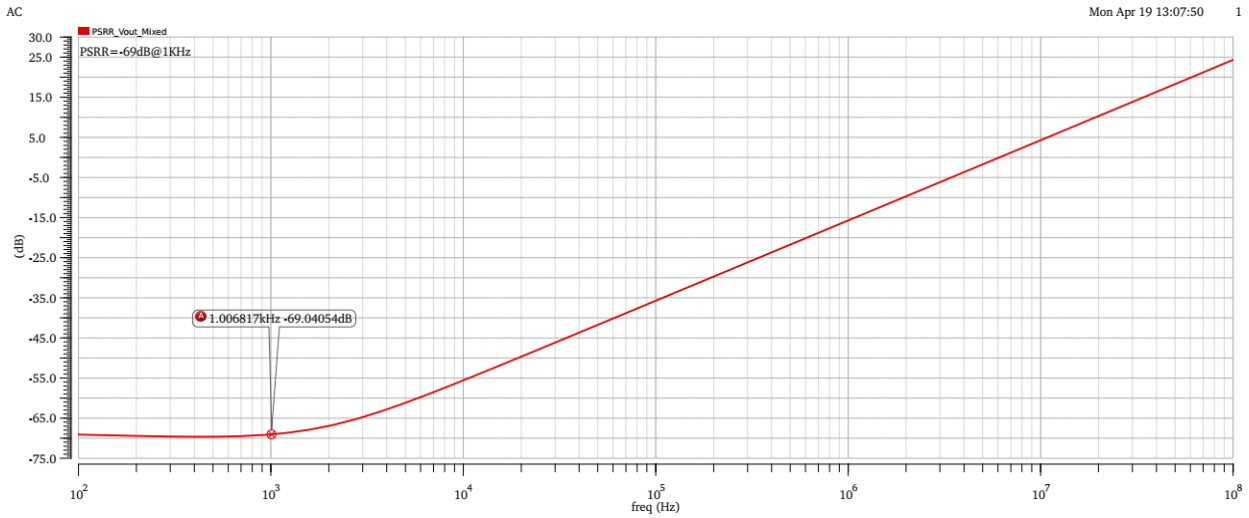

Fig. 13: LDO power supply rejection ratio (PSRR)

4.3.Differential comparator simulations (Overshoot/Undershoot Detectors)

The comparator with hysteresis circuit in Fig. 9, which is used for the overshoot and undershoot detectors, has been verified as shown in Fig. 14. It is evident that there is a 110mV built-in hysteresis. Such hysteresis inures stable operation and minimizes ripple of the LDO output when sharp changes in load current take place. The reference voltages for all detectors are detailed in Table 1.

4.4.Top level LDO simulations

Extensive top-level simulations were run to verify the operations of the mixed-mode LDO. These simulations take into account both feedback loops: the analog loop and the DACs-based loop. All simulations show how the proposed LDO responds to sharp increases/decreases in load current. Fig. 15 compares the response of the proposed mixed-mode LDO to the analog-based LDO for a nominal voltage of 1.2V. The load current increases from 1mA to 100mA in 10nsec. Then, it decreases back to 1mA in 10nsec. It is evident that the proposed mixed-mode LDO has a more graceful response to the sharp increase/decrease in load current. While the output of the analog-based LDO completely collapses to ground or hits the supply voltage, the mixed-mode LDO output changes by ~ 200mV only and settles to steady state in 3.5usec. Once, steady state is achieved, the analog feedback loop in the mixed-mode LDO fully determines the LDO output, and both DACs and the level detectors that control DACs are turned off completely. Fig. 16 shows the results of the Load transient response when load current steps between 1 mA and 100 mA at VDD=1.8 V. The maximum variations in transient output namely undershoot and overshoot of the proposed LDO are 60 mv and 58 mv respectively, whereas the recovery times are 1.5 us and 1.2 us, respectively. The line transient response when supply voltage changes between 1.2 V and 2 V in 1µs have also been provided in Fig. 17. The result shows that the maximum voltage spike is 177 mV. Fig. 18 shows how the proposed LDO responds to different steps in load current: 25mA, 50mA, 75mA and 100mA. The output voltage sharp increase is proportional to the maximum value of the load current. In all cases, the steady state output voltage of the LDO remains at 1.2V without any presence of ripples. Fig. 19 show performance at extreme PVT corners: slow process and hot temperature in addition to fast Process and cold temperature.

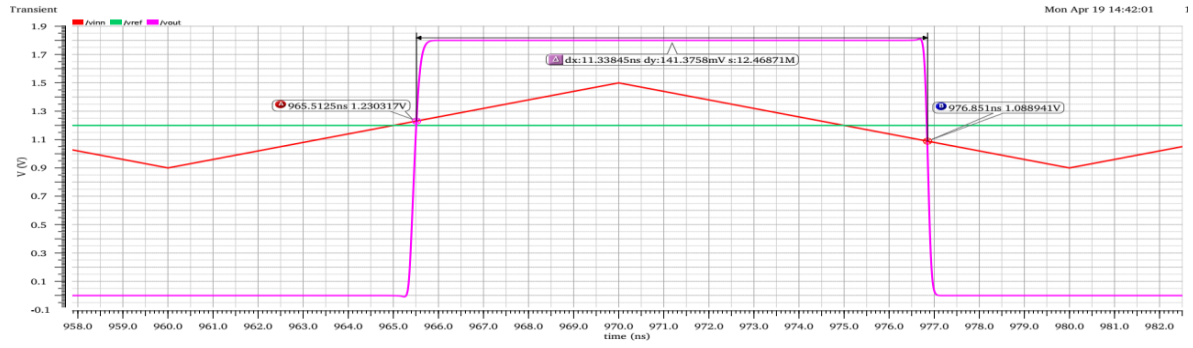

Fig. 14: Comparator transient simulations

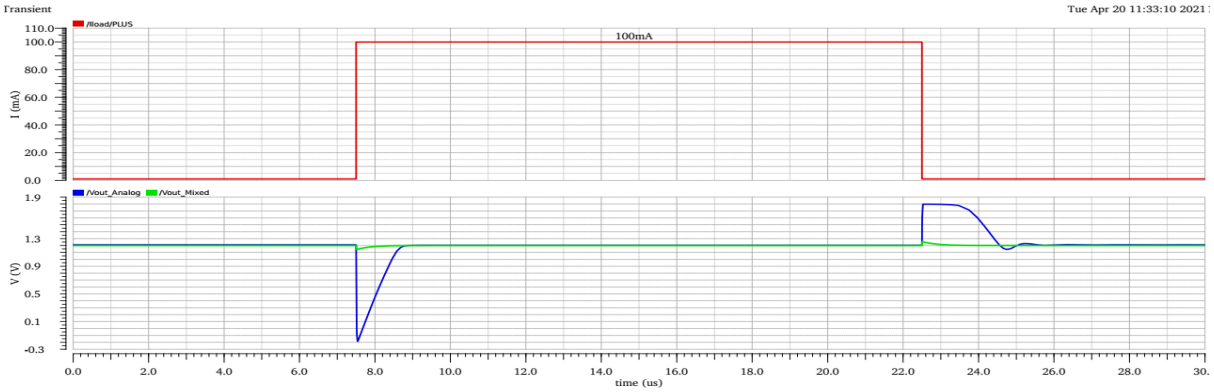

Fig. 15: Proposed hybrid-mode LDO vs. Analog LDO during sharp changes in load current

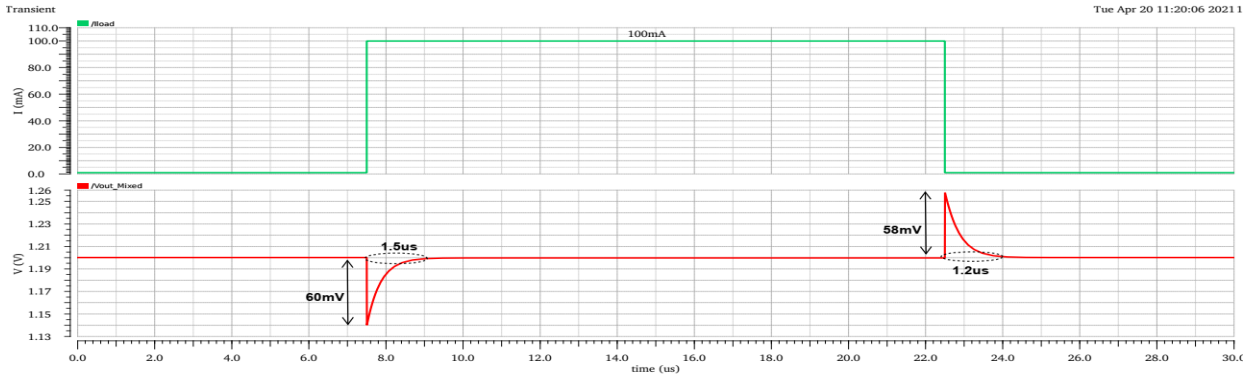

Fig. 16: Load transient response when load current steps between 1 mA and 100 mA

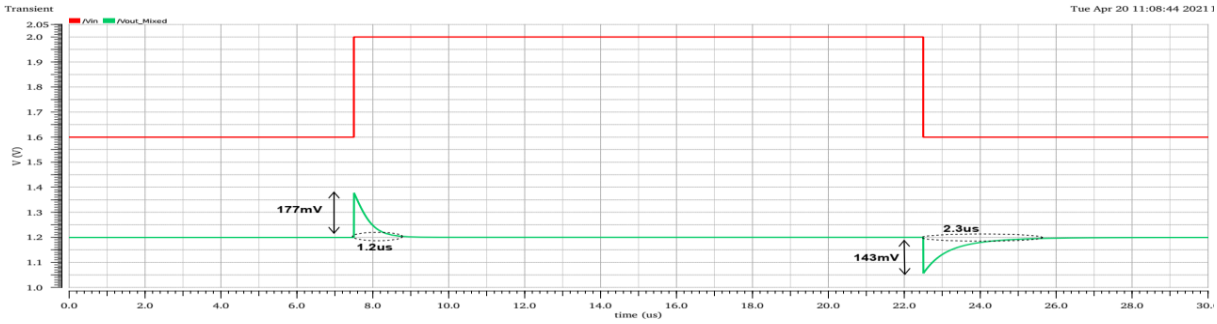

Fig. 17: Line transient response when supply voltage steps between 1.6 V and 2.0 V

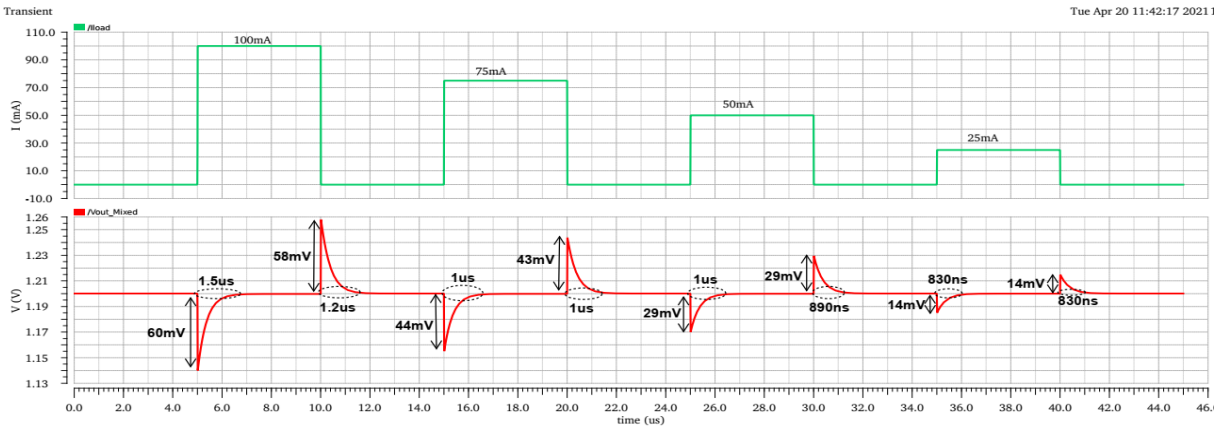

Fig. 18: Hybrid-mode LDO response to sharp changes in load current

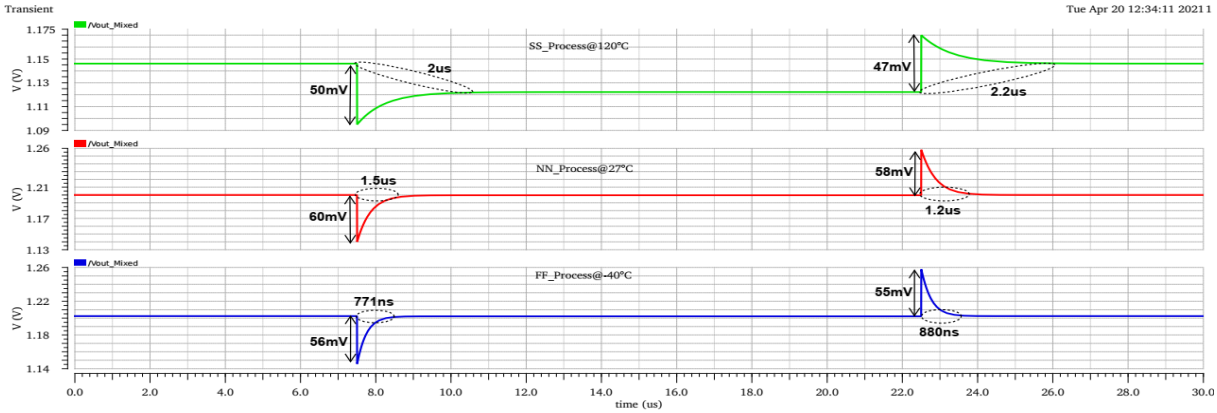

Fig. 19: Hybrid-mode LDO response at fast corner@ -40C, nominal corner@27C, and solwer corner@120C for a 100mA step load current

4.5.LDO quiescent current

The total quiescent current is determined by three blocks: the operational amplifier, the undershoot master comparator and the overshoot master comparator. These three blocks are ON in steady state operation and are not turned off. Fig. 20 show Monte Carlo simulation quiescent current of the proposed regulator LDO. The total quiescent current is 58,26uA

4.6.Layout

The layout for the proposed a fully integrated hybrid-mode low-drop out voltage regulator with fast transient response performance for IoT applications is shown in Fig. 21. The output transistors occupy the majority of the chip area. All devices or circuits prone to produce electromagnetic interference or susceptible to interference are enclosed with double layer guard rings. The layout is done by respecting following items; design rules (DRM, MRC and Density) and designer constraints information (constraint manager, matchCat, text…). The total chip area of the proposed circuit in TSMC 90 nm technology is 245,5um x 366,6um, occupying a total area of 0.09mm2 including pads.

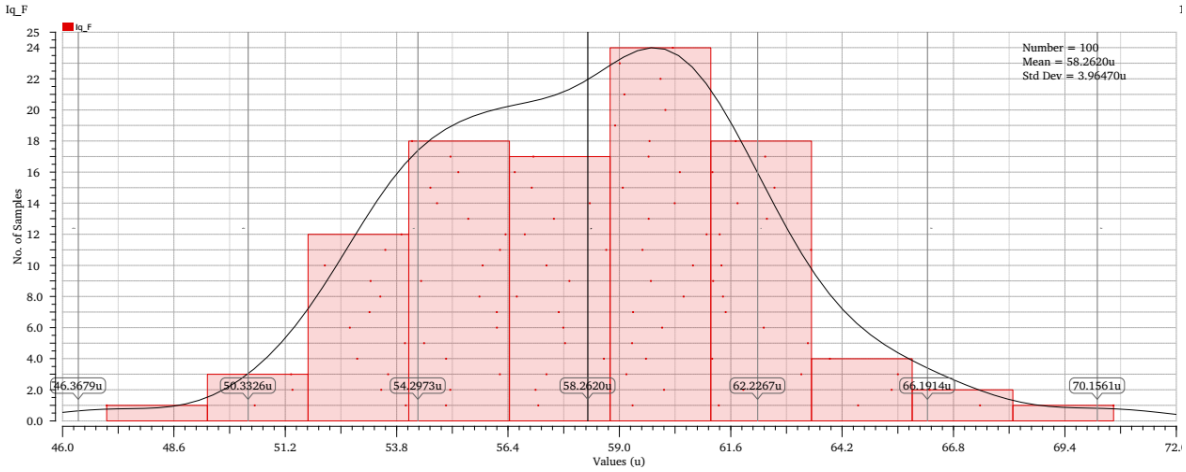

Fig. 20: Monte Carlo simulation quiescent current of the proposed regulator LDO

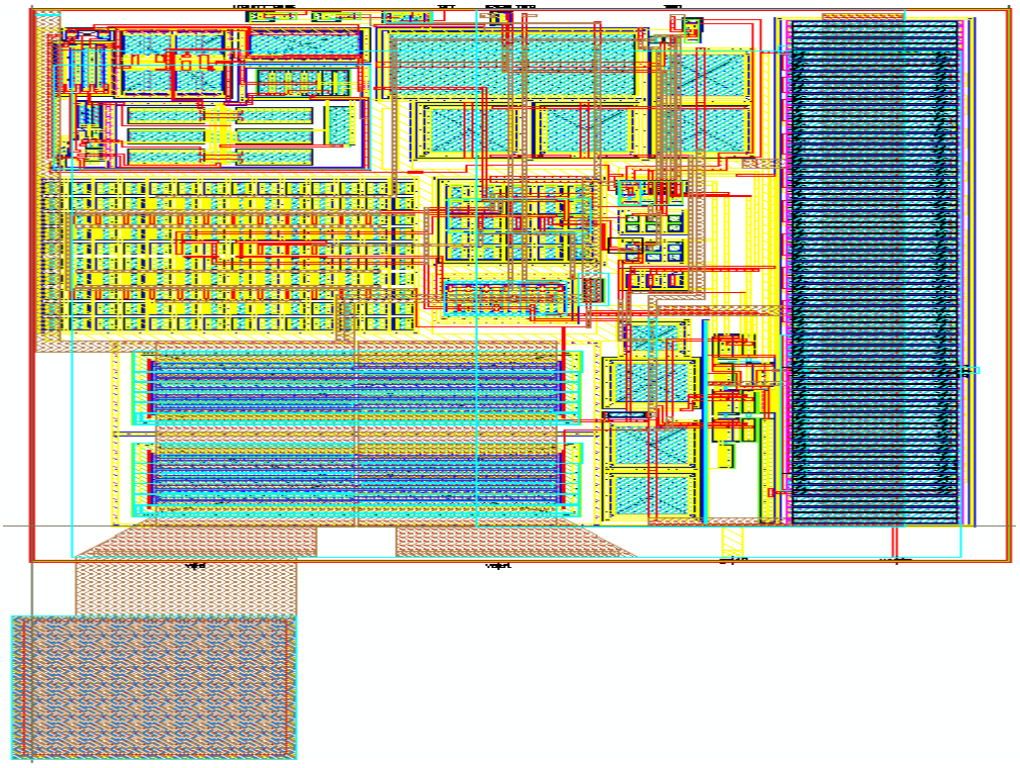

Fig. 21: Layout of the proposed a fully integrated hybrid-mode

5. Conclusion

This work presented an integrated hybrid-mode LDO regulator that achieves fast transient response performance. The LDO utilizes two feedback mechanisms. The first feedback mechanism is the conventional analog regulation that includes an operational amplifier. It controls the output voltage in steady state where small changes in load current take place. The second feedback mechanism kicks in only when large and sharp changes in load current occur. It utilizes high speed current DACs that provide current in opposite polarity to the sharp change of the load current which reduces its impact. As a result, addressing sharp changes in current is not limited by the gain-bandwidth product of the error amplifier.

Reference	[11] 2018	[14] 2019	[15]* 2019	[16]* 2017	[9] 2020	This work* 2021
LDO Type	Mixed-Mode	Digital	Analog	Analog	Hybird	Hybrid-Mode
Technology	180nm	65nm	180nm	180nm	40nm	90nm
Input Voltage (V)	1.2	1	1.1	1.4	1.25-1.4	1.6-2.0
Output Voltage (V)	1	0.9	1	1.2	1.1-1.25	1.2
PSRR @ 1KHz (dB)	-32	-	-58	-65	-36	-69
Quiescent Current (uA)	176	753	20	31.6	300	58
Delta Vout @ Load_Step/Tedge	125mV @ 150mA/3uS	260mV @ 35mA/1nS	552mV @ 100mA/0.2uS	42mV @ 100mA/0.3uS	71mV @ 240mA	60mV @ 100mA/10nS
Settling Time @ Load_Step/Tedge	-	3usec @ 35mA/1nS	1.3usec @ 100mA/0.2uS	1.3usec @ 100mA/0.3uS	0.52usec	3.5usec @ 100mA/1.5uS
Bypass Capacitor Value (nF)	0.1	0	0.1	0.1	20	1
Clock Needed	No	Yes	No	No	No	No
Load Regulation mV/mA	0.17	-	0.001	0.0027	N-A	0.014
Ripple @ Steady State	No	Yes	No	No	No	No
Area(mm^2)	-	-	-	-	0.056	0.09

*Simulations Results

Table 1. Performance comparison with previous work

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