# Nano-Power Low-Dropout Voltage Regulator Circuit in 90-nm CMOS Technology for RF SoC Applications

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*Abstract:* - This paper presents a nano-power Low Drop-Out (LDO) voltage regulator circuit for Radio-Frequency System-on-Chip (RF SoC) applications, this LDO is designed for a smaller dimension due to CMOS technology and in the weak inversion region, can thus be used to minimize power loss of LDO regulator without transient-response degradation. The proposed structure its low power dissipation make it ideal for RF system-on-chip applications that require low power dissipation under different loading conditions. In order to optimize performance for LDO, the proposed amplifier helps to minimize power of LDO regulators without using any on-chip and off-chip compensation capacitors. The output spot noise at 100Hz and 1 kHz are 200nV/sqrt (Hz) and 6nV/sqrt (Hz), respectively. The active area of the circuit is 850 $\mu m^2$. The regulator operates with supply voltages from 1.2V to 2V.

*Key-Words:* - Low-dropout linear regulators; CMOS analog integrated circuits; Weak inversion region; Power consumption; Negative and Positive feedback; Noise

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## 1 Introduction

Today, the Low-dropout linear regulators (LDOs) are present in all mobile electronics powered by a battery [1]. It is used to regulate the supplies ripples to provide a clean voltage source for the noise-sensitive analog/radio-frequency (RF) blocks and low power dissipation. Nowadays, voltage regulation circuits have to be integrated onto RF systems on chip (SoC) in order to reduce the static power dissipation, cost, area ... and complexity of RF transmitters/receivers [3].

In particular, its cutting edge product is focused on linking, processing and sharing stable voltage between devices with ultralow power consumption (Nano-Power) in hostile environments through Mobile Phone, PC, Tablet and other devices.

The low power consumption is a very critical requirement to extend the battery life. Thus, low voltage and low quiescent current are the most desirable parameters to achieve high battery efficiency for power saving purpose and in order to optimize performance for battery operated Radio-Frequency System-on-Chip (RF SoC) applications.

Therefore through the Nano-power technology objects will no longer be neutral and passive, but active and participatory in all new forms of interactions for the creation of a smarter planet. Recent development of highly integrated System-on-Chip (SoC) design leads to the production of more powerful consumer electronics products such as smart-phones, requiring several LDOs in order to optimize the power consumption of different circuit blocks independently, thereby improving the system performance in [4]. Besides, in [3] low quiescent current, or in another hand low power quiescent (low power dissipation), low-dropout (LDO) regulators are spectacularly popular and are widely used for their power efficient nature. On the other hand, different techniques have been proposed in the literature to improve the transient response of LDOs. In [5]-[8] a reduced supply voltage is necessary to

decrease power consumption to ensure a reasonable battery lifetime in portable electronics. For the same reason, low-power circuits are also expected to reduce thermal dissipation, of increasing importance with the general trend in miniaturization. In [2]-[3], current amplifier Miller compensation is used, reducing the total compensation capacitance but increasing the power consumption and the complexity of the design. Furthermore, in [9]-[10], Gm-C filters are employed to omit offset and noise signals, but the drawback of these circuits is their high power dissipation. Even in [1], if the resistors of these amplifiers are implemented using transistors, its power consumption is still a problem. In addition, a cascode compensation with a dynamic bandwidth boosting was proposed in [12]-[13], which guaranteed stability over the full range of alternating load current at the expense of high power consumption.

Hence, to ensure stability, frequency compensation is always required especially for multistage amplifiers. For this reason, some frequency-compensation topologies such as nested miller compensation [10] have been used to implement multistage amplifiers. In these amplifiers, although the stability problem has been basically solved, the enormous power dissipation and bandwidth reduction remain a serious problem. Unfortunately, the problem of the energy consumption still exists. Although these topologies can basically solve the problem and make multistage amplifiers practicable, they suffer from serious problems such as enormous power dissipation and bandwidth reduction. More importantly, existing structures of the regulators operate in the region of strong inversion static dissipating a power of a few microwatts.

Particularly, the optimization of the power dissipated in these circuits is the subject of study for many designers. The classics regulators CMOS operating in the strong inversion region [22]-[23], the design of these circuits is made with polarized transistors in the region of strong inversion of the drain-source channel [22]. In this region, the gate-source polarization voltage $V_{GS}$ is greater than the conduction threshold voltage $V_{TH}$ ( $|V_{GS}| > |V_{TH}|$ ) hence the drain current of a few microamperes and therefore the power dissipated in the regulator is a few microwatts.

In this paper, we propose a new regulator LDO structure operating in the weak inversion region, the static power dissipated in the regulator is thus reduced of some nano-watts. In the recent years, the increasing demand of these circuits, consequently, push the designers to improving the performance. Our study is busy at the minimization of the static power (quiescent power) dissipated in the regulators.

The basic idea is to polarize all transistors that are enter in the design of the regulator (except the pass transistor: power transistor) with the currents drains of a few nano-amperes in the weak inversion region of the transistors. In this region, the gates-source voltages $|V_{GS}|$ are slightly lower than the conduction threshold voltage $|V_{TH}|$ ( $|V_{GS}| < |V_{TH}|$ ). The power dissipated in the regulator is thus greatly reduced. The small Slew-rate of the output error amplifier signal (pnincipal blocks of the regulator) is the major drawback of the regulators operating in the weak inversion region.

The basic idea of the solution to this problem is to amplify by mirror effect the low current polarization of the amplifier. So the load capacitor the latter is controlled by an output current of a few nano-amperes error, the process allows to get a slew-rate of the same order of the grandeur as that of the amplifier operating in strong inversion.

## 2 Proposed LDO Architecture

The proposed LDO regulator is depicted in Fig 1. The error amplifier is realized by a dynamically biased differential amplifier input stage with transistors NMOS-PMOS. Moreover, for good performance at: low power dissipation, low frequencies, the output stage is controlled by a feedback loop. This feedback loop consists of an amplifier driving the gate of transistor MP, So the gate of transistor MP has to be driven at a gate-source voltage than the output voltage and this might be lower than the input voltage of the LDO. The feedback network (FB) is realized by four diode-connected PMOS transistors, M1, M2, M3 and M4, with same aspect ratio. By using this approach, the silicon area of the feedback network is smaller as compared to the conventional approach using passive resistors. The reference voltage, VREF, is half of the LDO regulator output voltage. Sub-threshold MOS transistors are utilized as a feedback network instead of conventional poly or N-well resistors in order to save standby current, minimize power dissipation and minimize silicon area. Indeed, the band-gap current drained through the pass transistors provide enough phase margin to guarantee stability, even at no load condition [6].

The transistor MP is sub-power and main power transistor. The transistor size of MP is 600µm/100nm. The feedback network is realized by a string of diode-connected PMOS transistors M29 - M34 biased in the sub-threshold region to minimize quiescent current as well as the silicon area [11]. Furthermore, in ultra-low power design, the silicon area will be much larger if the feedback network is realized by conventional approach using passive resistors. Finally, the error amplifier was implemented using two-stage with self biased current mirrors topology. Note that the transistors M3, M4, M9, M10, M11 and M12 are set to operate in common-gate configuration and weak inversion. A significant disadvantage of the weak inversion is that very small currents are available to drive output capacitance so the slew rate becomes very small. Therefore, a conventional common-source differential-input amplifier with small tail-current is chosen as the first gain stage, which is constructed with transistors, M1, M2, M3 and M4, and M5 acted as a tail-current. The error amplifier gain is increased with a positive feedback current mirror and a negative feedback loop. MN14, MN13, MN2, MP4 and MP9 are organized as the positive feedback current mirror. Transistors, M11, M12, M23 and M22, make up the second gain stage. Indeed, the band-gap current drained through the pass transistors provide enough phase margin to guarantee stability, even at no load condition [6].

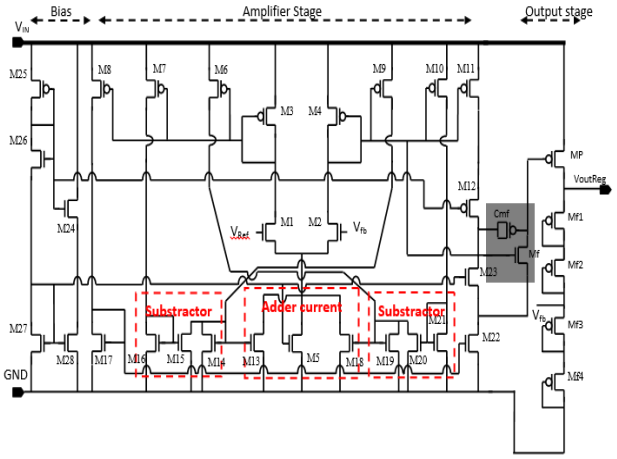



Fig 1. Conceptual schematic of the proposed LDO

## 2.1 Sub-threshold Operation

The MOS transistor has two primary regions of operation in which current flows from the source to the drain; they are the weak inversion or sub-threshold region and the strong inversion region. The sub-threshold region occurs when the gate voltage $V_{GS}$ is less than the threshold voltage $V_T$ and the strong inversion region occurs when the gate voltage is greater than the threshold voltage. The sub-threshold current is diffusion current and the strong inversion current is a drift current. The immediate region where the strong inversion and sub-threshold regions meet is called the transition region. Fig 2 where the drain current versus the gate voltage is represented shows the three regions. The current is plotted on a logarithmic scale so that the diffusion current, which depends exponentially on the gate voltage, can be viewed. Most nano-power amplifiers use transistors in the sub-threshold region, the sub-threshold characteristics.

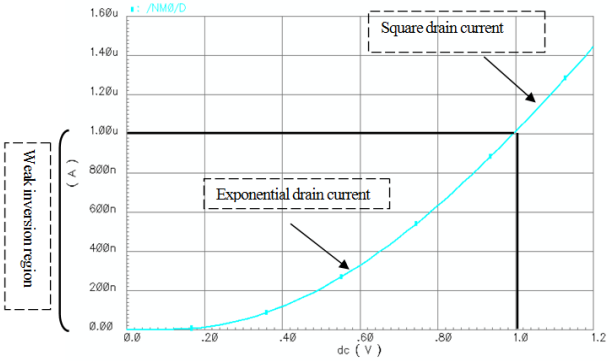



Fig 2. Characteristics of the transistor in the weak inversion region

In weak inversion regime the expression of drain-source current of the simplified model of the transistor is:

$$I_D = \mu_n C_{ox} {}^{W}/_{L})_i (n - 1) V_T^2 exp\left(\left({(V_{gsi} - V_{TH})}/{n V_T}\right)\right)\left(1 - exp\left({-V_{dsi}}/{V_T}\right)\right) \quad (1)$$

Where W and L are the effective channel width and the effective channel length respectively, $V_{TH}$ is the threshold voltage, $V_T$ is the thermal voltage of the MOSFET devices, µ is the carrier mobility, and COX is the gate-oxide capacitance. The power dissipation of the proposed LDO topology is given by (2). Finally, n is a non-ideal factor known as the sub-threshold slope is given by (3).

$$Power_{diss} = (V_{DDD} - V_{SS})\mu C_{ox}\frac{W}{L}(n - 1)V_T^2 e^{\frac{1}{nV_T}}\left((1 + V_{GS16} - V_{th})\left(1 - e^{\frac{-V_{DS16}}{V_T}}\right) + 2(1 + V_{GS14} - V_{th})\left(1 - e^{\frac{-V_{DS14}}{V_T}}\right) + 2(1 + V_{GS19} - V_{th})\left(1 - e^{\frac{-V_{DS19}}{V_T}}\right) + (1 + V_{GS21} - V_{th})\left(1 - e^{\frac{-V_{DS21}}{V_T}}\right)\right) \quad (0)$$

$$n = \frac{q.NFS.2\sqrt{\emptyset_B + V_{SB}} + \gamma_n C_{ox}}{C_{ox}.2\sqrt{\emptyset_B + V_{SB}}} \quad (3)$$

## 2.2 Dynamically Biased Differential Amplifier Input Stage

Fig 3 shows the local negative loop that increases the impedance of the Vout node. It consists of MP3, MP7, MN16, MN15, MN14, MN13 and MN1. To increase the impedance of the Vout node, the loop gain of the negative feedback may be large. The positive feedback helps to increase the loop gain of the negative feedback by boosting up the drain node impedance of MN12, MN23 and MP11, MP12. It also consists of MP4, MP9, MN14, MN13 and MN2.

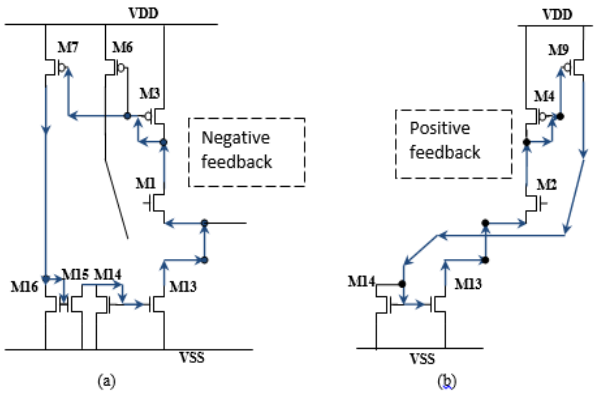



Fig 3. Feedback control: (a) the negative feedback, (b) positive feedback

To get a large enough gain and wide bandwidth on the one hand for the differential error amplifier and in the other side for the LDO regulator, the gain of the error amplifier is increased with a gain boost-up using local positive and negative feedback.

## 2.3 Band Gap Reference Circuit

Fig 4 shows a proposed band gap reference voltage schematic. M38 and M39 form the input pair. M2, M8, M14, and M15 form the bias network. M12 and M13 form an active load. VDD is the supply voltage; Vd7 is the drain voltage of M35 (or source voltage of M31) is connected to the tail voltage of M38 and M39. VRef is the output voltage and is connected to the gate terminals of M39, the drain of M43 and the source of M44. This technical is used to restore balance to the input pair. M43, M44, and M45 form the output stage of the band gap.

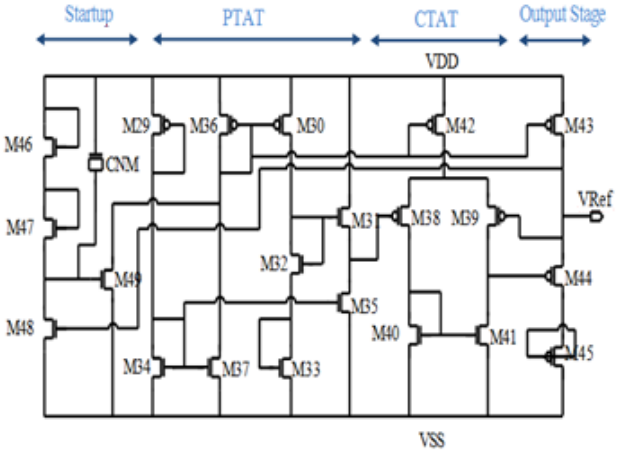



Fig 4. Schematic of the proposed band gap reference circuit [7]

## 2.4 Output and input noise of the load stage LDO

In general, for CMOS LDO circuit, the noise spectrum is dominated by 1/f noise at low frequencies and dominated by thermal noise of the transistors at higher frequencies. The frequency at which the 1/f noise is equal to the thermal noise denoted the corner frequency. The sub-threshold current is small due to the large drain-to-source resistance in the sub-threshold operation, which will allow a large thermal noise to pass through the circuit. Moreover, the LDO structure employed in this design is illustrated in Fig 1. The input transistors of the circuit are PMOS. Since the flicker noise of PMOS transistors are one to two orders of magnitude smaller than their NMOS transistors [24]. The output and input referred noise spectral density for a load stage LDO (large size) is given by (4) and (5):

$$S^2_{V,total} \cong \frac{8}{3}KT\frac{1}{g_{mMP}} + \frac{K_F}{C_{ox}WL)_{MP}f} + \frac{4KT}{g_{mf5}} + \frac{K_F}{C_{ox}WL)_{Mf5}f} \quad (4)$$

$$S^2_{Vin,Total} \cong 4KT\left(\frac{2}{3g_{mMP}} + \frac{g_{mMf5}}{g^2_{mMP}}\right) + \frac{K_F}{C_{ox}WL)_{MP}f} + \frac{K_F}{C_{ox}WL)_{Mf5}f} \quad (5)$$

Where $g_m$ is the trans-conductance of the MOSFET transistors, K is the Boltzmann constant, T is temperature in Kelvin, and W and L are the effective channel width and the effective channel length, respectively. Further, KF is another process parameter with an order of $10^{-25}V^2F$, while f is the frequency, and $C_{OX}$ is the gate-oxide capacitance.

### 2.5 Frequency response of the proposed LDO

The small-signal transfer function of the open-loop gain of the LDO can be obtained by means of analyzing its equivalent small-signal circuit. For simplification, we assume that the dc gain and the output resistance of each stage are large enough. The small signal model of proposed LDO is shown in Fig 5, in which $g_{mi}$, $r_{dsi}$, and $C_i$ are the trans-conductance, output resistance, and capacitance at the drain terminal of transistor Mi, respectively.

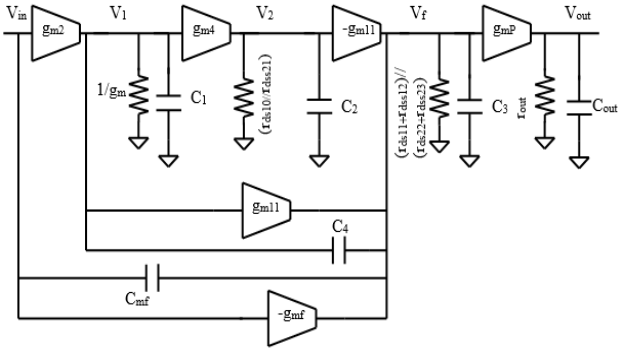



Fig 5. Small signal model of the proposed LDO

Analytically, the small-signal transfer function of the open loop gain of the low power amplifier described as seen in expression (6). Hence, the loop transfer function has three zeros, $z_1$, $z_2$ and $z_3$, and four poles, $p_0$, $p_1$, $p_2$ and $p_3$ are described as seen in expressions (7) - (13). Considering $R_1 = 1/(1/g_{ds10}//1/g_{ds21})$, $R_2 = 1/(1/g_{ds11}+1/g_{ds12})//(1/g_{ds23}+1/g_{ds22})$, $C_4 = C_{gd11}$, $C_{mf}$ is a miller capacitor, connected between the gate of MP and the output node of the amplifier stage where the output node of the amplifier stage and the gate of MF are connected, is used to move the dominant pole to the drain of M2 in first stead of the output node of differential stage. The major parasitic capacitances of a MOS transistor include junction capacitance $C_{db}$ and $C_{sb}$, as well as overlap capacitances $C_{gs}$ and $C_{gd}$, then the parasitical capacitances Cgs and $C_{bs}$ respectively are much larger than the corresponding parasitical capacitances $C_{bd}$ and $C_{gd}$. The bulk is tied to the source to reduce the threshold voltage. In doing so, $C_{sb}$ is shorted of each transistor. Since the impedances is smaller than the trans-conductances of each transistor, as given by: First, ( $C_{gs} >> C_{bd}$ , $C_{bs} >> C_{gd}$ , and $g_m / g_{ds} >> 1$.

$$A(s) = \frac{g_{mp}g_{m2}g_{m11}R_1R_2\left(1+\frac{-C_2}{g_{m4}}s+\frac{g_{mf}C_{mf}(C_1+C_2)}{g_{m2}g_{m4}g_{m11}}s^2+\frac{-C_{mf}C_2(C_1+C_4)}{g_{m2}g_{m4}g_{m11}}s^3\right)}{\left(1+\frac{s}{p_0}\right)\left(1+\frac{g_{m11}R_2C_4}{g_{m2}r_{out}}s+-R_1R_2C_2(C_3+C_{mf})s^2+\frac{g_{m11}R_1R_2C_{out}C_2C_4}{g_{m2}}s^2\right)} \quad (6)$$

$$Z_1 \cong {g_{m4}}/{C_2} \quad (7)$$

$$Z_2 \cong {g_{m2}g_{m11}C_2}/{C_{mf}(C_1+C_2)} \quad (8)$$

$$Z_3 \cong {g_{mf}((C_1+C_2))}/{C_2(C_1+C_4)} \quad (9)$$

$$p_0 \cong {g_{m4}}/{(C_1+C_4)} \quad (12)$$

$$p_1 \cong {g_{m2}r_{out}}/{g_{m11}R_2C_4} \quad (11)$$

$$p_2 \cong {g_{m11}C_4}/{g_{m2}R_1r_{out}C_2(C_3+C_{mf})} \quad (10)$$

$$p_3 \cong {g_{m2}(C_3+C_{mf})}/{g_{m11}C_4C_{out}} \quad (13)$$

## 3 Post Layout Performance Characterization

The proposed LDO topology has been designed and laid out, as shown in Fig 6, and the obtained performance metrics correspond to Cadence post simulations in a 90 nm CMOS process. The core area of the LDO is occupies an active area of 850 µm2. This work is improved by the use good layout techniques such as common centroid configuration and dummy devices were used to allow a good matching between the transistors.

The statistical analysis results, such as Monte Carlo simulations, are also used to test the performance in addition to the worst case. So, the worst case conditions are used for quick simulations, where the statistical analysis requires complex techniques and methodologies. Then, for the worst condition, the power dissipation variation in this analysis is less than 1µW. Monte Carlo analysis of the LDO output for 500 runs is shown in Fig 7. In this analysis the output means is 916nW and the standard deviation is 12nW.

Monte Carlo analysis was performed to study the LDO's sensitivity to process variation such as carrier mobility and MOSFET threshold voltage. The 99.7% of the fabricated IC would fall into the range of ± 30% of the nominal designed values. All the Monte Carlo simulations used a 10% variation in both threshold voltage and mobility per sigma. Fig 8 shows process variation effects on the power-supply rejection ratio better than -80 dB up to 100 KHz for different load currents.

Fig 9 shows the noise spectrum at 1.2 V supply. The 1/f cut-off frequency is at 1 KHz. The total integrated noise at 10Hz, 100 Hz, and 1 kHz are about 6.6 µV / $(Hz)^{1/2}$, 200 nV / $(Hz)^{1/2}$, and 6 nV / $(Hz)^{1/2}$ respectively.

Load regulation was defined as the measure of the circuit's ability to maintain the specified output voltage under varying load conditions [12]. This is an especially important characteristic for the LDO proposed because it should be able to regulate output voltage level. Quantifying the load regulation is done by measuring the change in output voltage level over a specified change in load current. The effect of fabrication process variation for three corner cases « fast-fast(ff), typical-typical (tt),and slow-slow(ss) » on the load regulation of the LDO are shown in Fig 10, which indicate less sensitivity to the process variation. This time, however, the input voltage was fixed to 1.2V and the output current was varied from 0-mA to 20-mA or the full load condition. The output voltage deflects from the nominal 1V output as the load current changes. It achieves a good line regulation of 1.0%. This shows that the proposed LDO regulator remains stable even during a fast transition of the supply voltage.

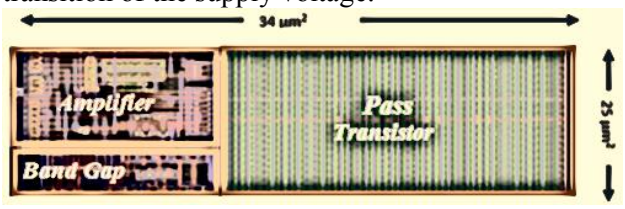



Fig 6. Layout of the proposed LDO

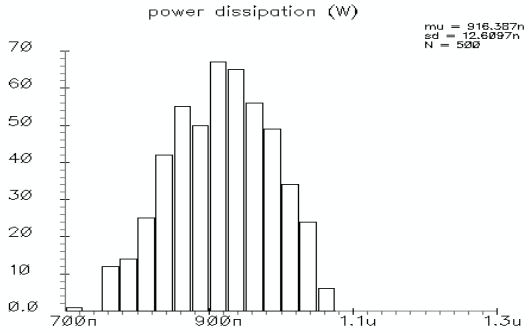



Fig 7. Results of the Monte Carlo analysis for 500 iterations

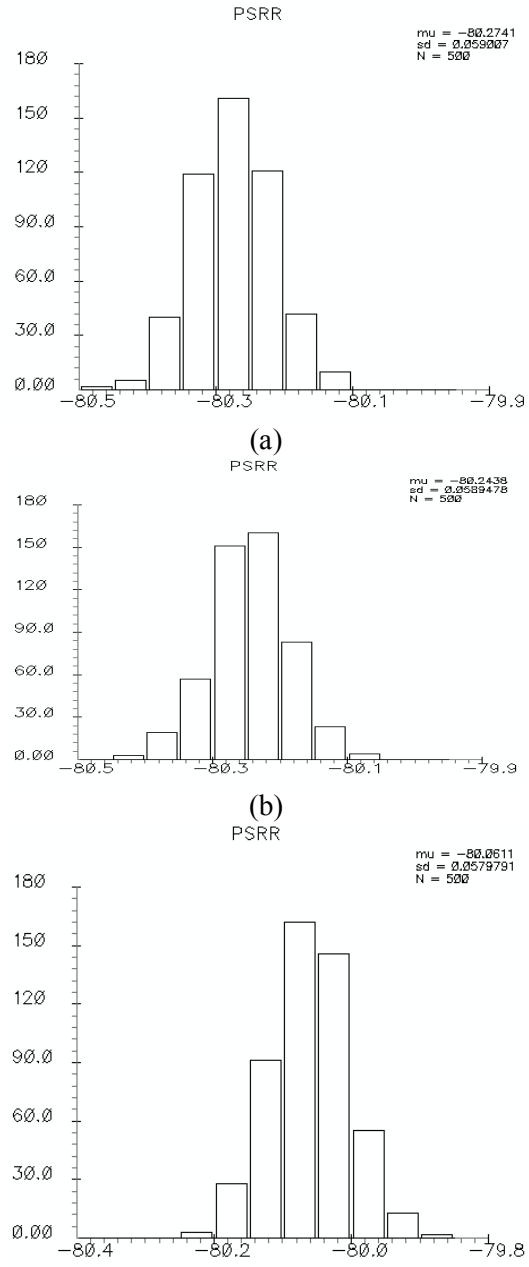



Fig 8 Monte carlo analysis of the PSRR@10kHz: (a) for ILoad = 0 mA. (b) for ILoad = 5 mA. (c) for ILoad = 50 mA.

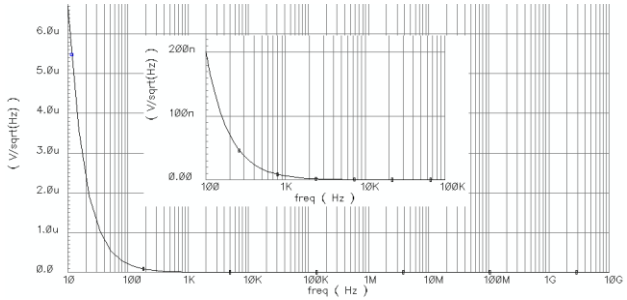
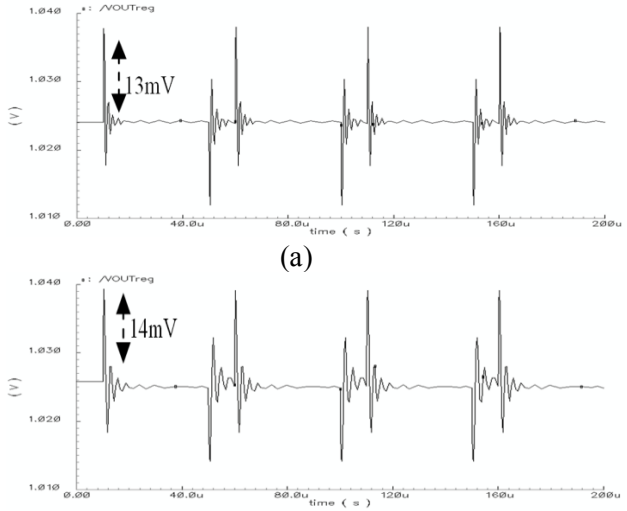
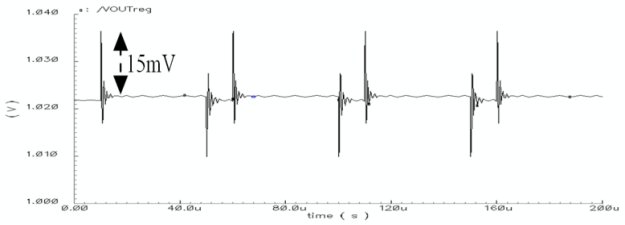



Fig 9. Post layout simulation result for noise spectrum of the LDO




(a)

(b)




(c)

Fig 10. Load transient response of the proposed LDO regulator in different corners, (a) Typical-Typical, (b) Slow-Slow and (c) Fast-Fast

For better comparison, Table 1 provides a performance comparison between the proposed LDO and recent works. For the reported LDOs, both the simulation and experimental results are mentioned. The comparison clearly shows the improvements of proposed design, which requires a new regulator LDO, by using a structure operating in the weak inversion region and provides the best transient response and regulations. In the other hand, the proposed LDO is suitable for practical applications, presenting extremely fast transient response as well as low power consumption and excellent line and load regulations. Note that, when compared to the rest of LDOs reported in the literature, the proposed circuit occupies a larger silicon area. However, when only active area is considered, this value is reduced to 468µm$^2$.

Table 1
Provides a performance comparison between this work and recently published designs

| Parameter | [20][a] | [19] [a] | [17] | [22] [a] | [15] | [14] | [21] [a] | This Work [a] |
|---|---|---|---|---|---|---|---|---|
| Technology (CMOS) | 0.35µm | 180-nm | 180-nm | 180-nm | 90-nm | 0.13-µm | 65-nm | 90-nm |
| Supply Voltage (V) | 1.4 | 1.2 | 1.4-1.8 | 1.2 | 1.2 | 1.4 | 1.2 | 1.2-2 |
| VDROP (mV) | 200 | 200 | 200 | 200 | 300 | 200 | 200 | 200 |
| Vout (V) | 1.2 | 1 | 1.2 | 1 | 0.9 | 1.2 | 1 | 1 |
| Iload,max (mA) | 100 | 100 | 100 | 100 | 100 | 50 | 50 | 20 |
| Line Reg.(mV/V) | N.A. | N.A. | 0..37 | 0.7 | N.A. | 2.4 | 8.89 | 4.12 |
| Load Reg.(µV/mA) | N.A. | N.A. | 2 | 70 | N.A. | 3500 | 34 | 55 |
| CL (pF) | 100 | 100 | 100 | 100 | 600 | 100 | 10 | 100 |
| IQ (µA) | 130 | 3.7 | 46.4 | 3.7 | 6000 | 4.1 | 23.7 | 0. 9 |
| PSRR(dB)@1KHz | 62dB @1kHz | N.A. | 48dB@1kHz | 65dB@1kHz | N.A. | 45dB@1kHz | 52dB@1kHz | 68dB@1kHz |
| Current efficiency % | 95.74-99.87 | 73- 99.99 | N.A. | 99.99 | 94.3 | N.A. | 99.95 | 96 |
| ΔVout mV | 125 | 277 | 55 | 277 | 90 | 198 | 40 | 38 |
| TR µs | 2 | 6 | 7 | 6 | 0.00054 | 1.16 | 1.65 | 0.72 |
| FOM [aa] ns | 0.089 | 0.222 | N.A. | 0.000102 | 32000000 | 32000 | 0.782 | 0,036 |
| Active Area µm$^2$ | 69000 | 25300 | N.A. | 25300 | 8000 | N.A. | N.A. | 852 |

[a] Simulation Results.
[aa] FOM=TR (Recovery time). IQ / ILoad.MIA . (The smaller FOM means the better performance).
NA: Not Available

Furthermore, the voltage difference (ΔVout) of the proposed LDO is lower than that of [21]-[22], [14]-[17], and [19]-[20], but it is higher than that of [15].

## 4 Conclusion

In this paper, a CMOS low power dissipation LDO regulator is introduced based on a less power dissipation proposed amplifier. The proposed LDO is designed using cost-effective 90nm CMOS technology. Post-layout simulation results show that the LDO occupies an active area of 852 µm2, consuming only a quiescent current of 1 µA at a minimum load of 20 mA. The LDO is able to regulate the output at constant 1 V with a dropout voltage of 0.2 V. The total power consumption of the amplifier and driven-right-leg circuit is reduced to 900 nW while the important parameters of the amplifier are kept comparable to similar works. This result is achieved using negative feedback and

positive feedback transistors of the in the sub-threshold region. As the result, the proposed LDO is suitable to be used in many RF SoCs Applications due to its advantage of low power dissipation.

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