Interline Power Flow Controller with Control strategy to limit Fault Current in Electrical Distribution System

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Abstract: In this article, Interline power flow controller (IPFC) has been recommended to limit the short circuit current (SCC) in low voltage (LV) electrical distribution system. Industrial loads are increasing due to various reasons in the distribution system. It leads to the power requirement at the distribution system level. Therefore, there is a scope for increase in the fault current. Due to the increased fault current, the protection of switchgear is vital. A simple control strategy wth IPFC is proposed in the distribution system to limit the fault current. Low voltage distribution system i.e 800 MW thermal power plant water system LV distribution system is considered for demonstrating the effectiveness of the IPFC. Short circuit analysis is performed without and with the IPFC by applying ETAP and MATLAB (SIMULINK). The simulation results are compared. Further, the effect of different ratings of standard transformers is also analyzed. It is noticed that the control strategy with IPFC can limit the fault current.

Key–Words: Interline power flow controller, short circuit current, ETAP and MATLAB

Received: December 12, 2019. Revised: June 5, 2020. Accepted: June 16, 2020. Published June 30, 2020

1 Introduction

Limiting of fault current is a necessary to suppress the stress within the electric distribution system. It is important to limit the stress over a certain assets of electric distribution system[1]. Modern power systems are designed with a high degree of flexibility[2]. Therefore, least part of the electrical distribution system may be interrupted during the fault condition. The electric power is distributed via step down transformers in low voltage distribution system to different loads. The rating of the transformers should be verified. If the fault current is within the limits, parallel operation of the transformers is feasible. To compensate other loads, an extra set of transformers with LV switchgear is required. An alternative solution is compensation equipment installation to reduce short-circuit current[3],[4].

1.1 Literature survey

Several researchers have used various devices and algorithms in the past four decades to limit the fault current. Limiting reactors are used for three-phase faults[5] and grounding device and modifications of zero sequence impedance are usual practices for line to ground fault. The alternative equipment is FACTS device. Primary function of the FACTs device to control powers and maintain voltage within the limits.

The fault limitation strategy using FACTS devices is first introduced in [5] and [6]. a SMES with a series phase compensator is used for current limiting in [7]. A novel hybrid current-limiting circuit breaker for medium voltage is suggested in [8]. A series compensator with fault current limiting function is presented in [9]. Dual functional medium voltage level DVR has been used in [10] to limit downstream fault currents. Other techniques [11],[12],[13] are also applied for short circut studies. TCSC has been proposed to reduce fault current in [14]. Particle swarm optimization [15] has been applied to reduce the losses and fault current Level. It is explained with control strategy. The fault current limitation is achieved by switching off all the switches and changing the DSSSC from inverter mode to rectifier mode[16].Effectiveness of the IPFC to reduce the I_F reduction is discussed in [18,19].

1.2 Observation and Motivation

Limiting fault current in low voltage distribution system is an issue due to an increase in industrial loads.

The short circuit current levels increase with the added lines in the low voltage distribution system. The fault current limitation offered by controllers becomes crucial to diminish such large currents. The fault current is limited using impedance control. However, use of the FACTS devices for reducing the I_F is limited. The alternative equipment is a FACTS device. These observations motivates to introduce the IPFC for short circuit study.

1.3 Contribution

- Deployment of the interline power flow controller for limiting the fault current
- Short circuit analysis on switchyard with different faults
- Control strategy is applied
- Simulation results with various case studies are explained

1.4 Organization of the article

Organization of the article is provided here.

- Short circuit calculations for transformer is provided in section 02
- Section 3 describes the fault calculations with IPFC
- Control strategy is presented in section 04
- Simulation results with various case studies is explained in section 05
- In section 06 conclusions of the work is provided

2 I_F calculation for Transformer

The short-circuit current levels increases with the addition of lines. The fault current limitation offered by controllers becomes crucial to diminish such large currents. Short circuit current (SCC) calculation are provided in the following sub-sections. Fig.1 shows diagram of distribution system.

The diagram is shown in Fig. 2. A three-phase fault has take place at LV bus. Fault current is calculated as follows.

$$E = Z_{T1} I_{F1} \tag{1}$$

$$E = Z_{T2} I_{F2} \tag{2}$$

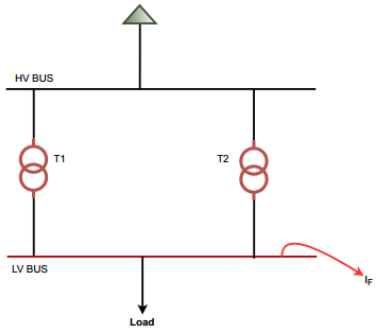

Figure 1: Diagram of Distribution system

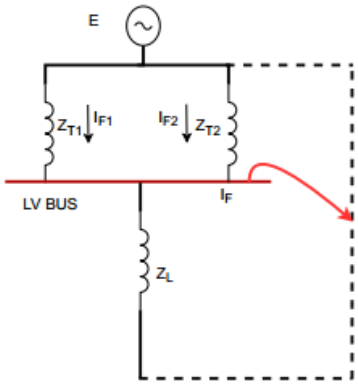

Figure 2: Impedance diagram

Bus fault current I_F is

$$I_F = I_{F1} + I_{F2} \tag{3}$$

$$Z_{sc} = \frac{Z_{T1} \times Z_{T2}}{Z_{T1} + Z_{T2}} \tag{4}$$

$$I_F = \frac{E}{1.732 \times Z_{sc}} \tag{5}$$

I_{sc} is calculated using the above equation. It depends on the transformer impedance at low voltage bus. The load impedance is un-controlled. Change in the I_{sc} is decided by the impedance of the transformer. But it is fixed.

3 I_F calculation with IPFC

Interline power flow controller is connected at the low voltage side of the distribution transformer. It is installed with two transformers at the common low voltage bus. It is used to balance the load in normal operation. Controller senses the V_{BUS} during the fault condition. The controller injects negative voltage in the reverse direction of the $V_{generated}$. The simple network is indicated in Fig. 3.

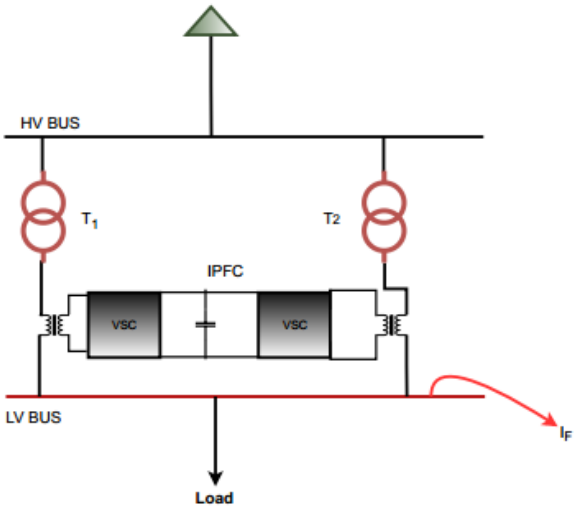

Figure 3: Diagram of distribution network with IPFC

During the fault, the IPFC injects the controlled voltage V_{se1} and V_{se2} into the lines in reverse to the generated voltage to suppress the I_F. The equations are provided here.

$$E = Z_{T1} \times I_{F1} + V_{se1} + X_{se1} \times I_{F1} \quad (6)$$

$$I_{F1} = \frac{E - V_{se1}}{Z_{T1} + X_{se1}} \quad (7)$$

$$E = Z_{T2} \times I_{F2} + V_{se2} + X_{se2} \times I_{F2} \quad (8)$$

$$I_{F2} = \frac{E - V_{se2}}{Z_{T2} + X_{se2}} \quad (9)$$

From (9) and (11) it is noticed that the SCC is reduced. therefore, the injection of voltage is a vital consideration.

4 Controller Design

The controller provides an injection of voltage.The the proposed control strategy is given in Fig. 4

The above controller will work as per following rules.

- The proposed controller is a closed loop function with comparison of Source voltage (E) and load voltage (VL)
- During short circuit load voltage is zero and resultant after the summator only source voltage will be appeared.

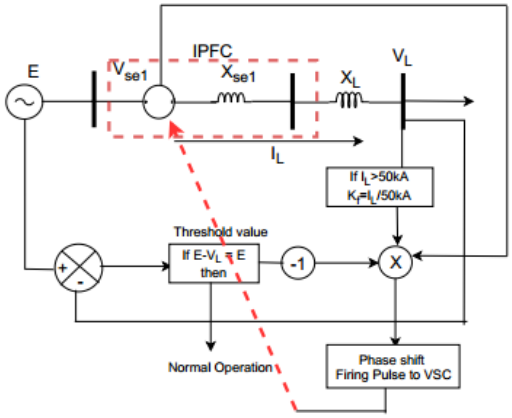

Figure 4: Block diagram of the controller

- In this condition –ve voltage will be injected in a system, for this Vse1 will be multi-plied with -1 and Kf will be multiplied with Vse1
- With Kf, it will be decided to required injection of voltage in series in a system to re-duce the fault current
- This intern firing angle is adjusted to inject voltage in opposite direction of source.

During the fault, the controller will verify the bus SCC. If the measured current is more than desired SCC of the switchgear, then during this condition

$$K_f = \frac{I_L}{50 \times kA} \quad (10)$$

$$V_{inj} = -K_f \times V_{inj} \quad (11)$$

The following case studies demonstrate the proposed concept.

5 Results and Discussion

In this section, various test cases are analysed for different fault conditions. The test cases are develoed in ETAP and MATLAB. The parameters considered in the implementation of the IPFC are shown in Table 01. The details of transformer can be found in [17].

Table 1: Parameters of IPFC

s.no	parameter	value
1	Line nominal voltage	415 V
2	Apparent power	1 MVA
3	Switching devices	IGBT

5.1 Case 01

The test case shown in Fig. 5 is developed in ETAP and MATLAB. Rating of the transformer is 1600 kVA,6.25$percent$ and the load is water system unit with 800 MW. Various fault analysis has been done on this system. The results are provided in the subsequent sections.

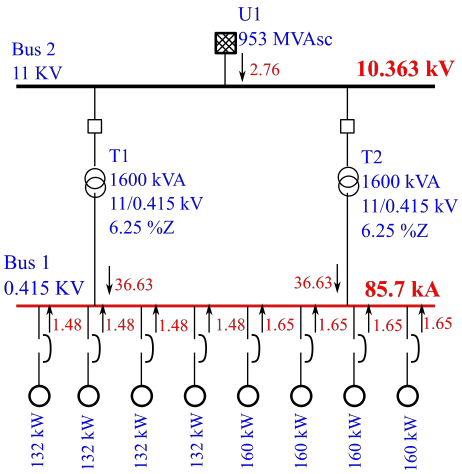

Figure 5: Test case 01

5.1.1 Symmetrical fault

3 phase fault is performed at switchgear bus in ETAP. The fault is set at 0.4 seconds. During the symmetrical fault, the current is noted. The fault current is 85.7 kA. The fault current is plotted and provided in Fig. 06

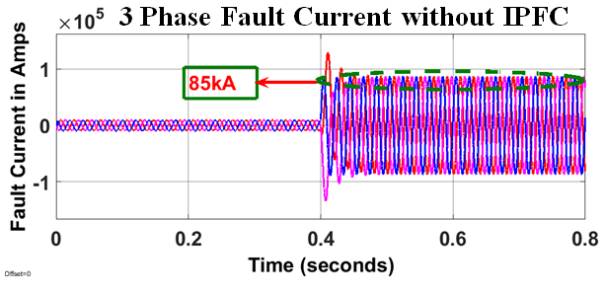

Figure 6: Bus fault current for 3 phase fault

The same model has been developed in MATLAB (SIMULINK). The I_F is aproximately 85 kA. It is almost double of the rated fault current in presence of the cascade transformers.

5.1.2 LG fault

Line to ground fault is performed at switchgear bus in ETAP. The fault is set at 0.4 sec. During the symmetrical fault, the current is noted. The fault current is 85.7 kA. The fault current with IPFC is plotted and provided in Fig. 07.

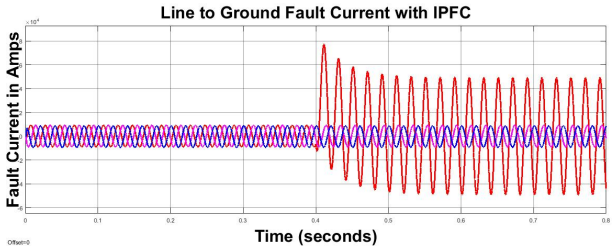

Figure 7: LG fault current without IPFC

5.1.3 LL fault

Line to line fault is performed at switchgear bus in ETAP. The fault is set at 0.4 sec. During the symmetrical fault, the current is noted. The fault current is 85.7 kA. The fault current with IPFC is plotted and provided in Fig. 08.

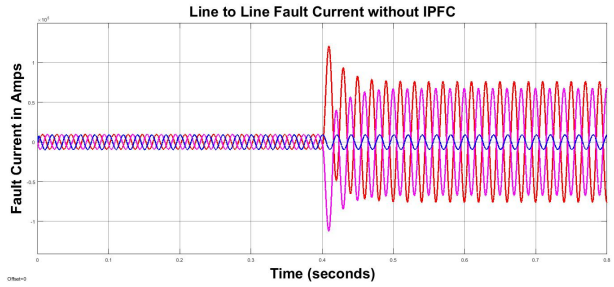

Figure 8: LL fault without IPFC

5.1.4 LLG fault

LLG fault is performed at switchgear bus in ETAP. The fault is set at 0.4 sec. During the symmetrical fault, the current is noted. The fault current is 85.7 kA. The fault current with IPFC is plotted and provided in Fig. 09.

5.2 Case 02

In this case, the deployment of the IPFC is shown in Fig. 10.

The fault current for LG fault is indicated in Fig. 11 and Fig. 12.

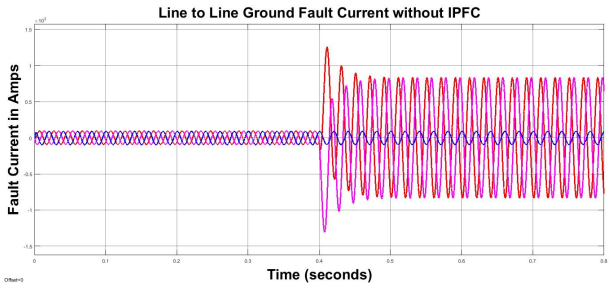

Figure 9: LLG fault without IPFC

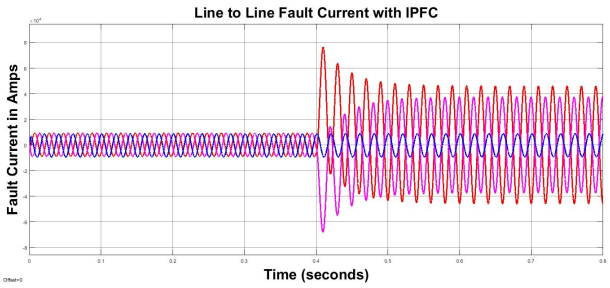

Figure 12: L-L fault IPFC

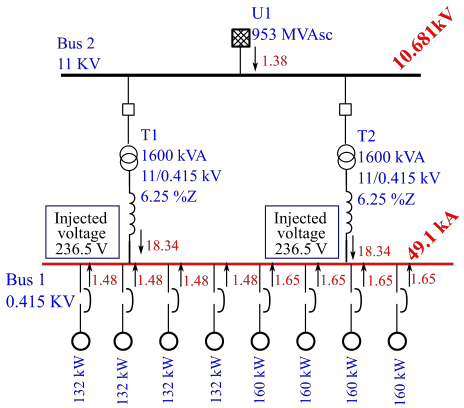

Figure 10: ETAP Model for 1600kVA transformer with IPFC

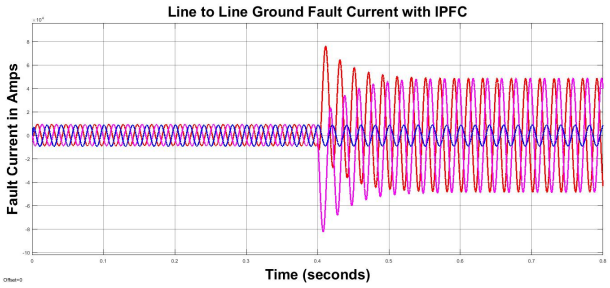

Figure 13: LLG fault current with IPFC

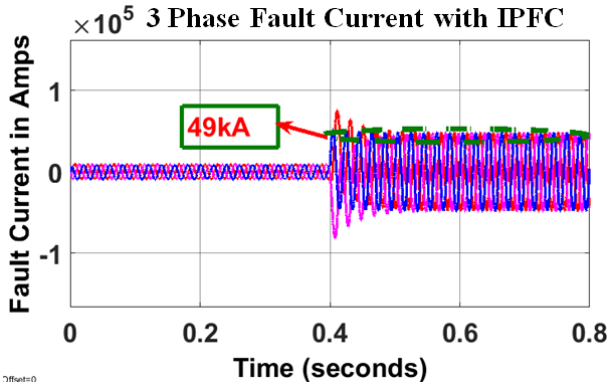

Figure 11: 3 phase fault current at Bus with IPFC and 1600 kVA transformer

The I_F is comedown from 85.7 kA to 49 kA. It is because of the limit on $V_{Injected}$ of the IPFC. When the bus I_{SC} is observed by voltage injection method in ETAP, the injected voltage is 236 V. The results of fault current is matched with simulated results.

5.3 Case 03

In this case, Two 1250 kVA transformers with 5 percent of impedance are considered.

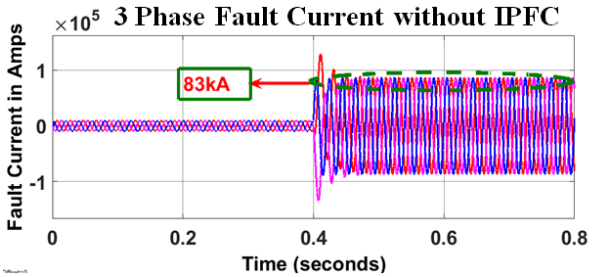

Figure 14: Fault current without IPFC for 1250kVA transformer

From Fig. 8 and Fig. 9 there is a reduction in I_F. For 1600kVa and 1250kVA rating of transformers, IPFC is utilized. The summary of the different case studies is tabulated in Table 2.

Table 2: Fault currents with and without IPFC

s.no	Rating	Z	case 01	case 02
1	1600kVA	6.25	85.342kA	49.129kA
2	1250kVA	5.00	83.234kA	49.846kA

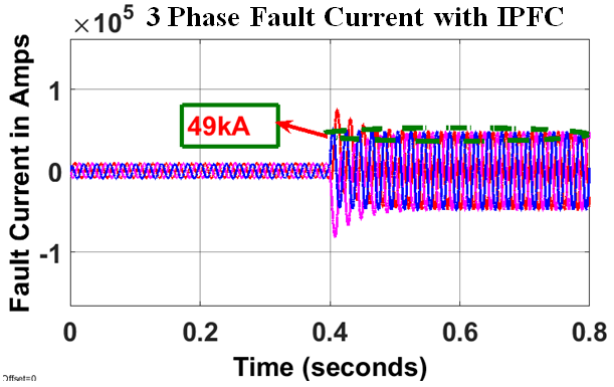

Figure 15: Phase bus fault current with IPFC for 1250kVA transformer with Simulink analysis

case 01 I_f without IPFC case 02 I_f with IPFC

5.4 Result comparision

Table 3: Fault currents with and without IPFC

s.no	Type of Fault	case 01	case 02
1	L-L-L	85.342 KA	49.129kA
2	L-G	85 kA	49 KA
3	L-L	83 kA	42 kA
4	L-L-G	84 kA	49 kA

In the above table, case 01 is I_f without IPFC and case 02 is I_f with IPFC.

Table 4: Fault currents with and without IPFC

s.no	Type of Fault	case 01	case 02
1	L-L-L	83.234KA	49.846kA
2	L-G	83kA	49 KA
3	L-L	83 kA	42 kA
4	L-L-G	83kA	49 kA

In the above table, case 01 is I_f without IPFC and case 02 is I_f with IPFC. With the cascade transformers, the fault current reaches to 85kA during L-G fault. With the deployment of the IPFC with the proposed control strategy, the fault current in the line is reduced from 85 kA to 49 kA. The percentage reduction is around 57 % of the fault current. Different phase faults of L-L and L-L-G faults without and with IPFC analysis are provided in Table 03. For other cases, reduction of the fault current is 55 percent. From the above, the IPFC is able to reduce fault current in all the fault conditions both symmetrical and unsymmetrical faults. Moreover, two transformers are operated in by satisfying two conditions i.e (i) vector group of the transformers, (ii) voltages, (iii) the short circuit current must be below the designed fault current. But as per third condition it is not possible to reduce fault current below 50kA due to parallel of transformer impedance. Therefore, FACTS controllers are the best suitable for reducing the short circuit current. Another observation is that the IPFC controls the active power and reactive power n normal operation and operates in inductive mode to reduce fault current during short circuit.

6 Conclusion

This article is focused on the deployment of the interline power flow controller to reduce the fault current in low voltage distribution system. Reduction of the I_F with the IPFC is much encouraging. It has been noticed from the results the I_F is with the deployment of the IPFC compared with the transformer. It can gives huge economical benefits to the medium scale industries. The economic benefits are (i) fault current of busbar design can be retained to 50kA instead of going to 65kA fault current, (ii) parallel operation of transformers can be allowed in industries instead of going for another set of transformer and new LV switchgear. With these reasons, 10 to 15 % of switchgear equipment cost can be reduced. This analysis may be extended to check for other rating of transformers and technical and economical feasibility for various process plant industries.

Acknowledgements: Authors thank BITS Pilani University for providing infrastructure. Also the authors thank Tata projects limited.

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