Configurable converter for performance assessment of cascaded multilevel power converters

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Abstract— This paper presents the development of a configurable converter, designed and built for the evaluation of several configurations of cascaded H-bridge multilevel power converter with single DC source and separate DC source sub-topologies. The converter can be configured in the symmetric and asymmetric topologies and the voltage levels range is limited by the four H-bridges hardware. The converter also can be set to obtain modulations from 3 levels and up to 81 levels. For configuring the converter a MATLAB® graphical user interface was developed in order to facilitate the topology changes and selects the number of voltage levels and switching angles. It also allows optimizing the modulations by switching angles through a genetic algorithm. The interface data are encoded and transmitted to a FPGA which controls the configurable multilevel converter.

Keywords— Power converter, Multilevel converter, PWM, FPGA, optimization, genetic algorithm.

1. Introduction

The study of electric power quality is a current and relevant topic of discussion [1, 2, 3] indeed generalized with the advent and the widespread use of power inverters. The multilevel converters present a solution, due to the fact that their output voltage presents a harmonic content inferior to that of a conventional converter [4]. The other part of the solution is the control selection [5, 6], the topology [7], frequency variation method [8] and the technique used for modulation generation [9]. From this perspective, the converter is the element in charge to supplying the electrical power quality, provided it is of the appropriate design.

Among multilevel converters, there has been a rise in H-bridge cascaded converters, due their considerable advantages compared with classic topologies such as diode clamped or flying capacitor [4], [10]. Nevertheless, among the cascaded multilevel H-bridge converters, there are single DC source and separate DC source sub-topologies [11]. The first only requires one source of voltage for the whole converter and the insulation between stages is achieved with the use of transformers [12]. The second sub-topology needs a voltage DC source from the H-bridge and the sources should be insulated [13]. Both sub-topologies have their advantages and drawbacks. This work completes the development of a platform (configurable converter) that facilitates the in-depth study of each sub-topology's behavior, allowing in a matter of seconds the converter configuration and the modulation characteristics via a graphical user interface. The versatility of the platform allows the study multiple possibilities, with the goal of finding possible solutions in terms of power quality and efficiency.

2. A short review

The appearance of the multilevel power converter was the development of Baker and Lawrence's work in 1975 [14], now known as the cascaded H-bridge converter. In 1981, the first multilevel converter with three levels by means of diode fixation was presented [15]. From this patent and the respective work, there has been a wide variety of investigations in search of optimizing and improving the multilevel system of power conversion [13]. The utilization of the patent's original idea is now known as a sub-topology, [14], known as separate DC source [16]. Another proposal used a single DC voltage source to power all H-bridges and used transformers at the output of every bridge in order to create electrical insulation. The construction of the step waveform was

achieved through the cascaded connection of the transformers output. This sub-topology received the name 'single DC source cascaded H-bridge multilevel converter' [17, 18, and 19].

In terms of the optimization of the harmonic content of the multilevel converters' modulations, numerous techniques have been proposed depending on the sub-topology used, according to the specific objective and the nature of the search for the optimal point. [20, 21, 22]. However, there are promising strategies in the line of evolutionary algorithms such as Particles Swarm Optimization (PSO) [23], Ant Colony Optimization (ACO) [24] and genetic algorithms (GA) [25], [26], [27], among others. Genetic algorithms are methods of classic and functional optimization, that are used as a comparison to other methods of optimization, in the same way that the mathematic expression that describes THD in terms of switching angles, provides a clear criteria of evaluation of the function of optimization [9].

3. Cascaded multi-level converters

Fig. 1 shows the general diagram of a cascaded multilevel inverter with H-bridges (CMLI), where the basic function can be observed, in which the form of the output waveform is constructed through the addition of the output of each H-bridge. [14]. The CMLI topology can be divided into two categories, depending on the relationship of the voltages at each bridge. These categories are symmetrical and asymmetrical. They are symmetrical if the voltages in all bridges are equal and asymmetrical if the voltages are different (the relationships 1:2 o 1:3 are common used).

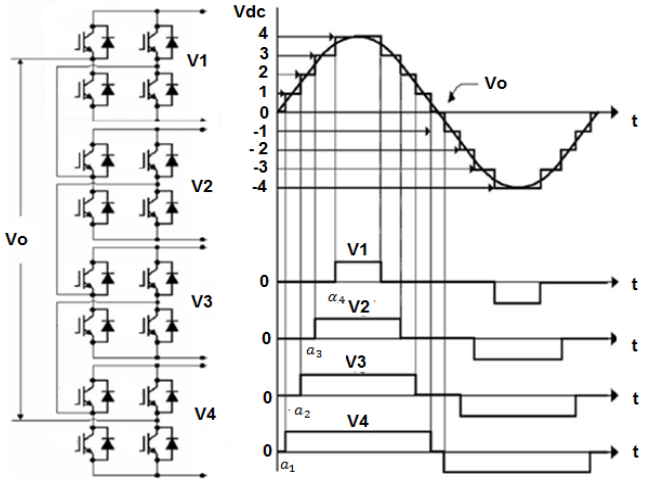


Fig 1. H-bridge multilevel converter, waveforms of the H-bridges and the converter output.

In terms of the ways of obtaining the voltage of each bridge, two sub-topologies can be described: separate DC source sub-topologies, in which all bridges are powered from separate sources (ver Fig. 2.a) and single DC source sub-topologies, in which all bridges are powered from the same source. The difference in voltages and the electrical insulation is achieved through the use of transformers. (ver Fig. 2.b.). Fig. 2.c shows an example of these sub-topologies in asymmetric form with relation to 1:2. The two obtain the same output voltage waveform [14].

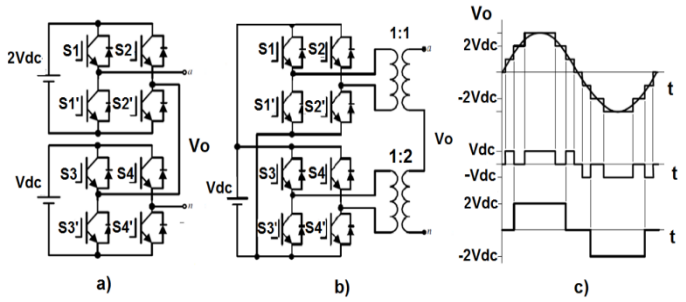


Fig. 2: Asymmetrical sub-topologies of the H-bridge cascaded multilevel converter. a) Separate DC source, b) Single DC source, c) Output.

4. Graphical User Interface

The software is divided into five options listed in a graphical user interface in Matlab® as shown in Figure 3.

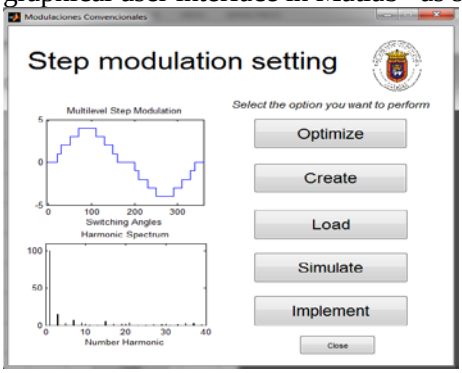


Fig. 3. GUI Main menu.

The "Optimize" option allows to find the switching angles that provide minimal harmonic content using genetic algorithm.

The "Create" option allows the system to create modulations by specifying switching angles of the first quarter of the waveform entered directly into the interface.

The "Load" option allows to read files containing an optimized modulation or modulation created in the interface.

The "Simulate" option performs the simulation of the cascaded converter multilevel allowing to observe the behavior of relevant electrical parameters presented in detail as the harmonic spectrum, waveforms by bridge and transistor, voltages, input and output currents.

Finally, the "Implement" option encodes information to be transmitted to the hardware.

All the option or processes related are outlined below.

4.1 Optimize process

The general process of the optimization of the software is presented in Figure 4. In order to obtain an optimized modulation, it is necessary to enter the parameters of the algorithm's functionality, which are: the number of levels of voltage of the first quarter of the wave, the order of the maximum harmonic of evaluation of THD and the maximum number of generations from the genetic algorithm. With the parameters, the search begins for the modulation with the least THDv evaluated up to the selected harmonic, and finally the genetic algorithm finds the optimum and delivers the switching angles, the form of the wave, the THD and the harmonic spectrum, among other data.

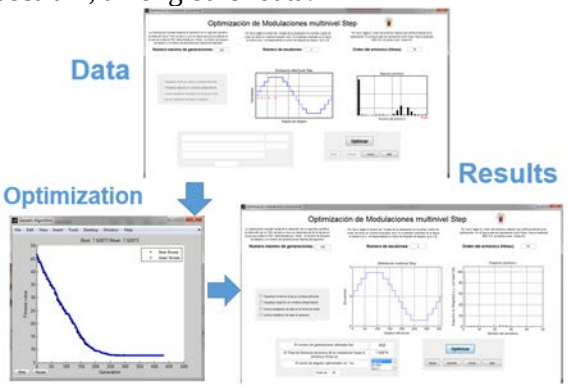


Fig. 4. Optimization process.

The functionality of the optimization algorithm is shown in the flow diagram in Figure 5, in which the vector L represents the number of shooting angles by stage in the first quarter of the waveform.

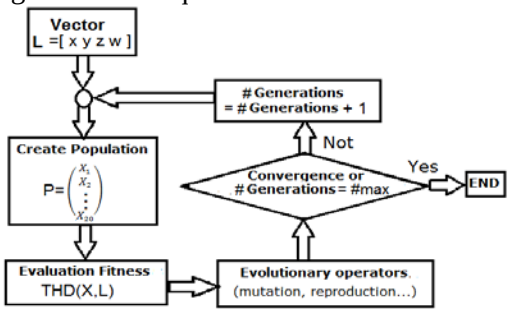


Fig. 5. Flowchart of the optimization algorithm.

For the step modulation, the switching angle corresponds to 1 for each level of voltage and each part of the vector indicates a voltage level [1 1 1 1 . .]. The algorithm begins with a random sample and continues mutating until it arrives at a convergence, evaluating the generations using function fitness.

The process of the genetic algorithm is carried out in Matlab® through the cell GA (Genetic Algorithm) which evaluates each generation with the mathematic expression of THD, expressed in terms of the number of levels and the number of switching angles per level, which corresponds to the fitness function (Equation 1), explained in detail in [7]. The αij corresponds to the angle, *j* is the number of the angle, *i* is the number of the step, and L_i is the component *i* of the vector *L*.

$$THD = \frac{\sqrt{\sum_{n=2}^{50}\left[\frac{1}{n}\left(\sum_{i=1}^{4}\sum_{j}^{L_i}(-1)^{j-1}\cos n\alpha_{ij}\right)\right]}}{\left(\sum_{i=1}^{4}\sum_{j}^{L_i}(-1)^{j-1}\cos\alpha_{ij}\right)}\cdot 100 \quad (1)$$

The corresponding optimization was performed using genetic algorithms, according to [28]. The population size is consider of 20 individuals, each individual (X) formed by all switching angles in the first quarter of the output voltage waveform

$$X = \left[\alpha_{11}, \alpha_{12}, \cdots, \alpha_{1x}, \alpha_{21}, \alpha_{22}, \cdots, \alpha_{2y}, \alpha_{31}, \cdots, \alpha_{1z}, \cdots, \alpha_{4w}\right] \quad (2)$$

The algorithm run was finished when the values of the population converge or when the number of generations reached the maximum assigned.

Figure 6a shows the result of the optimization process for a 5 levels voltage modulation. The full-wave corresponds to a 9 levels voltage modulation. At the interface, the upper limit of the sum entered is 50. So the genetic algorithm searches and evaluates the switching angles looking for a minimum value of the fitness function (THD value up to the 50th harmonics).

An optimum value of switching angles was found in generation 432, as shown in Figure 6b. Which corresponds to the harmonic spectrum shown in Figure 6c and has a THD value of 7.6287% and switching angles vector of [6.86512, -20.7844, -35.511, -55.8075].

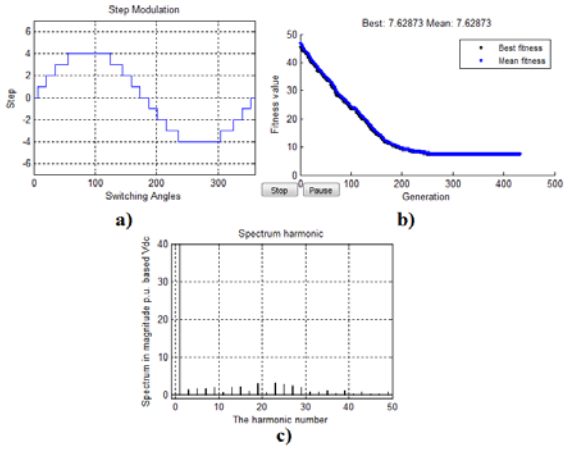


Fig. 6 The optimization process.

4.2 Modulation generation process

The stage of development allows to the system to produce any modulation up to 81 level, in which the software requests the input of the switching angles of the first quarter of the wave. Each angle corresponds to the change of a voltage level. The THD and the harmonic spectrum are updated with the change of any switching angle evaluated to the maximum harmonic selected. This process is shown in Figure 7. Upon completing the development, it's possible to store the modulation for later analysis.

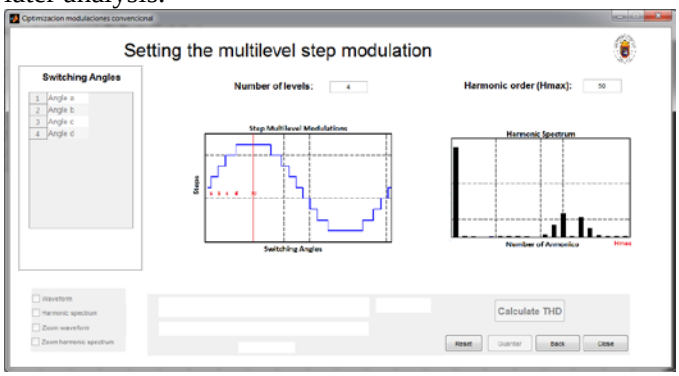


Fig. 7. Graphical user interface for modulation setting.

An application example for generating the switching angles, which were calculated according to the optimization described in Figure 5 is shown in Figure 8. Where it is known that the theoretical THD value of 7.6287%, with the switching angles vector of [6.86512, 20.7844, 35.511, 55.8075].

The result is presented in the process of generating the multilevel voltage waveform. Where the similarity of the THD modulation generated by the switching angles (up to harmonic 50) with the theoretical value calculated by the optimization process is evident.

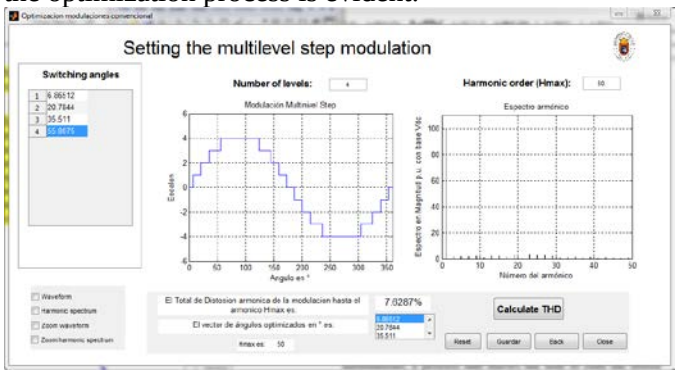


Fig. 8. Graphical user interface for step modulation setting.

4.3 Load modulations process

As the platform's interface allows the user to store modulations, a process that allows the user to read the stored modulations is of course necessary. In this process, the waveform of the modulation loaded along with the harmonic spectrum, the THD and the switching angles as observed in Figure 9 can be viewed. Yet despite its simplicity, this process provides the platform with the necessary memory capacity to use the optimized and developed modulations in the system.

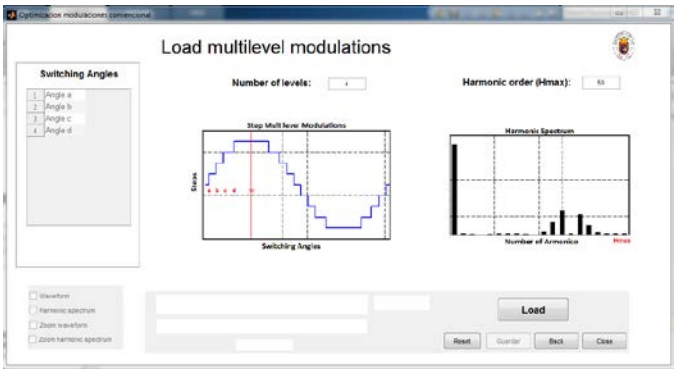


Fig. 9. Modulation loading interface.

4.4 Simulation process

The general process of simulation requires the input of the specific parameters of the hardware such as voltage (single DC or separate DC source), relationship of the sources (symmetrical, asymmetrical 1:2, 1:3), supply voltage and output RMS value. These parameters determine the number of necessary bridges and the characteristics of the converter. The simulation is carried out in its totality in Simulink as demonstrated in Figure 10. The product obtained is the relevant electrical parameters of the converter.

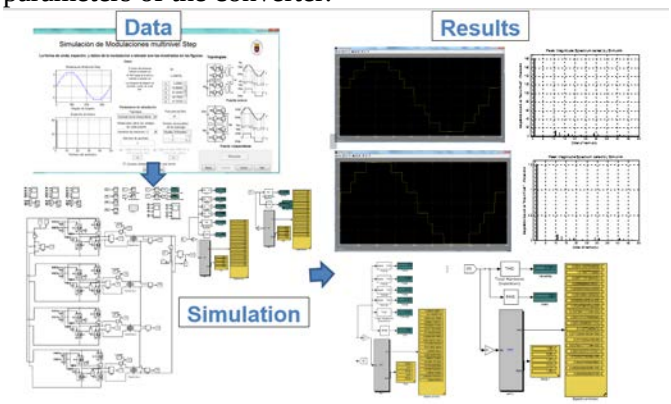


Fig. 10. Process of simulation.

The simulation carried out is only for the power stage and has the capacity to modify the number of H-bridges, the magnitudes of the sources of voltage and the topology. The simulation includes the measurements of input voltage, input current, output voltage of each H-bridge, output voltage of the converter, output current, display of the control signals, harmonic spectrum of voltage and current, and THD of voltage and current.

4.5 The process of implementation

The implementation is the culminating process of the visual interface, in which the parameters of the converter's hardware are required, between this the topology (single DC or separate DC source) and the relationship of the sources (symmetrical, asymmetrical 1:2, 1:3). The software calculates the number of H-bridges necessary and the values of voltage in order to implement the modulation obtained previously. The process is divided into two stages, the first being the calculation of the electrical parameters as in the case of the drive signals of every transformer. The system provides the RMS levels in the sub-topology single DC source for configurations with a number of levels equal to the maximum of the H-bridges. The second stage is the coding of the values to be transmitted to the FPGA that is responsible for sending the switching signals to the scalable converter (hardware). The form of the interface is shown in Figure 11.

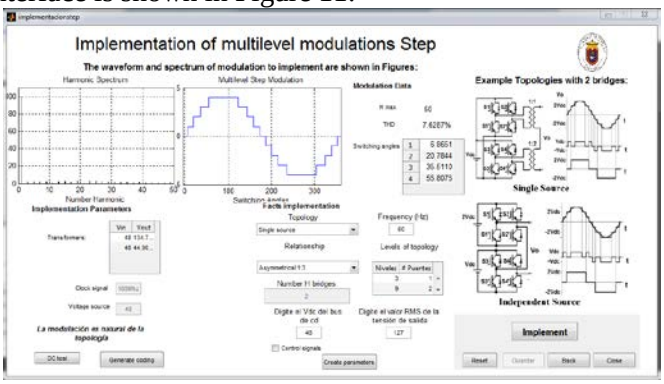


Fig. 11. Graphical user interface for modulation implementation.

5. Hardware

5.1 Overall scheme.

The aim of the system is to achieve the desired flexibility with the lowest number of switches, the result being the electronic diagram shown in Figure 12. The system relies on four H-bridges that permit one to obtain modulations of 3 to 81 levels of voltage, in symmetrical or asymmetrical configurations, with the highest level (81) reached with sources of asymmetrical relation 1:3:9:27, in single DC or separate DC source. As it is shown in Table 1.

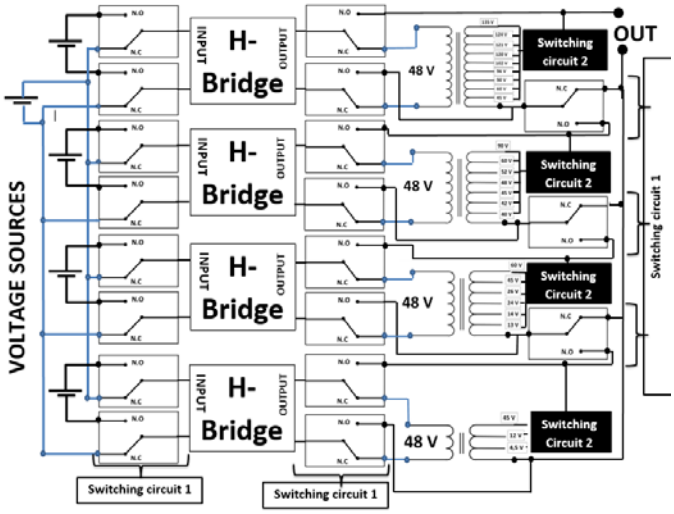


Fig. 12. Electrical diagram of the modular converter.

Table I. Experiment Results

H-bridges Numbers	Symmetrical	Asymmetrical	
		1:2	1:3
2	5	7	9
3	7	15	27
4	9	31	81

The system provides the RMS levels in the single DC source sub-topology for configurations with a number of levels equal to the maximum of the H-bridges.

5.2 Communication stages

In order to commute the connections of the circuit's bridges, there are essentially two switching circuits. The first is responsible for making power connections and is made up of the switches shown in the electronic diagram of Figure 12. Its function is to connect the H-bridge inputs and outputs of.

At the input, it is necessary to select the type of supply of the H-bridges, whether that be an isolated voltage source per bridge or that all H-bridges are connected to a single voltage source. At the output, it is necessary to select the connection or de-connection of the transformers in agreement with the number of bridges. Additionally at the output, it is necessary to cascaded connect the output of the H-bridges or the transformers' secondary windings.

The second circuit is responsible for selecting the necessary transformer derivation to obtain the voltage values of the asymmetry selected and maintain the waveform and the RMS level of the output voltage. This

works only in single DC source configuration. There is an extra circuit that functions simultaneously with the first and is responsible for connecting the control of the H-bridges in an equal configuration to the level of power of the implemented circuits shown in Fig. 13.

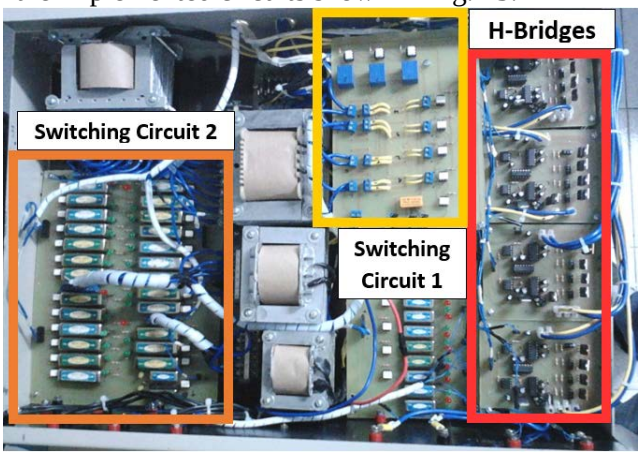


Fig. 13. Configurable converter prototype.

5.3 Platform

The hardware of the scalable converter is shown in Figure 14. This prototype consists of four H-bridges, four transformers and 32 relays that allow the configuration of deferential sub-topologies. The control was developed through an algorithm in Matlab® and the use of a FPGA XUPV5-LX110T, allowing for the adjustment of the converter in order to obtain a single DC or separate DC source inverter. With 1 to 4 stages reaching modulations between 3 and 81 levels with step modulations and PWM, the transformers are designed with an specific methodology.

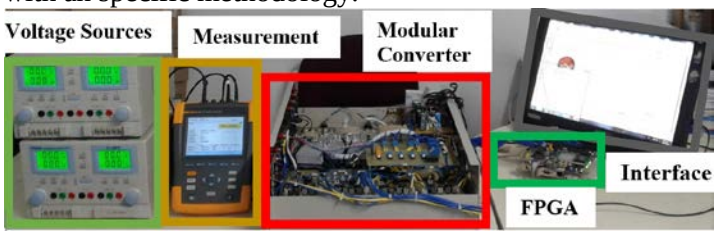


Fig. 14. Experimental setup.

5.4 Communication

The general diagram of communication for implementation is shown in Figure 15. The characteristics of connection and drive control are coded in order to be sent to the visual interface in an organized way, and then to be sent to the FPGA via the RS-232 protocol. The FPGA decodes the information and sends it to the conditioning circuits which provide the precise values in terms of magnitude and time in order to commute the relays and transistors.

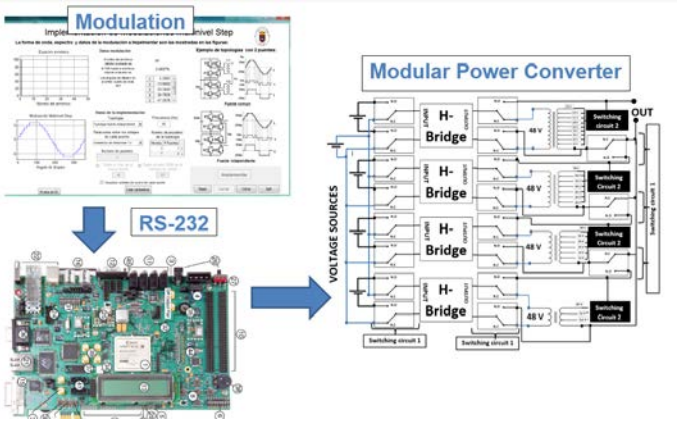


Fig. 15. Overall diagram of the implementation process.

The FPGA was programmed in VHDL in such a way that it codifies the information and sends the switching signals to the conditioning circuits. For the reception of the data, the UART (Universal Asynchronous Receiver-Transmitter) is used to receive values with an input bit, 8 databits and a stop bit. In the process, FIFO buffers are used to verify the data at a rate of 16X and a speed of transfers of 115200 bauds.

The oscillator clock used in the FPGA is 100Mhz. The information received is decoded and converted into 42 control signals.

The modulations of the H-bridges at steady state are 6 signals. The remaining 36 signals corresponding to the drive pulses for the switching circuits of the multilevel converter.

6. Functionality Tests

6.1 Optimization

To demonstrate the functioning of the platform it is necessary to begin with the optimization of a modulation in the interface. The selected modulation has nine levels and its waveform is shown in Figure 6 along with the harmonic content which shows the optimization as having a THDv of 7.62%. The shooting angles are shown in the simulation interface in Figure 16, matched the optimized switching angles generated by the optimization process.

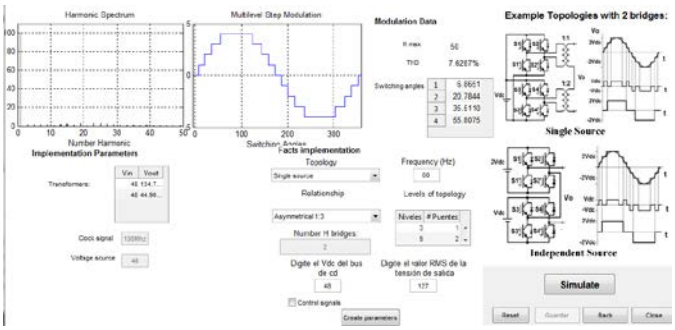


Fig. 16. Simulation interface.

To test, the sub-topology selected is the single DC source, in a configuration of asymmetric 1:3, for which two H-bridges are required, the value of the DC-bus is 48 volts and current RMS AC 127V output value is expected, the transformers outputs of the H-bridges are 134.7V and 44.9 V RMS values.

6.2 Simulation

In the simulation, physical characteristics of the converter are selected to be implemented as shown in Figure 14. For this test, the election is the single DC source sub-topology with output asymmetry of 1:3, for which the use of two H-bridges is required. The converter scheme in Simulink is shown in Figure 17, in which can be observe the hardware configuration specified in Figure 16.

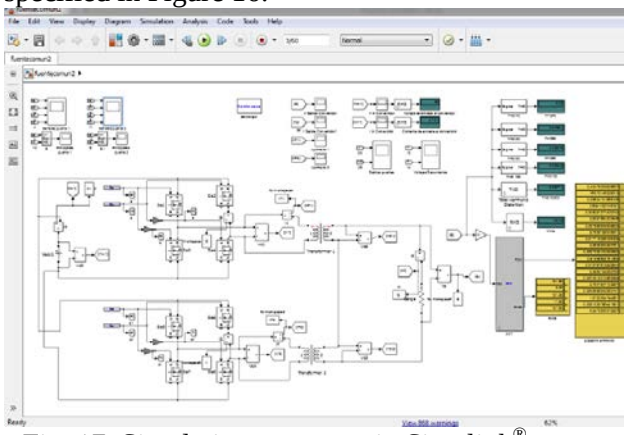
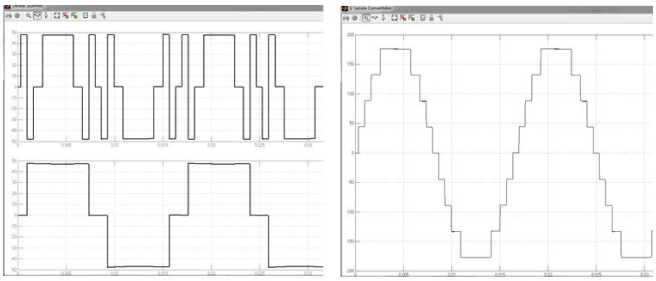


Fig. 17. Simulation converter in Simulink®.

The output of each of the H-bridges is presented in Figure 18a and the addition of the two that correspond to the output of the multilevel converter simulated in Figure 18b, in which can be observe that it match precisely with the theoretical waveform.



a) b)

Fig. 18. Voltage generation. a) At each H-bridges b) Output.

Implementation of the no load test

The converter implemented uses only two H-bridges of the platform, each one connected to a transformer output. The transformation relationships are of 48/127.2V and of 48/42.42V, calculated in the interface and selected by the second circuit of the switching circuit. In this way, the prototype must be powered by a source of direct current of 48 volts and the result is an alternating voltage waveform with a 170 volt peak. The converter rated power is limited by the transformers design, having 200 VA. The measurements shows that the Figure 19 were obtained by the Fluke 434 series II network analyzer set to a fundamental frequency of 60 Hz and to display the first 50 harmonics.

The waveform is shown in Figure 19, in which one can note the correspondence of the waveform and the theoretical wavelength.

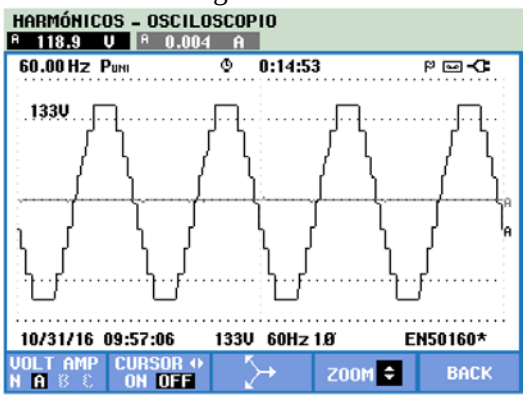


Fig. 19. Step modulation voltage waveform.

The harmonic spectrum and THDv of the modulation implemented correspond to the theoretical value of the theoretically optimized modulation, as observed in Figure 20.

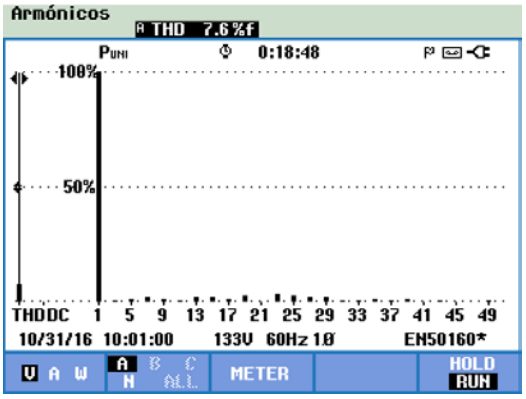
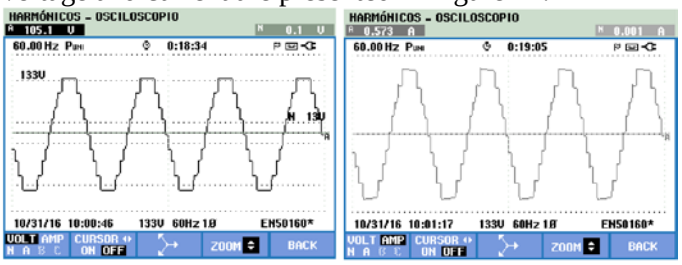


Fig. 20. Step modulation harmonic spectrum.

The vacuum test shows that the THDv of the converter's output is exactly equal to the value of the THDv of the theoretically calculated modulation, which validates the correct functioning of the platform, and show its versatility.

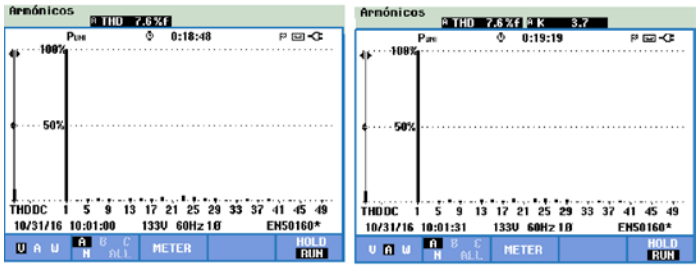
Implementation of charge resistive testing

The waveforms obtained with a resistive load of 60W are presented in Figure 21. The harmonic spectra of voltage and current are presented in Figure 22.



a) b)

Fig. 21. Resistive load waveform. a) Voltage. b) Current.



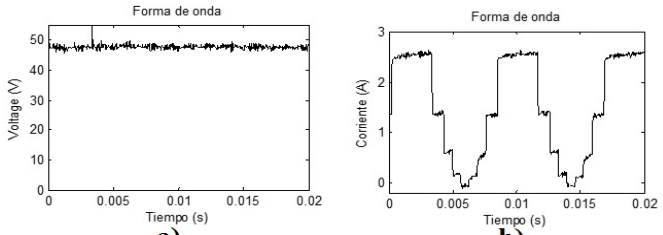
a) b)

Fig. 22. Resistive load harmonic spectrum. a) Voltage. b) Current.

6.3 DC bus

To acquire the voltage, the Fluke TP 120 sensor was used. For the current waveform, the Fluke 801-110s sensor was used and via the DAQ card of the National Instrument NI6211, the data acquisition software used was Matlab® at a rate of 48 Ksamples/s.

In figure 23, one can see the current and DC bus voltage waveforms of each converter using the scalable modulation.



a) b)

Fig. 23. DC buses with scalable modulation. a) Voltage and b) Current of the DC bus of the single DC source converter

Output variables

The measured output variables are shown in Table 2. The THD of the nine level single DC source converter along with the power values in order to estimate the efficiency. The result of the vacuum test differs subtly from the charge test, in which the THDv increases.

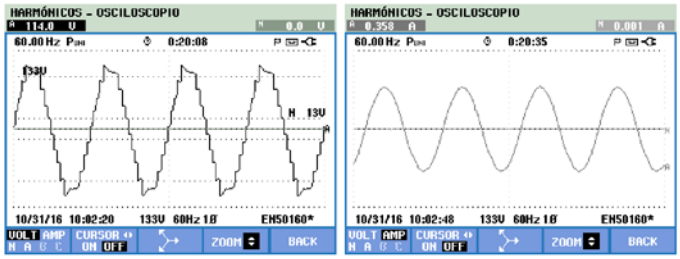
Table 2. Table of Experiment Results

Modulation	Test	Parameter	Single DC Source
Step	No Load	RMS Voltage	118.9 V
		THDv	7.6%
	Load	RMS Voltage	105.1 V
		RMS current	0.571 A
		Output Power	60.01 W
		THDv	7.6%
		THDi	7.6%
		Input Power	70.192 W

The scalable modulation (step) demonstrates a greater efficiency due to lower losses as a result of the commutation of the converter.

6.4 Inductive load implementation

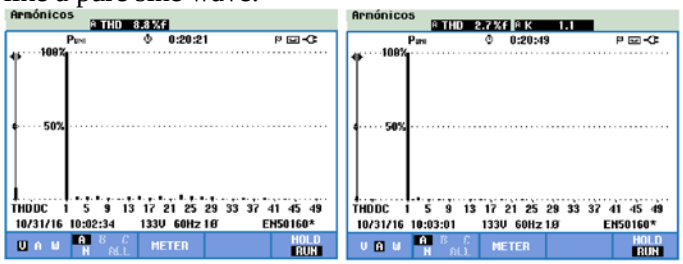
A test with inductive load is shown in Figure 24. Appreciating the effects of the inductive load to the voltage waveform and the drastic changes in the current waveform affecting harmonic content, voltage regulation and efficiency.



a) b)

Fig. 24. Inductive load waveform. a) Voltage. b) Current.

The effects of inductive load directly affect the voltage waveform and impact the harmonic spectra and harmonic content, raising the distortion of the voltage to deform the waveform and also reducing current distortion by filtering the waveform and make it more like a pure sine wave.



a) b)

Fig. 25. Inductive load harmonic spectrum. a) Voltage. b) Current.

7. Conclusions

The flexibility of the platform of investigation of cascaded multilevel converters permits one to obtain in a matter of seconds the relevant electrical parameters of the single DC and separate DC source sub-topologies in symmetrical and asymmetrical configurations, validated by a precise implementation in the hardware, thus facilitating the comparison of the sub-topologies' functionalities in terms of energy quality and efficiency.

The THDv obtained in the practice is exactly equal to that which was calculated theoretically, validating the successful functionality of the switching circuits, the system communication, the optimization process, the functioning of the H-bridges - in general terms, the adequate functioning of the platform. Considering that the measuring instrument is regulated by the IEEE 519, the THDv is therefore calculated considering the first 50 harmonics, and so the optimization carried out is up to the 50th harmonic and the resulting error is insignificant.

The feasible possibilities of converters with the aim of carrying out a thorough practical study are extremely vast, and they increase with the implementation of PWM modulations. This doubles the number of converters in analyzing their behavior with Step modulations and optimized PWM.

The visual interface facilitates the use of the modular power converter as, in practice; one only has to input the converter's data and closely follow the instructions.

The process of functional optimization and the versatility of creating modulations in a simple way and then implementing them deeply, facilitated by the obtaining of the relevant electronic parameters means that the platform is a powerful tool that aims to analyze, both theoretically and practically, the single DC and separate DC source sub-topologies in a range of 5 to 81 voltage levels.

The tests demonstrate the right use of parameters analysis and behavior of relevant variables of the converter. At the end, confirms the advantages of using the cascaded multilevel power converter.

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