Advancing in-memory arithmetic based on CMOS-integrable memristive crossbar structures

EIKE LINN
Institut für Werkstoffe der Elektrotechnik II
RWTH Aachen University
Sommerfeldstr. 24, D-52074 Aachen
GERMANY

HEIDEMARIE SCHMIDT
Department of Materials for Nanoelectronics
Technische Universität Chemnitz, Nano-Spintronics group
Reichenhainer Str, 39, D-09126 Chemnitz
GERMANY

Abstract: - Memristive computing will be advantageous in large-scale, highly parallel mixed-mode processing architectures because processing can be performed directly within memristive memory architectures and intra-chip communication can be implemented by a memristive crossbar structure with reconfigurable logic gates. Here we report on the development of a new concept for in-memory adders, using XOR functionality. Exploited memristive crossbar structures are based on memristive complementary resistive switches, e.g. TaO_x, and $BiFeO_3$.

Key-Words: - Silicon Devices, Thin Film Technologies, Logic Synthesis, Data storage, In-Memory Logics, Fast Algorithms, Neural Networks, Artificial Intelligence, Numerical Analysis and Circuits, System architecture

1 Introduction

For today's data-intensive applications, the data storage and processing is becoming more and more challenging due to the ongoing increase of data volume [1]. Especially big data problems such as genome decoding require analysis of large data sets stored in memory. According to the ITRS roadmap there are several emerging non-volatile memory technologies which could ease the data storage issue [2]. Particularly redox-based resistive switches (ReRAMs) [3, 4], also called memristive devices or memristors for short [5-7], are among the most promising candidates as future ultimately scaled $4F^2$ memories (F: feature size). Most ReRAM devices offer filament-type switching behavior, but some materials, especially perovskites, show interface-type switching [8-11]. The advantage of interface-type switching materials is that both resistive states, the high resistance state (HRS) and the low resistance state (LRS), scale with the feature size F. Moreover, memristive devices enable basic in-memory logic operations [12]. Therefore, they supersede the separation of arithmetic logic unit (ALU) and memory, which is present in common von-Neumann computer architectures [13]. The avoidance of memory-accesses in combination with the feasibility of massive parallel computations makes memristive crossbar array-based architectures highly attractive for future energy-efficient data-intensive processing units [14, 15]. To avoid parasitic currents in passive crossbar array architectures, typically a two-terminal selector device is required [16]. Alternatively, two anti-serially connected cells, a complementary resistive switch (CRS) [17] or a device offering inherent selector mechanism can be applied. There are several types of devices which offer either (1) inherent non-linear branches (NL) [18], (2) inherent threshold switching behavior (TS) [19], (3) complementary switching (CS) [20] or (4) flexible barrier switching (FBS) [21]. The use of FBS cells combines two advantages: First, those devices are

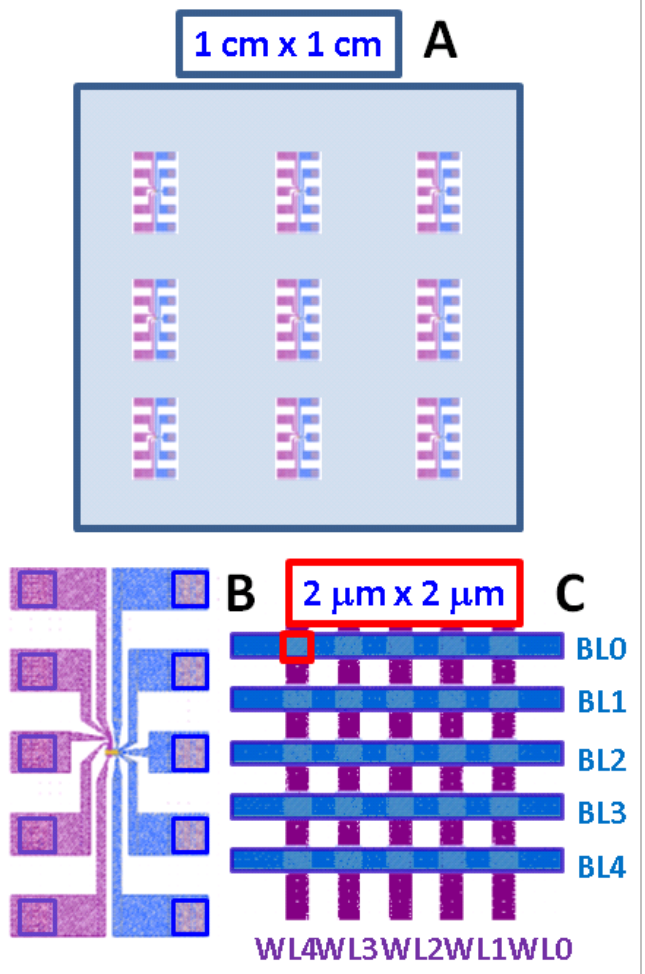

Fig. 1 (A) Chip overview (1 cm x 1 cm), (B) Single 5x5 crossbar array with 25 $BiFeO_3$ FBS devices, (C) Mask level for Ti^+ implantation and/or Ar^+ irradiation on cross points before deposition of top electrodes (bitlines).

energy-efficient [22], offer excellent scaling properties due the area-dependent resistance [23], and second, enable non-destructive read-out procedures. The first sequential logic concept using memristive devices was proposed by Borghetti *et al.* [24] requiring several devices and multiple steps while crossbar array compatibility is limited [25]. An advanced concept enables 14 out of 16 Boolean logic functions with a single device and is suitable for CRS cells [13]. Recently, a further enhanced concept which enables all 16 Boolean functions with a single device was presented in [12]. This approach is suitable for FBS cells and CRS cells [46]. Boolean logic functions can be used to make binary arithmetics, namely adders, subtractors, multipliers, and dividers. For example, a binary adder is a logic unit which produces the sum of two binary numbers. In many computers the adder is not only used in the ALU but also in other parts of the processor, where adders are used to calculate addresses, table indices, and similar operations. There are several in-memory-adder concepts available: (1) the adder concept proposed by Lehtonen *et al.* using the basic IMPLY logic [26], (2) an optimized serial adder suggested by Kvatinsky *et al.* [27] (both using 1R devices) and (3) a sequential adder based on the CRS logic [28]. In this work we will show how in-memory adders based on XOR-functionality can be realized based on $BiFeO_3$ and CRS crossbar arrays, respectively. As a rule of thumb it can be noted that device concepts can be simplified the more Boolean logic functions can be realized bythe memristive device. The paper is structured as follows: In Sect. 2 we discuss fabrication of memristive devices and of memristive modelling. In Sect. 3 we discuss implementation of in-memory logic functionality in memristive switches with flexible barriers and filamentary switching. Finally, we compare the functionality of the recently introduced toggle cell adder [28] and of the novel XOR-based in-memory adder in terms of cycle count and area consumption. The paper closes with a summary and outlook.

2 Device concept

In the following we discuss the realization of novel XOR-basedin-memory adders using FBS. For example, one or a 5 x 5 crossbar arrays (Fig. 1) with memristive (=nonvolatile +resistive) $BiFeO_3$ switching cells on CMOS-compatible electrodes, e.g. on TiN and TaN can be used. $BiFeO_3$ can be deposited by two deposition techniques with a different temperature gradient and corresponding different Ti diffusion during the $BiFeO_3$ thin film growth, namely by pulsed laser deposition and by magnetron sputtering. In addition to the temperature gradient during the $BiFeO_3$ thin film growth, the profile of fixed Ti^+ donors is controlled by a local Ti^+ ion implantation into the CMOS compatible bottom electrode. The profile of mobile oxygen

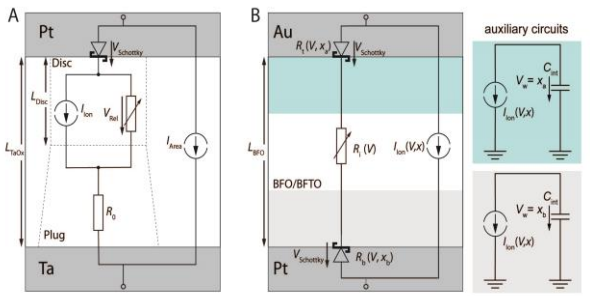

Fig. 2 (A) Equivalent circuit model of a TaO_x resistive switching device. The auxiliary circuit for the state variable calculation (mean oxygen vacancy concentration at the upper interface) is not shown. [38] (B) Equivalent circuit model of a $BiFeO_3$ FBS cell. Each interface is a state variable dependent Schottky diode. The bulk region is a state variable independent region. The oxygen vacancy concentration at the interfaces is calculated in auxiliary circuits points before deposition of top electrodes (bitlines).

vacancies is controlled by the ambient pressure and substrate temperature during $BiFeO_3$ thin film growth and by Ar^+ ion irradiation. For implementation of accurate memristive models of ReRAM devices a sound physical picture of the device and a wide range of experimental data covering both the quasi-static I-V characteristic as well as dynamic behavior is needed. Possible physical mechanisms for each device region have to be identified to derive corresponding transport equations. This approach will enable the realization of a generic device model. Later data from electrical characterization will be used to decide which of the feasible mechanisms is able to describe the measurement data best. Finally, the best model parameters can be extracted and incorporated into the circuit model (Fig. 2). Another issue for nanoscale memristive devices is the device variability. To check for the validity of the model, multi-element simulation have to be conducted. Based on a generic device model the energy consumption can be estimated. In this work we present the device concept only and compare existing ECM-CRS, VCM-CRS, and selector-based (1S1R) adder implementation with the new $BiFeO_3$ in-memory adder qualitatively. Finally, we will give a quantitative analysis of the resulting cycle count and device count.

3 Memristive crossbar structures

3.1 In-memory logic functionality using non-volatile resistive switches

Redox-based bipolar resistive switches (BRSs) can be either electrochemical metallization (ECM) cells or valence change mechanism (VCM) devices [3]. ECM cells offer filamentary switching, whereas VCM cells either offer flexible barrier switching (FBS) [12] (Fig. 3 A, B) or filamentary switching [17] (Fig. 3 C, D). For BRS cells in general a serial selector is required to reduce parasitic current paths, whereas for some FBS devices the inherent non-linearity of the low resistive current branch is sufficient to suppress parasitic currents. Especially the $BiFeO_3$-based FBS cells offer good selectivity, high endurance, and retention [29-31]. Two-layer $BiFeO_3$ memristors offer two complementary pairs of storing states (PHRS/NLRS and PLRS/NHRS) which can be accessed by positive or negative voltage write voltages, respectively (Fig. 3 A,B). Since the current characteristic in each state is polarity dependent both storage states are distinguishable, enabling a non-destructive read-out of this device. Furthermore, for area dependent switching properties the total current scales with the feature size [23], thus low power operations will be realizable for small feature sizes F [22]. As the resistive switching in $BiFeO_3$ FBS cells is electroforming-free and analog, we could perform memristance measurements [32], develop a new hardware-based cryptography approach [33], and reveal spike-timing dependent plasticity [34]. For filamentary ECM and VCM devices there is another option to avoid sneak paths: the anti-serial connection of two devices, called complementary resistive switch (CRS). In Fig. 3 C a ECM-type CRS cell is depicted. This cell consists of Pt top and bottom electrodes, a Cu middle electrode and solid

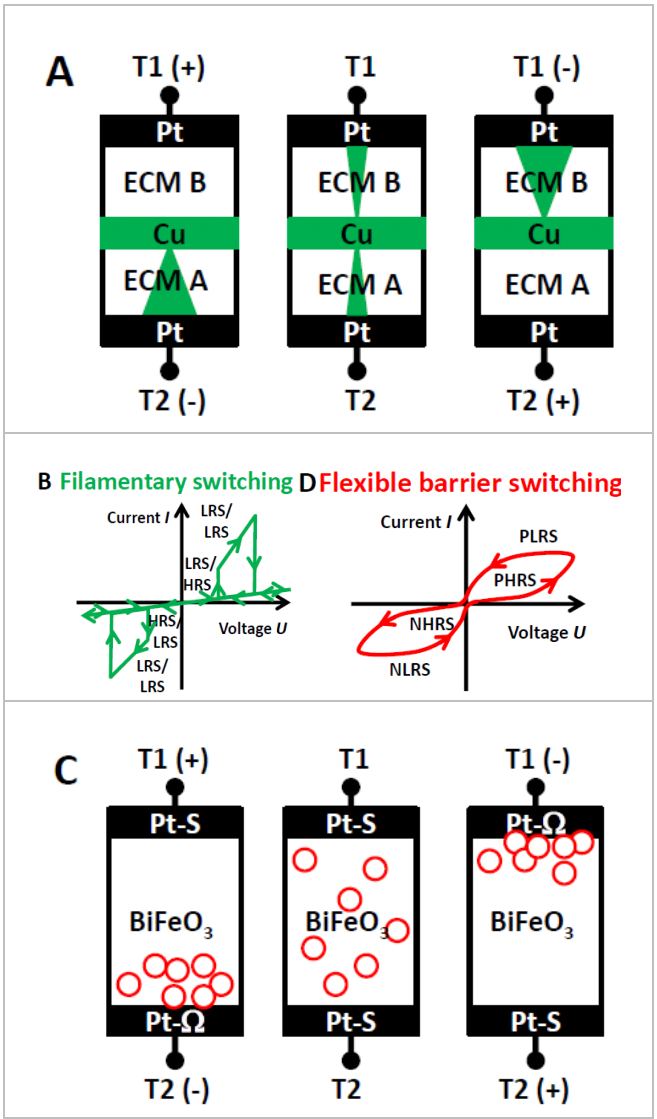

Fig. 3 (A) Equivalent circuit model of a TaOx resistive switching device. The auxiliary circuit for the state variable calculation (mean oxygen vacancy concentration at the upper interface) is not shown. [38] (B) Equivalent circuit model of a BiFeO3 FBS cell. Each interface is a state variable dependent Schottky diode. The bulk region is a state variable independent region. The oxygen vacancy concentration at the interfaces is calculated in auxiliary circuits points before deposition of top electrodes (bitlines).

electrolyte, e.g. GeS, in between the electrodes. The device offers two storing states (HRS/LRS and LRS/HRS) and a third state (LRS/LRS) which is only accessed during read operation. Since both storing states are overall high resistive, CRS cells offer an inherent selector mechanism [17, 35-36]. In terms of logic in-memory operation according to [13], each device can be considered a finite state machine offering two states: LRS (Z = '1') und HRS (Z = '0') (BRS cell), HRS/LRS (Z = '1') and LRS/HRS (Z = '0') (CRS cell) cf Fig. 3 D. For the logic operation input voltages $|V_{logic}|$ larger than the given threshold voltage $|V_{th}|$ are needed. By applying the input voltages ($+|V_{logic}|/2$ ('1') or $-|V_{logic}|/2$ ('0')) to the terminals T1 and T2, the logic operation is conducted. The result is directly stored as the memory state Z. It is important to note that the previous state Z_{prev} can be considered as a third input variable to the logic function. For realizing an adder with RIMP and NIMP logic operations (Fig. 4), the new state is calculated as follows [13]:

$$Z = (\mathrm{T1\ RIMP\ T2})\,Z_{prev} + (\mathrm{T1\ NIMP\ T2})\,\overline{Z_{prev}} \qquad (1)$$

The logic operation p RIMP q is exemplarily described in the following (Fig. 2 A). First, the device is initialized to state Z_{prev} = '1' by applying '1' to terminal T1 and '0' to terminal T2. Next, the variable p is applied to terminal T1 and q is applied to terminal T2:

$$Z = (\mathrm{p\ RIMP\ q}) \cdot `1' = \mathrm{p\ RIMP\ q} \qquad (2)$$

After this operation the final result is stored as resistive state in Z and no further step is required. Using for example ECM-CRS cells the TRUE and FALSE operations require only one configuration step, whereas p IMP q, p RIMP q, p NIMP q, p RNIMP q, p, q, NOT p, NOT q require two configuration steps. The functions p AND q, p NAND q, p OR q, p NOR q require three configuration steps [13]. For direct implementation of p XOR q and p XNOR q a second device would be needed in this approach. In the second concept according to [12], each logic operation using $BiFeO_3$ devices requires two configuration steps. The final read-out polarity r (marked by grey color in Fig. 4 A, B) is operation and input dependent. r = 1 corresponds to a positive readout voltage, whereas r = 0 corresponds to a negative readout voltage. The RIMP functionality using this approach is exemplified in Fig. 4 B. In this concept, the read output corresponds to this general logic function:

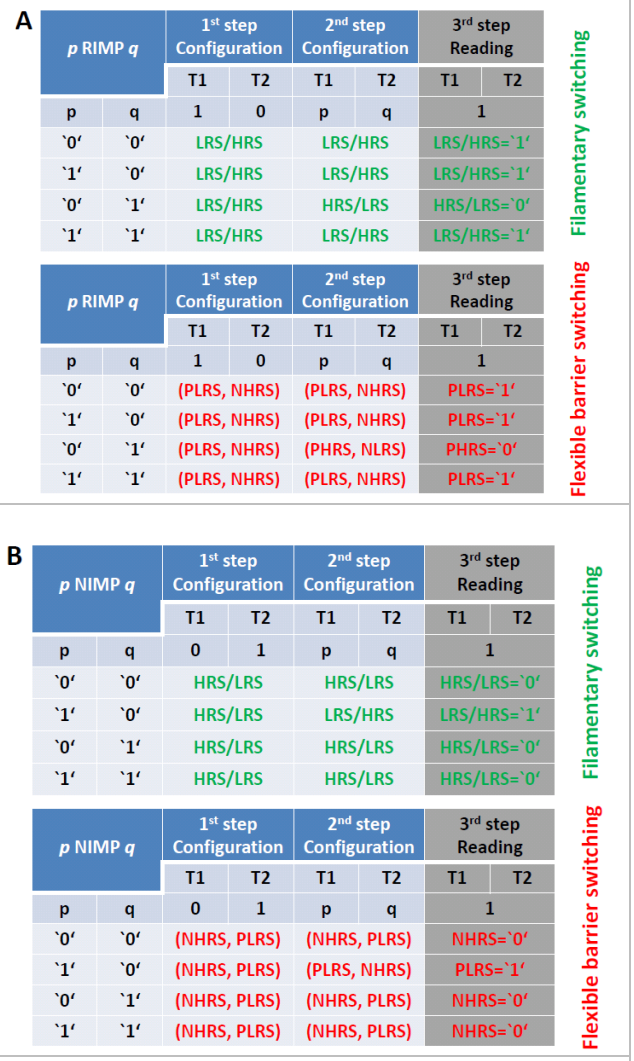

Fig. 4 Realization of the logic function (A) p RIMP q and (B) p NIMP q using ECM-CRS (resistance states in green color) and $BiFeO_3$ (resistance states in red color) devices. In a 1st step the initialization takes place. In a 2nd step the logic operation is performed and the result is stored as resistive state in the ECM-CRS and $BiFeO_3$ device [12, 13]. If a variable read-out operation (for RIMP and NIMP: r = 1) is conducted as part of the logic operation, all 16 Boolean functions can be realized with a single device (third step marked by grey color) [1].

$$\text{Out} = \left((\text{T1 RIMP T2})Z_{\text{prev}} + (\text{T1 NIMP T2})\overline{Z_{\text{prev}}}\right)\cdot \text{r} + \ldots$$
$$\ldots + \overline{\left((\text{T1 RIMP T2})Z_{\text{prev}} + (\text{T1 NIMP T2})\overline{Z_{\text{prev}}}\right)}\cdot \bar{\text{r}} \quad (3)$$

For p RIMP q, the device is first initialized to Zprev = '1'. Then, the second step of the logic operation is conducted. Finally, the read-out is conducted, using r = 1 for the RIMP function. Thus, the equation simplifies to:

$$\text{Out} = ((\text{p RIMP q})\cdot \text{´1`})\cdot \text{´1`} = \text{p RIMP q} \quad (4)$$

The concept according to [13] was first verified by means of memristive simulation for both ECM-type [25, 37] and VCM-type devices [38, 39]. Next, the experimental verification was done for TaOx-based VCM-type CRS in quasi-static and pulse mode [39]. The second concept was introduced and experimentally verified by means of FBS devices in [12]. The feasibility of all 16 Boolean functions with a single device was revealed there. In [46] it was shown that the FBS approach using a conditional readout can be also adopted to CS and CRS devices. However, it has to be noted that the read-out destroys the state of ECM-CRS cells and necessitates a write-back step.

3.2 Developing adders using RIMP and NIMP functionality

Using the elementary logic concept from Ref. [13], more complex logic functions can be realized. In [28] a CRS-based sequential in-memory adder was proposed. There, the calculation is performed in one wordline of a n x n passive crossbar array. In the crossbar array configuration, each device is connected to a wordline WL (terminal T1) and a bitline BL (terminal T2). In Fig. 5 A a corresponding $4F^2$ passive crossbar array consisting either of ECM-CRS or $BiFeO_3$ FBS devices is depicted. To enable in-memory adders in passive crossbar arrays, the available array size is a very important value, since the ratio between the size of the control logic and the array size will decrease with increasing array size (Fig. 5 B). In this respect the use of $BiFeO_3$ devices offering an inherent select mechanism is highly attractive, since $BiFeO_3$ devices are expected to enable large and scalable crossbar arrays.

To realize the adder functionality, the wordline is initialized to the input carry c0 first (Fig. 6). Next,

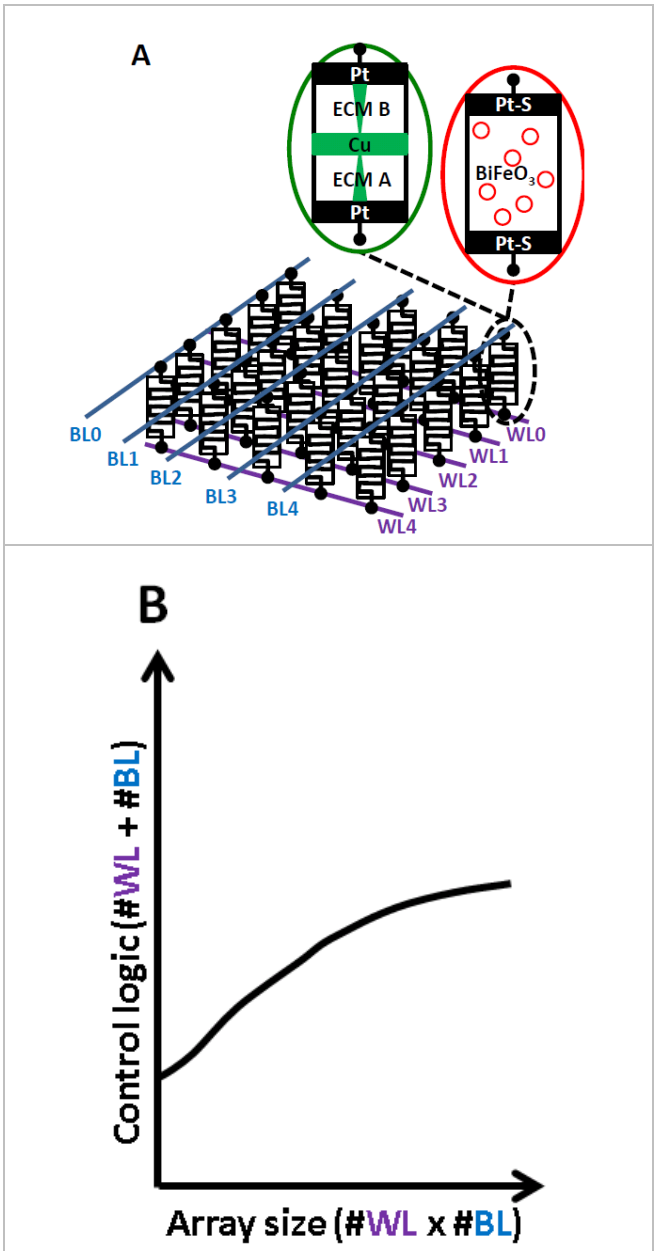

Fig. 5 (A) Schematic representation of logic gates on an array structure with 5 wordlines WL and 5 bitlines BL. The logic gates ECM-CRS devices (green circle) or $BiFeO_3$ FBS devices (red circle) (s. a. Fig. 3). (B) The size of the control logic depends on the sum of wordlines and bitlines (#WL + # BL), whereas the array size scales with the product between wordlines and bitlines (#WL x # BL). Larger array structures will have much smaller control logics in comparison to the array structure size. Adapted from [1].

the carry of the next significance (c1) is calculated in only one step. The calculation of the sum bit (si) requires two steps. These steps are repeated for each significance 0 to N. Note, to enable the final sum calculation, the value of ci+1 has to be read-out prior to this operation. For CRS devices this requires a destructive read-out and subsequent writeback (Toggle Cell (TC)-adder approach) or a second wordline performing the auxiliary calculation of the carries (PreCalculation (PC)-adder approach). The complete cycle flow graph implementing the TC-adder functionality is depicted in Fig. 6. From this flow graph one can see that the number of cycles increases linearly with the bit width of the input operands. The CRS-based adders according to [28] require 4N+5 cycles (TC-adder) and 2(N+1)+2 cycles (PC-adder), whereas earlier adder implementations require 89N [26] or 29N cycles [27]. Moreover, also the device count for the CRS-based adders [28], which is directly connected to the required memory area, is less than in the previous adder implementations.

By using FBS devices the number of cycles can be further reduced since no writeback steps are required, as shown also for 1S1R devices recently [47]. Moreover, by using the logic paradigm introduced in [12] also adder implementations requiring less switching cells are feasible.

3.3 Developing adders using XOR functionality

Two different in-memory adder concepts, one using RIMP and NIMP functionality and the other using XOR functionality can be exploited using memristive 5x5 crossbar arrays. In the following we wish to show how in-memory adders can be implemented in CMOS-compatible array structures (Fig. 5) using memristive switching $BiFeO_3$ cells with XOR functionality, e.g. in single wordlines of $BiFeO_3$ 5 x 5 crossbar arrays. In Sect. 3.2 we have shown how in-memory adders can be realized with RIMP and NIMP functionality. According to the logic concept introduced in [12] also XOR functionality is available in $BiFeO_3$ FBS devices. Therefore, we have explored in-memory adders with XOR functionalities. In contrast to the previously considered adder concept, the read-out in the alternative adder concept is part of the logic operation. Thus the number of read-out steps increases. On the other hand, the number of required

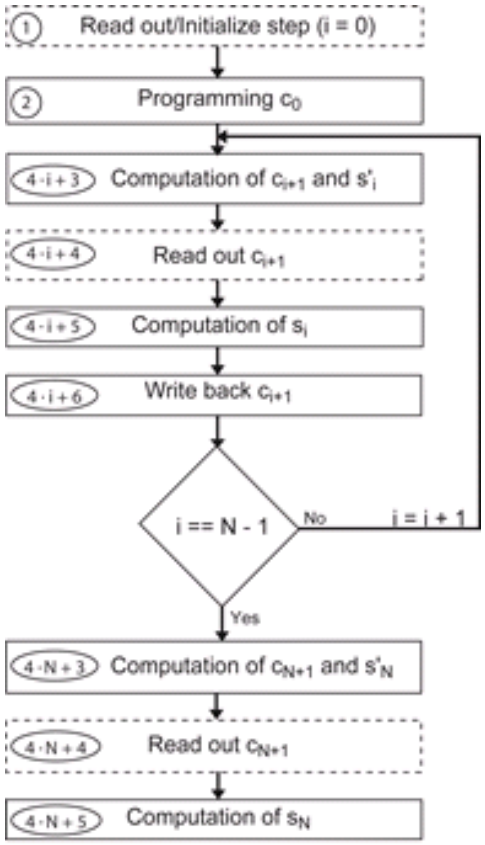

Fig. 6 Cycle flow graph of the TC-adder. The first step is the initialization step. In the second step, the c0 carry is programmed to the cells. In case c0 = 0 a common addition is carried out. In case c0 = 1 a subtraction using two's complement method is enabled. Note that in this case the second operand is inverted. The next four steps are performed in a loop for N-1 times, where N is the bit width of the operands. First, the carry of the next significance and the preliminary sum are calculated. Next, the carry is read, and the sum bit is calculated. In case of the destructive read-out in ECM-CRS devices, a write-back step is required. Note, that for $BiFeO_3$ FBS devices this step is not required. Finally, carry of significance N+1 and the sum bit N are calculated. In case of subtraction using two's complement method, the carry of significance N+1 is discarded. From [28].

devices can be reduced in comparison to the PC-adder. Without introducing any kind of optimization a maximum number of 7N+1 steps is required to perform the addition (Fig. 7 B). The first step is the initialization step. In the second step, the c0 carry is programmed to the cells. In the case c0 = 0 a common addition is carried out. In case of c0 = 1 a subtraction using two's complement is enabled. Note that in this case the second operand is inverted. The next four steps are performed in a loop for N-1 times, where N is the bit width of the operands. First, the carry of the next significance and the preliminary sum are calculated. Next, the carry is read, and the sum bit is calculated. In case of the destructive read-out in ECM-CRS devices, a write-back step is required. Note, that for $BiFeO_3$ FBS devices this step is not required.

4 Conclusions and outlook

We have developed a new in-memory adder concept using XOR functionality and compared it to recently introduced PC and TC adders based on RIMP and NIMP functionality. For that we exploited the functionality of memristive crossbar array structures with $BiFeO_3$ FBS cells or ECM-CRS cells, respectively.. The number of arithmetic cycles increases linearly with the bit width of the input operands. Without introducing any kind of optimization a maximum number of 7N+1 steps is required to perform the in-memory addition with $BiFeO_3$ FBS cells. For CRS devices addition requires a destructive read-out and subsequent writeback (compare Toggle Cell (TC)-adder approach) or a second wordline performing the auxiliary calculation of the carries (compare Pre-Calculation (PC)-adder approach). The initial CRS-based adders require 4N+5 cycles (TC-adder) and 2(N+1)+2 cycles (PC-adder), whereas earlier adder implementations require 89N [26] or 29N cycles [27]. The most relevant metrics are energy per operation, cycle count and device count, i.e. crossbar array size. However, so far we excluded the comparison of overall hybrid CMOS/crossbar array system to an all-CMOS implementation, since one would need to implement all the CMOS parts in a current technology to obtain accurate performance values. In the future we will develop concepts for in-memory subtractors, multipliers and dividers, too. Furthermore, we plan to investigate how functionality, variability, and parasitic effects in overall hybrid CMOS/crossbar arrays can be controlled by exploiting the novel transport

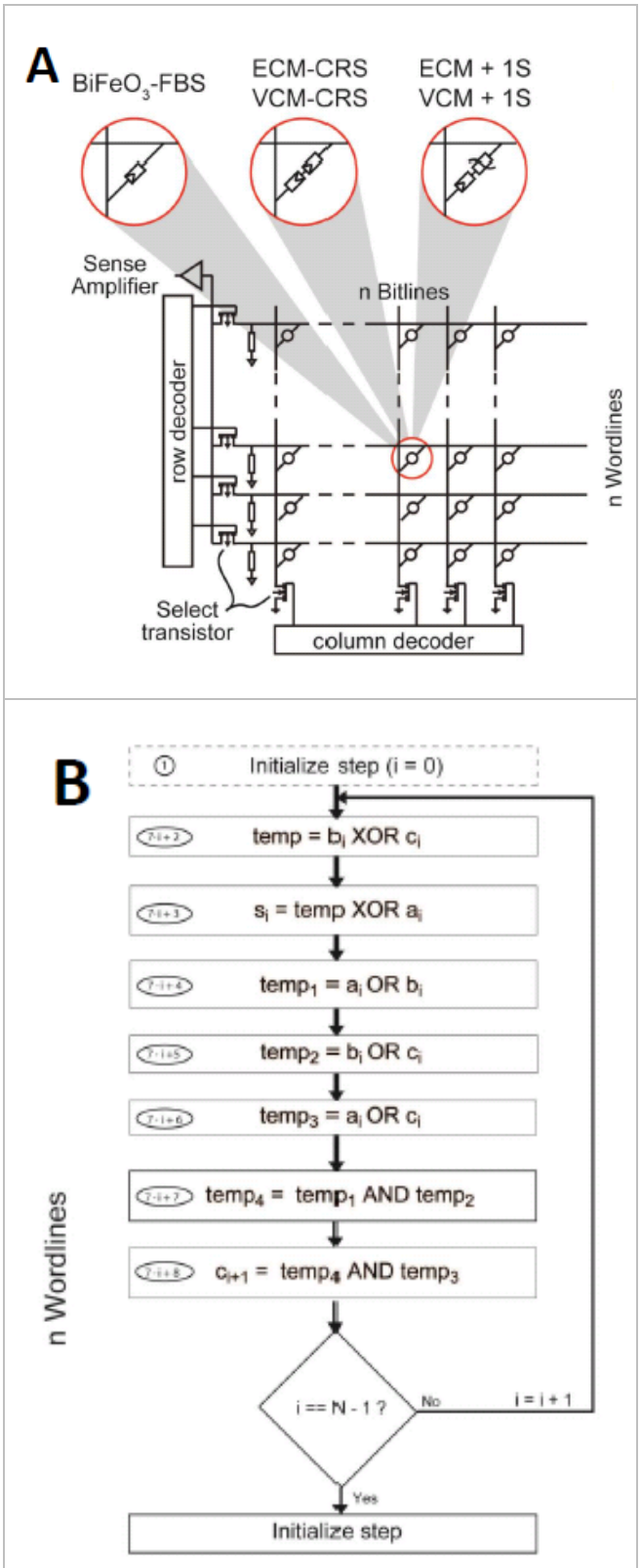

Fig. 13 (A) Schematic sketch of an in-memory adder based on crossbar arrays with different cells, namely $BiFeO_3$ FBS cells, ECM-CRS und VCM-CRS cells, and ECM+1S and VCM+1S cells. (B) Cycle flow graph of an in-memory XOR-adder based on single wordlines in crossbar arrays with $BiFeO_3$ cells.

properties in $BiFeO_3$–type memristive switching cells.

Acknowledgments: We are indebted to Nan Du, Tiangui You, Damilo Bürger, and to Oliver G. Schmidt for fruitful discussions. Financial support by the Deutsche Forschungsgemeinschaft (SCHM 1663/4-1,2) and by the Initiative and Networking Fund of the Helmholtz Association (VH-VI-422) made this work possible.

References:

[1]. H. Schmidt, T. Mikolajick, R. Waser, and E. Linn, Neuartige, lernfähige Memristor-Logik: Big Data ohne Energiekollaps (invited), Physik in unserer Zeit, vol. 2, 2015, pp. 84-89.

[2]. IITRS - The International Technology Roadmap for Semiconductors, Edition 2013, http://www.itrs.net/, 2013.

[3]. R. Waser, R. Dittmann, G. Staikov, and K. Szot, Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges, Adv. Mater., vol. 21, 2009, pp. 2632-2663.

[4]. J. J. Yang, D. B. Strukov, and D. R. Stewart, Memristive devices for computing, Nat. Nanotechnol., vol. 8, 2013, pp. 13-24.

[5]. L.O. Chua, Memristor-the missing circuit element, IEEE Trans. Circuit Theory, vol. CT-18, 1971, pp. 507-519.

[6]. L.O. Chua and S.M. Kang, Memristive devices and systems, Proc. IEEE, vol. 64, 1976, pp. 209-223.

[7]. D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, The missing memristor found, Nature, vol. 453, 2008, pp. 80-83.

[8]. A. Sawa, Resistive switching in transition metal oxides, Mater. Today, vol. 11, 2008, pp. 28-36.

[9]. R. Meyer, L. Schloss, J. Brewer, R. Lambertson, W. Kinney, J. Sanchez, and D. Rinerson, Oxide Dual-Layer Memory Element for Scalable Non-Volatile Cross-Point Memory Technology, Proc. NVMTS, 2008 pp. 54-58.

[10]. Y. Shuai, S. Zhou, S. Streit, H. Reuther, D. Bürger, S. Slesazeck, T. Mikolajick, M. Helm, and H. Schmidt, Reduced leakage current in $BiFeO_3$ thin films with rectifying contacts, Appl. Phys. Lett., vol. 98, 2011, pp. 232901.

[11]. Y. Shuai, X. Ou, C. Wu, W. Zhang, S. Zhou, D. Bürger, H. Reuther, S. Slesazeck, T. Mikolajick, M. Helm, and H. Schmidt, Substrate effect on the resistive switching in $BiFeO_3$ thin films, J. Appl. Phys., vol. 111, 2012, pp. 07D906.

[12]. T. You, Y. Shuai, W. Luo, N. Du, D. Bürger, I. Skorupa, R. Hübner, S. Henker, C. Mayr, R.

Schüffny, T. Mikolajick, O. G. Schmidt, and H. Schmidt, Exploiting Memristive BiFeO3 Bilayer Structures for Compact Sequential Logics, Advanced Functional Materials, vol. 24, 2014, pp. 3357-3365.

[13]. E. Linn, R. Rosezin, S. Tappertzhofen, U. Böttger, and R. Waser, Beyond von Neumann-logic operations in passive crossbar arrays alongside memory operations, Nanotechnology, vol. 23, 2012, pp. 305205.

[14]. M. Di Ventra and Y. V. Pershin, The parallel approach, Nat. Phys., vol. 9, 2013, pp. 200-202.

[15]. R. Waser, V. Rana, S. Menzel, and E. Linn, Energy-efficient Redox-based Non-Volatile Memory Devices and Logic Circuits, 3rd Berkeley Symposium on Energy Efficient Electronic Systems, 2013.

[16]. G. Burr, R. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, and H. Hwang, Access devices for 3D crosspoint memory, J. Vac. Sci. Technol. B, vol. 32, 2014, pp. 040802.

[17]. E. Linn, R. Rosezin, C. Kügeler, and R. Waser, Complementary Resistive Switches for Passive Nanocrossbar Memories, Nat. Mater., vol. 9, 2010, pp. 403-406.

[18]. A. Flocke, T.G. Noll, C. Kugeler, C. Nauenheim, and R. Waser, A fundamental analysis of nano-crossbars with non-linear switching materials and its impact on TiO_2 as a resistive layer, IEEE, 2008, pp. 319-322.

[19]. S. Kim, J. Park, J. Woo, C. Cho, W. Lee, J. Shin, G. Choi, S. Park, D. Lee, B. Lee, and H. Hwang, Threshold-switching characteristics of a nanothin-NbO_2-layer-based Pt/NbO_2/Pt stack for use in cross-point-type resistive memories, Microelectronic Engineering, vol. 107, 2013, pp. 33-36.

[20]. F. Nardi, S. Balatti, S. Larentis, D.C. Gilmer, and D. Ielmini, Complementary Switching in Oxide-Based Bipolar Resistive-Switching Random Memory, IEEE Trans. Electron Devices, vol. 60, 2013, pp. 70-77.

[21]. T. You, N. Du, S. Slesazeck, T. Mikolajick, G. Li, D. Bürger, I. Skorupa, H. Stöcker, B. Abendroth, A. Beyer, K. Volz, O. G. Schmidt, and H. Schmidt, Bipolar Electric-Field Enhanced Trapping and Detrapping of Mobile Donors in $BiFeO_3$ Memristors, ACS Applied Materials & Interfaces, vol. 6, 2014, pp. 19758-19765.

[22]. N. Du, M. Kiani, C. Mayr, R. Schüffny, T. You, D. Bürger, I. Skorupa, O. G. Schmidt, and H. Schmidt, One single pairing spike-timing dependent plasticity in multiferroic, low-power devices, Frontiers in Neuroscience: Neuromorphic Engineering, vol. 9, 2015, pp. 227.

[23]. L. Jin, Y. Shuai, X. Ou, P. F. Siles, H. Z. Zeng, T. You, N. Du, D. Bürger, I. Skorupa, S. Zhou, W. B. Luo, C. G. Wu, W. L. Zhang, T. Mikolajick, O. G. Schmidt, and H. Schmidt, Resistive switching in unstructured, polycrystalline $BiFeO_3$ thin films with downscaled electrodes, Physica Status Solidi A, vol. 211, 2014, pp. 2563-2568.

[24]. J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, Memristive' switches enable 'stateful' logic operations via material implication, Nature, vol. 464, 2010, pp. 873-876.

[25]. S. Ferch, E. Linn, R. Waser, and S. Menzel, Simulation and Comparison of two Sequential Logic-in-Memory Approaches Using a Dynamic Electrochemical Metallization Cell Model, Microelectronics Journal, vol. 45, 2014, pp. 1416-1428.

[26]. E. Lehtonen and M. Laiho, Stateful Implication Logic with Memristors, 2009 IEEE/ACM International Symposium on Nanoscale Architectures, 2009, pp. 33-36.#

[27]. S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, 2013, pp. 2054-2066.

[28]. A. Siemon, S. Menzel, R. Waser, and E. Linn, A Complementary Resistive Switch-based Crossbar Array Adder, accepted for IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), vol. 5, 2015, pp. 64-74.

[29]. X. Ou, Y. Shuai, W. Luo, P. F. Siles, R. Kögler, J. Fiedler, H. Reuther, S. Zhou, R. Hübner, S. Facsko, M. Helm, T. Mikolajick, O. G. Schmidt, and H. Schmidt, Forming-Free Resistive Switching in Multiferroic $BiFeO_3$ thin Films with Enhanced Nanoscale Shunts, ACS Applied Materials & Interfaces, vol. 5, 2013, pp. 12764-12771.

[30. Y. Shuai, X. Ou, W. Luo, A. Mücklich, D. Bürger, S. Zhou, C. Wu, Y. Chen, W. Zhang, M. Helm, T. Mikolajick, O. G. Schmidt, and H. Schmidt, Key concepts behind forming-free resistive switching incorporated with rectifying transport properties, Sci. Rep., vol. 3, 2013, pp. 2208.

[31]. Y. Shuai, X. Ou, W. Luo, N. Du, C. Wu, W. Zhang, D. Bürger, C. Mayr, R. Schüffny, S. Zhou, M. Helm, and H. Schmidt, Nonvolatile

Multilevel Resistive Switching in Ar^+ Irradiated $BiFeO_3$ Thin Films," IEEE Electron Device Lett., vol. 34, 2013, pp. 54-56.

[32]. N. Du, Y. Shuai, W. Luo, C. Mayr, R. Schüffny, O. G. Schmidt, and H. Schmidt, Practical guide for validated memristance measurements, Rev. Sci. Instrum., vol. 84, 2013, pp. 023903.

[33]. N. Du, N. Manjunath, Y. Shuai, D. Bürger, I. Skorupa, R. Schüffny, C. Mayr, D. N. Basov, M. Di Ventra, O. G. Schmidt, and H. Schmidt, Novel implementation of memristive systems for data encryption and obfuscation, J. Appl. Phys., vol. 115, 2014, pp. 124501.

[34]. C. Mayr, P. Stärke, J. Partzsch, R. Schüffny, L. Cederström, Y. Shuai, N. Du, and H. Schmidt, Waveform Driven Plasticity in $BiFeO_3$ Memristive Devices: Model and Implementation, Advances in Neural Information Processing Systems XXV, 2012, pp. 1709-1717.

[35]. R. Rosezin, E. Linn, L. Nielen, C. Kügeler, R. Bruchhaus, and R. Waser, Integrated Complementary Resistive Switches for Passive High-Density Nanocrossbar Arrays, IEEE Electron Device Lett., vol. 32, 2011, pp. 191-193.

[36]. S. Schmelzer, E. Linn, U. Böttger, and R. Waser, Uniform Complementary Resistive Switching in Tantalum Oxide Using Current Sweeps, IEEE Electron Device Lett., vol. 34, 2013, pp. 114-116.

[37]. E. Linn, S. Menzel, S. Ferch, and R. Waser, Compact modeling of CRS devices based on ECM cells for memory, logic and neuromorphic applications, Nanotechnology, vol. 24, 2013, pp. 384008.

[38]. A. Siemon, S. Menzel, A. Marchewka, Y. Nishi, R. Waser, and E. Linn, Simulation of TaO_x-based Complementary Resistive Switches by a Physics-based Memristive Model, 2014 IEEE International Symposium on Circuits and Systems (ISCAS), 2014, pp. 1420 - 1423.

[39]. T. Breuer, W. Kim, S. Menzel, V. Rana, A. Siemon, E. Linn, and R. Waser, Low-Current and High-Endurance Logic Operations in 4F2 - compatible TaO_x-based Complementary Resistive Switches, 2014 IEEE Silicon Nanoelectronics Workshop, 2014, pp. 67-68.

[40]. Y. Shuai, S. Zhou, D. Bürger, M. Helm, and H. Schmidt, Nonvolatile bipolar resistive switching in $Au/BiFeO_3/Pt$, J. Appl. Phys., vol. 109, 2011, pp. 124117.

[41]. W. Skorupa and H. Schmidt (Eds.), Subsecond Annealing of Advanced Materials: Annealing by Lasers, Flash Lamps and Swift Heavy Ions Springer, 2014.

[42]. E. Linn, A. Siemon, R. Waser, and S. Menzel, Applicability of Well-Established Memristive Models for Simulations of Resistive Switching Devices, IEEE Transactions on Circuits and Systems - Part I: Regular Papers (TCAS-I), vol. 61, 2014, pp. 2402 - 2410.

[43]. R. Degraeve, A. Fantini, S. Clima, B. Govoreanu, L. Goux, Y.Y. Chen, D.J. Wouters, Ph. Roussel, G.S. Kar, G. Pourtois, S. Cosemans, J.A. Kittl, G. Groeseneken, M. Jurczak, and L. Altimime, Dynamic Hour Glass Model for SET and RESET in HfO2 RRAM, Proceedings of the 2012 Symposium on VLSI Technology, 2012, pp. 75-76.

[44]. L. Nielen, S. Tappertzhofen, E. Linn, R. Waser, and O. Kavehei, An Experimental Associative Capacitive Network based on Complementary Resistive Switches for Memory-intensive Computing, 2014 IEEE Silicon Nanoelectronics Workshop, 2014.

[45]. O. Kavehei, E. Linn, L. Nielen, S. Tappertzhofen, S. Skafidas, I. Valov, and R. Waser, Associative Capacitive Network based on Nanoscale Complementary Resistive Switches for Memory-Intensive Computing, Nanoscale, vol. 5, 2013, pp. 5119-5128.

[46]. A. Siemon, T. Breuer, N. Aslam, S. Ferch, W. Kim, J. van den Hurk, V. Rana, S. Hoffmann-Eifert, R. Waser, S. Menzel, and E. Linn, "Realization of Boolean Logic Functionality using Redox-based Memristive Devices," Adv. Funct. Mater., vol. 25, pp. 6414–6423, 2015.

[47]. A. Siemon, S. Menzel, A. Chattopadhyay, R. Waser, and E. Linn, "In-Memory Adder Functionality in 1S1R Arrays," IECCC ISCAS, , pp. 1338-1341, 2015