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Optimizing Electric Double-Layer Capacitor Charging Efficiency through a Parallel Monitor Circuit: A Comparative Study with Lead-Acid Batteries

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Abstract: - This research explores the challenges associated with achieving a true full charge in Electric Double-Layer Capacitors (EDLCs) during relaxation charging. The conventional method, while reaching a full charge, is considered a pseudo full charge, leading to inefficient energy utilization. The proposed solution involves a parallel monitor with a simple electronic circuit that can be electronically disconnected during relaxed charging. This innovation prevents the wasteful flow of charging current through the parallel monitor, facilitating efficient relaxation charging. Experimental results demonstrate the effectiveness of the proposed parallel monitor in contrast to conventional methods, showing promise for practical applications in cordless equipment and similar scenarios. Future work aims to enhance accuracy and adaptability to variable charging currents. This article delves into enhancing the performance of Electric Double-Layer Capacitors (EDLC), particularly in series-connected configurations. Comparisons with lead-acid batteries highlight EDLC advantages in power electronics, showcasing long cycle life and high voltage operation. Charging inefficiencies arising from series connections prompt the introduction of a minimalist parallel monitor circuit. This circuit, utilizing only one MOSFET and two resistors, ensures uniform voltage distribution during charging. Additionally, it incorporates an electronic disconnection feature for relaxed charging, improving charging efficiency by over 25%. Experimental validation with a series-connected EDLC charging circuit demonstrates the effectiveness and practical utility of the proposed parallel monitor.

Key-Words: - Electric Double-Layer Capacitors (EDLCs), Relaxation charging, Charging efficiency, Parallel monitor circuit, Series-connected configurations, Charging current optimization, Energy utilization, MOSFET-based disconnection

1 Introduction

Electric double-layer capacitors (EDLCs), such as large capacitors, have the capability to store substantial amounts of electricity [1-5], making them useful for certain components in the latest market offerings. Due to this characteristic, they find applications in various domains of power electronics, including the storage of renewable electric energy sources like solar and wind power generation, as well as serving as replacements for secondary batteries in hybrid vehicles. Recent research has focused on enhancing the performance of EDLC [6-8]. In this context, we will compare EDLC with lead-acid batteries, a typical secondary

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battery. EDLC exhibits numerous advantages over lead-acid batteries, despite having lower energy density; it boasts a long cycle life and functions as a high-voltage device [9-17].

It offers several advantages, such as rapid charging and discharging capabilities with current, operability in low-temperature environments (below freezing), no memory effect, tolerance for over-discharging, and maintenance-free operation. However, even though a single cell of EDLC has a high withstand voltage due to its structure (ranging from 2.3V to 3.0V), the practical usage often involves connecting many cells in series or in series and parallel as a module. When charging in a series connection, considerations include selecting a charging power source with high efficiency and addressing the issue of uneven voltage sharing among cells. Without proper measures, the charging time may be limited by the first cell to be fully charged, leading to reduced stored energy and charging efficiency. The choice of a charging power source is crucial; while a constant voltage source results in a maximum efficiency of 50% during EDLC charging, a constant current source achieves around 50% efficiency and is commonly used. The problem of uneven cell voltage distribution arises due to differences in capacitance, leakage current, and initial residual voltage among cells. To address this, resistance can be added in series to the charging circuits of EDLC cells connected in series.

Various methods have been proposed for adding electronic circuits to monitor voltage, with the most practical example being the addition of a parallel monitor to each cell. This monitor ensures the cell reaches its withstand voltage and is fully charged by diverting charging current to the parallel monitor side. Ideally, a practical parallel monitor should be compact, utilizing a circuit with minimal components, especially as the number of cells increases in series or series-parallel configurations. In this paper, we propose a highly simplified parallel monitor circuit comprising only one MOSFET and two resistances. Notably, this circuit allows for easy electronic disconnection of the parallel monitor during relaxation charging by incorporating a straightforward electronic circuit. To validate its characteristics, an experimental setup using five EDLCs in a series-connected charging circuit is employed, and detailed measurements of charging characteristics and voltage sharing are conducted. The addition of a parallel monitor disconnection circuit is also explored, demonstrating the practicality of the proposed circuit for series-connected charging of EDLCs.

By incorporating this disconnection mechanism, the circuit reduces unnecessary energy consumption during the charging process, thereby potentially slowing the drain of a 12-volt battery and optimizing power use. This feature ensures that energy is conserved more effectively, making it highly beneficial for applications requiring prolonged battery life and efficient power management. Additional support is crucial for the precise selection of hardware to meet this requirement. Proper hardware choices ensure optimal performance, compatibility, and efficiency, particularly in complex systems where each component must align with specific technical and operational demands.

2 Niche Identification for Constant Current Charging And Relaxation Charging

Let's mathematically consider that constant current charging is suitable for Electric Double-Layer Capacitors (EDLC). The cell in an EDLC acts as a large capacitor, and its equivalent circuit, as shown in Fig. 1, resembles a complex RC circuit, with reported charging loss due to the internal resistance during charging [18-24]. However, uncertainties in resistance values make it challenging to calculate charging loss accurately [25-29]. Alternatively, a simplified equivalent circuit, depicted in Fig. 2, models the cell as a series connection of one capacitor (C) and equivalent series resistance (R). To explore the charging efficiency $(\eta(t))$, let's examine the capacitor charging circuit depicted in Fig. 3, where $\eta(t)$ is defined as the ratio of stored energy to the supplied charging energy, irrespective of the charging power source.

$$\eta(t) = \frac{P_{C(t)}}{P_{C(t)} + P_{R(t)}} \tag{1}$$

$$\eta(t) = \frac{\int_0^t i(t)\,\acute{v}_c(t)d\tau}{\int_0^t i(t)\,\acute{v}_c(t)d\tau + \int_0^t i^2(t)\,Rdt} \tag{2}$$

Here, $P_{C(t)}$ represents the capacitor storage power with resistance R, and $i(t)$ is the charging current. In Fig. 1(c), $v_c(t)$ represents the voltage, and $\acute{v}_c(t)$ is the virtual voltage of the capacitor C.

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Using equation (2), the following equation holds true for the charging efficiency $\eta(t)$ when using a constant voltage source, where t is the charging time:

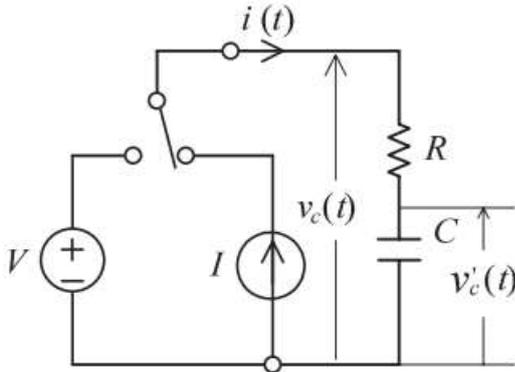$$\eta(t) = \frac{1}{2}\left(1 - e^{-\frac{1}{CR}}\right) \qquad (3)$$
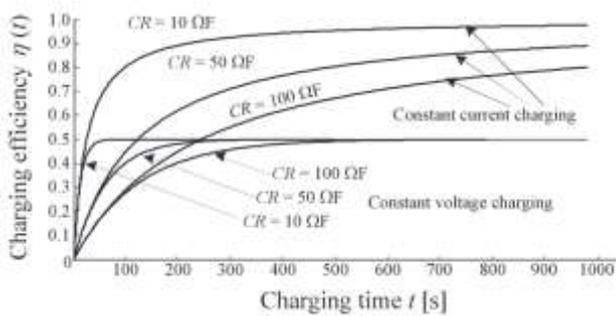

Fig. 1. Dual power source charging mechanism for EDLC.

Fig. 2. Comparison of charging efficiency between constant voltage source and constant current source.

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3 Introduction Parallel Monitor Circuit and Its Operation

To address this issue, various methods have been suggested, including the use of an electronic circuit known as a parallel monitor, which is connected in parallel to each cell to ensure an equal voltage during charging. Future advancements in parallel monitors could include the integration of a power transistor, comparator, shunt regulator, and power diode for precise voltage monitoring in specific applications. These improvements would address niche challenges, offering innovative solutions to meet real-world needs, enhancing efficiency and reliability [30]. Ideally, the parallel monitor circuit should be as simple as possible. This is crucial because as the number of cells in the charging circuit increases, so does the complexity and cost associated with the rising number of parallel monitors. In this study, we propose a minimalist parallel monitor circuit containing just one MOSFET and two resistors. This configuration offers the benefit of electronic disconnection of the parallel monitor itself during relaxation charging.

3.1 Circuit Configuration of the Parallel Monitor

The circuit configuration of the proposed parallel monitor is illustrated in Fig. 3(a). This uncomplicated circuit comprises a single MOSFET and two low-voltage-driven resistors. The operational principle, depicted in Fig. 3(a), unfolds as follows: Upon the initiation of charging, the voltage between the gate and source of the MOSFET is initially below the threshold. Consequently, the charging current I flows exclusively to the EDLC side, facilitating EDLC charging. As the EDLC voltage VC rises, surpassing the MOSFET threshold ($V_C/(1 + a)$), a fraction of the charging current I starts flowing through the MOSFET. Subsequently, this current gradually intensifies, causing a reduction in the charging current flowing through the EDLC. Eventually, all of the charging current I flows solely through the MOSFET, resulting in zero current through the EDLC. At this juncture, EDLC charging halts, and the EDLC voltage stabilizes at a constant level. The currents in resistors R_P and aR_P are negligible due to their kilohm-level resistance values. Consequently, the EDLC cell voltage V_C at this point can be considered the fully charged voltage $V_{C(max)}$. Fig. 3(b) represents an enhanced version of Figure 3(a) that enables the visual detection of full charge through a light-emitting diode (LED). It's noteworthy that the MOSFET body diode in both Figures 3(a) and (b) plays a role in preventing the reverse charging of the EDLC cell.

2 Problem Formulation

Let's mathematically consider that constant current charging is suitable for Electric Double-Layer Capacitors (EDLC). The cell in an EDLC acts as a large capacitor, and its equivalent circuit, as shown in Fig. 1, resembles a complex RC circuit, with reported charging loss due to the internal resistance during charging. However, uncertainties in resistance values make it challenging to calculate charging loss accurately. Alternatively, a simplified

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equivalent circuit, depicted in Fig. 2, models the cell as a series connection of one capacitor *(C)* and equivalent series resistance *(R)*. To explore the charging efficiency *(η(t))*, let's examine the capacitor charging circuit depicted in Fig. 3, where *η(t)* is defined as the ratio of stored energy to the supplied charging energy, irrespective of the charging power source.

3.2 Determination of constant a of parallel monitor

To ascertain the constant 'a' in the parallel monitor depicted in Figure 5, it is imperative to pre-measure the characteristics of the MOSFETs used, including parameters such as threshold voltage, on-resistance, and switching speed. These characteristics directly influence the performance of the parallel monitor circuit. Figure 6 illustrates the measurement circuit and a MOSFET obtained from a specific manufacturer, along with its characteristic diagram, which details the MOSFET's voltage-current relationship, operating limits, and response under varying loads, ensuring accurate integration into the charging circuit for optimal efficiency.
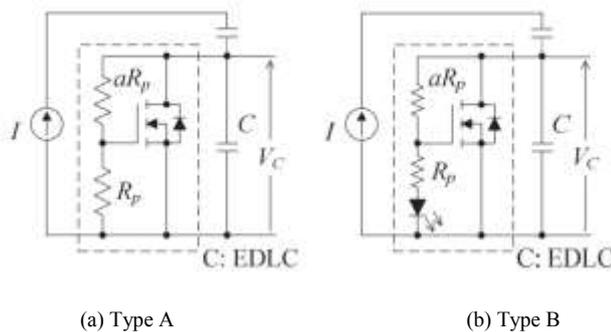

(a) Type A   (b) Type B

Fig. 3. Proposed parallel monitor circuits (0 < a ≤ 1).

In the measurement process, a constant current *I* is set to traverse the MOSFET. The gate-source voltage (V_{GS}) of the MOSFET is then varied, and the change in the drain-source voltage (V_{DS}) is calculated, considering 'I' as a variable parameter to obtain the V_{DS} - V_{GS} characteristic diagram, as demonstrated in Figure 6. In the characteristic diagram, when V_{GS} is below the MOSFET's threshold, the MOSFET current doesn't flow. However, the V_{DS} voltage, with a gentle slope depicted in Figure 6, saturates due to the no-load condition of the constant current source. Upon surpassing the MOSFET threshold, it enters a load state. As V_{GS} increases, the V_{DS} voltage experiences a rapid decrease. By analyzing the characteristic diagram, 'a' can be determined. For instance, when charging current I = 0.5 [A], a line is drawn on the

horizontal axis at the EDLC cell's full voltage $V_{C(max)}$ = 2.5 [V]. In a MOSFET, the gate-source voltage V_{GS} controls the transistor's operation by regulating the flow of current between the drain and source. The drain-source voltage V_{DS} represents the voltage drop across the MOSFET, influencing the amount of current flowing through the device based on the gate's input.
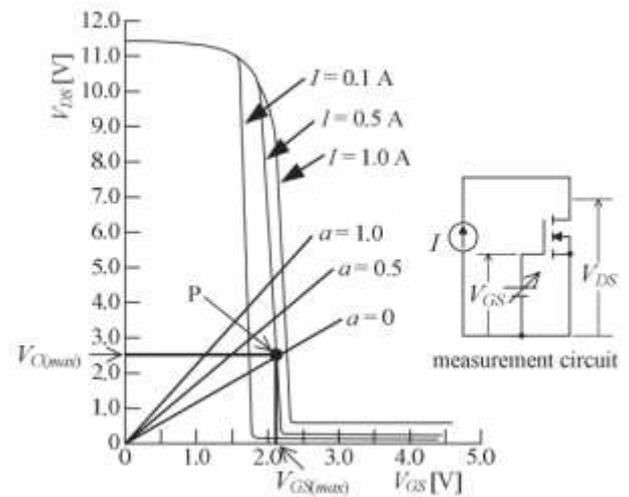

Fig. 4. V_{DS} - V_{GS} characteristics of a MOSFET

$$V_{DS} = (1 + a)V_{GS} \qquad (4)$$

The intersection of this horizontal line and the charging current line at I = 0.5 [A] reveals the V_{GS} value $V_{GS(max)}$ corresponding to point P. Utilizing this information, 'a' can be determined when V_{DS} = $V_{C(max)}$ and V_{GS} = $V_{GS(max)}$. Similarly, a similar equation holds for Figure 5(b).

$$V_{DS} = (1 + a)V_{GS} - aV_F \qquad (5)$$

In this scenario, V_F denotes the forward voltage of the LED. Similar to equation (4), 'a' can be determined, assuming V_F is known. Resistor R_P is then selected to meet the LED's forward current IF. Typically, the parallel monitors in a series connection of cells use the same type of MOSFET, streamlining the measurement process depicted in Figure 4 to a one-time task. Although variations in MOSFET threshold voltage and temperature coefficients may slightly affect $V_{GS(max)}$ in Equations (4) and (5), the manufacturer's guaranteed EDLC voltage tolerance often eliminates the need for complex circuits or temperature compensation. For applications requiring precise EDLC cell withstand voltage, a variable resistor for aR_P can be used to

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fine-tune aR_P after initial charging, enhancing accuracy. Temperature compensation is possible by replacing resistor R_P with a thermistor. For practical use, the fluctuation in $V_{GS(max)}$ of parallel monitors usually falls within the permissible range of withstand voltage. To illustrate, an experiment involving 20 EDLC cells with a parallel monitor (a = 0.1) yielded average V_{DS} and V_{GS} values of 2.479 V and 2.258 V, respectively, with standard deviations of 0.06 V and 0.055 V. Caution is advised when selecting the MOSFET for the parallel monitor circuit in Figure 5. The recent influx of low-voltage drive MOSFETs does not necessarily guarantee a sufficient power rating for the maximum power usage. In cases where one MOSFET cannot handle the power burden, connecting multiple MOSFETs in parallel with a common gate voltage can help distribute the charging current, reducing MOSFET power consumption. The resistors R_P and aR_P determine a power consumption of $V^2_{C(max)}/\{(1 + a)R_P\}$, hence the importance of selecting resistor R_P with a resistance value on the order of kilohms to minimize wastage. To scale up the EDLC charger's capacity, increasing the number of cells in series using the charging circuits in Figures 5 and 6 is crucial. Connecting multiple EDLCs in parallel to one parallel monitor further amplifies charging capacity. For substantial scalability, combining circuits from Figures 5 and 6 into one bank and connecting multiple banks in parallel is an effective strategy.

3.3 Subsection

The intersection of this horizontal line and the charging current line at $I = 0.5$ [A] reveals the V_{GS} value $V_{GS(max)}$ corresponding to point P. Utilizing this information, 'a' can be determined when $V_{DS} = V_{C(max)}$ and $V_{GS} = V_{GS(max)}$. Similarly, a similar equation holds for Figure 5(b).
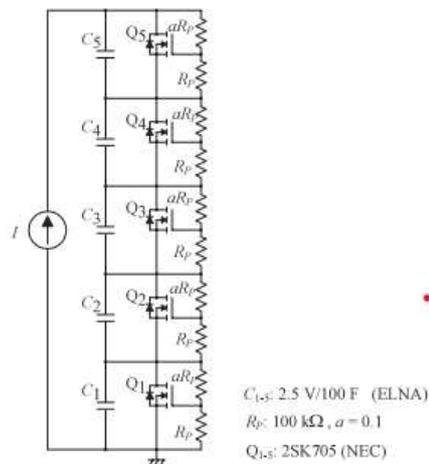

Fig. 5. Charging circuit for EDLCs with parallel moni- tors (Five serially connected EDLCs).
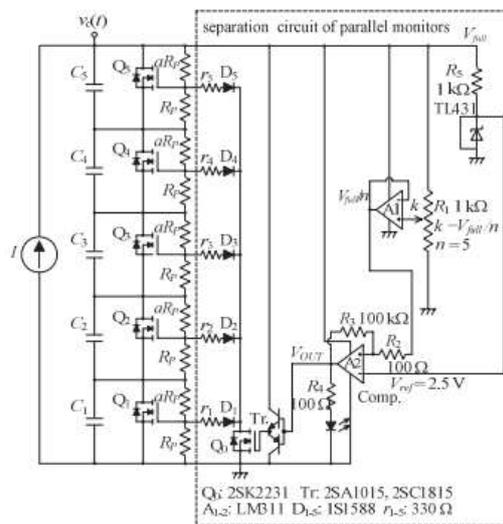

Fig. 6. Charging circuit for EDLCs with electronically separation circuit of parallel monitors during relaxation charging (Five serially connected EDLCs).

This is incorporated into the EDLC cell to detect the current, creating a logical inconsistency with the procedure of disconnecting the parallel monitor when the charge is nearing full during relaxation charging. To reconcile this contradiction, a measure was implemented to slightly lower the full voltage in the relaxed charging mode compared to the sum of the full voltages of each EDLC cell, preventing charging current from flowing to the parallel monitor side. Nevertheless, this configuration presents challenges in adjustment and poses the issue of reduced energy storage in the cell compared to a fully charged state.

The proposed parallel monitor in this study offers the advantage of electronically disconnecting during relaxed charging by incorporating a simple electronic circuit into the charging system. Figure 7

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illustrates a charging circuit for five EDLC cells with parallel monitoring in series, employed when relaxation charging is not in progress. Conversely, Figure 8 introduces an electronic circuit to the configuration in Figure 7, allowing charging by electronically disconnecting the parallel monitor during relaxation charging. The disconnection process in Figure 8 involves setting the input voltage of voltage follower A1 to 1/5 of the full voltage (V_{full} = 12.5 V) to detect full voltage in all cells. Adjust the voltage of variable resistor R_1 accordingly. Subsequently, setting the reference voltage V_{ref} of comparator A2 to V_{ref} = 2.5 V initiates a transition in the output V_{out} from low to high when all cells achieve full voltage. This prompts the LED to illuminate, signifying full charge detection. The resulting voltage change in $V_{out}t$ activates transistor Q_0, enabling the conductivity of the gate terminals of the MOSFETs (Q_1 to Q_5) in each parallel monitor between the resistors (r_1 to r_5), the diodes (D_1 to D_5), and Q_0.

consumption. The general formula for the current I_{Q0} flowing through transistor Q_0 during the operation of the isolation circuit can be derived from the circuit depicted in Figure 9. In this context, if the drain-to-earth voltage of the n-th parallel monitor is V_{Dn-E}, and the source-to-earth voltage is V_{Sn-E}, I_{Q0} is calculated using the provided formula, disregarding the forward voltage of diode D_n and the on-resistance of transistor Q_0.

$$I_{Q0} = \sum_{1}^{n} \left(\frac{V_{Dn-E}}{a(R_P + r_n) + r_n} + \frac{aV_{Sn-E}}{a(R_P + r_n) + r_n} \right) \quad (6)$$

4 Experimental Example

Using the circuits in Figures 5 and 6, we conducted a charging experiment with five EDLC series-connected circuits. The EDLC cell used was C = 100F, R = 5 mΩ (Elna), withstand voltage 2.5 V, MOSFETs (Q 1 to Q 5) were 2SK705 (NEC), and the full voltage of the charging circuit was 12.5 V.
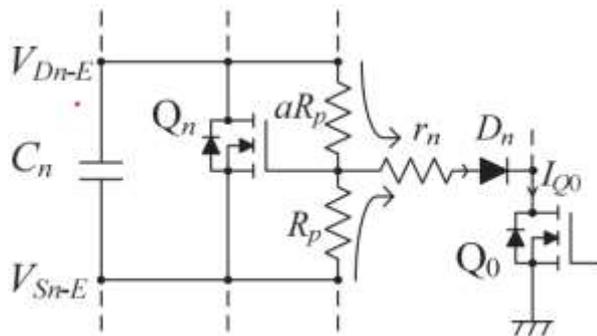

Fig. 7.   Relation between C_n current and I_{Q0}.

This process lowers the gate-source voltage of all MOSFETs below the threshold, preventing charging current flow to the MOSFETs and electronically disconnecting the parallel monitor. Although the resistances R_p and aR_P in each parallel monitor are not isolated, selecting resistance values in the order of kilohms renders the power consumption of R_p and aR_P negligible. For instance, if R_p = 10 kΩ, a = 0.1, the current in each parallel monitor is 0.227 mA (= 2.5 V/11 kΩ), which is in the range of milliamperes. This is minimal compared to the charging current in the order of amperes, making the power consumption of aR_P negligible. It's noteworthy that comparator A2 employs hysteresis to prevent erratic malfunctions near full charge, and resistors $r1, r2, r3, r4$, and $r5$ are strategically inserted to minimize current flow from the gate terminal of each MOSFET to ground, thereby reducing power
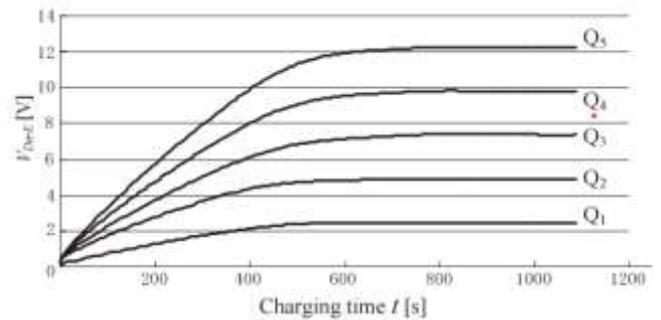

Fig. 8.   Drain to earth voltage characteristics of each MOSFET (Q_1 – Q_5) in Fig. 5.
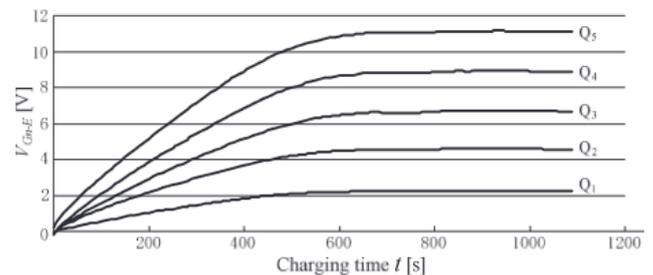

Fig. 9.   Drain to earth voltage characteristics of each MOSFET (Q_1 – Q_5) in Fig. 5.

Utilizing the circuits illustrated in Figures 5 and 6, a charging experiment was carried out involving five series-connected EDLC circuits. The specific EDLC cell employed in the experiment had a capacitance (C) of 100F, a resistance (R) of 5 mΩ

Financial Engineering
DOI: 10.37394/232032.2025.3.11

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(Elna), a withstand voltage of 2.5 V, and utilized MOSFETs (Q_1 to Q_5) of the type 2SK705 (NEC). The charging circuit's full voltage was set at 12.5 V.

4.1 Charging characteristics of EDLC with parallel monitor

Gauge the charging characteristics of the circuit depicted in Figure 7. Initiate the process by determining 'a' for the parallel monitor. Referring to the graph in Figure 6, opt for I = 0.5 A and V_{DS} = 2.50 V, resulting in V_{GS} = 2.27 V. Equation (4) yields 'a' as 0.1. Consequently, determine R_P = 10 kΩ and aR_P = 1 kΩ. Employ a constant voltage/constant current (CV/CC) power supply to initialize each cell, employing a constant current value CI = 0.5 A and a constant voltage value CV = 12.5 V. Subsequently, use a digital multimeter for automated assessment of charging characteristics. Fig. 8 illustrates the MOSFET characteristics (Q_1 to Q_5). This exhibits the measurement outcomes of drain voltage versus ground voltage $V_{Dn−E}$ (n = 1 to 5). In this scenario, the charging circuit's full voltage in Fig. 5 is 12.2 V, reflecting the charging voltage of each EDLC cell, and the corresponding MOSFET V_{DS} values are Q_1 = 2.48 V, Q_2 = 2.42 V, Q_3 = 2.49 V, Q_4 = 2.42 V, Q_5 = 2.42 V.

Next, observe Figure 9, depicting the charging characteristics of each EDLC cell's gate voltage versus ground voltage $V_{Gn−E}$ (n = 1 to 5). Extract the gate-source voltage VGS of each EDLC cell: Q_1 = 2.25 V, Q_2 = 2.33 V, Q_3 = 2.10 V, Q_4 = 2.2 V, and Q_5 = 2.20 V. Figures 8 and 9 collectively reveal that the charging voltage of each EDLC remains constant even during constant voltage charging (relaxation charging) mode. Notably, since the gate voltage surpasses the threshold, it is evident that the charging current flows to the parallel monitor MOSFET.

4.2 Charging characteristics of EDLC with parallel monitor disconnection circuit

Next, employing the circuit illustrated in Figure 8, an experiment was undertaken under conditions identical to those detailed in Section A, probing the impact of detaching parallel monitors during relaxed charging. *Presuming $r_1 = r_2 = r_3 = r_4 = r_5$ = 330 Ω*, the circuit denoted by the dotted line in Figure 8 draws around 0.2 mA of current. Consequently, the charging current was calibrated to CI = 0.52 A with CV = 12.5 V, consistent with the experiment outlined in Section A.
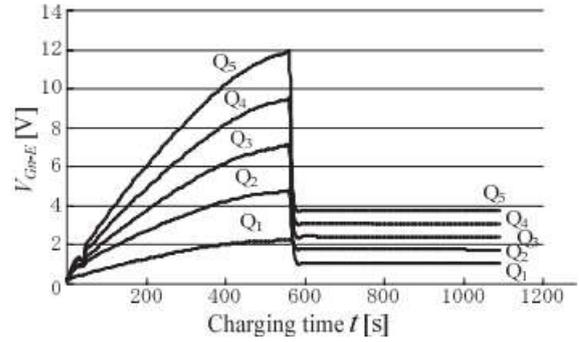

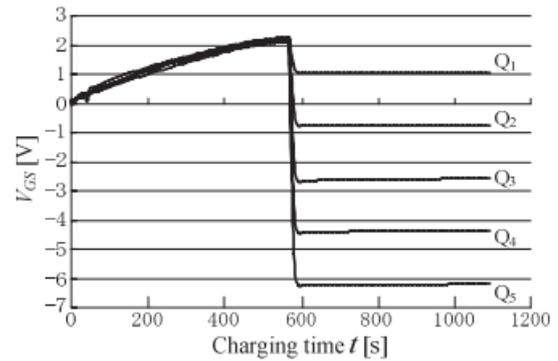Fig. 10. Gate to earth voltage characteristics of each MOSFET in Fig. 8

Fig. 11. Gate to source voltage characteristics of each MOSFET in Fig. 8.
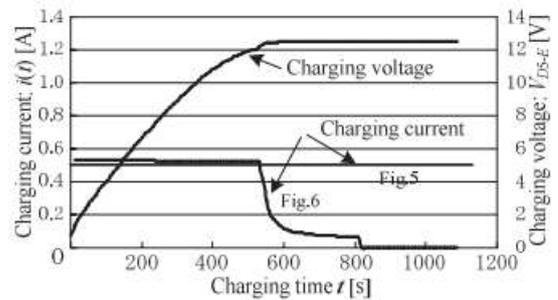

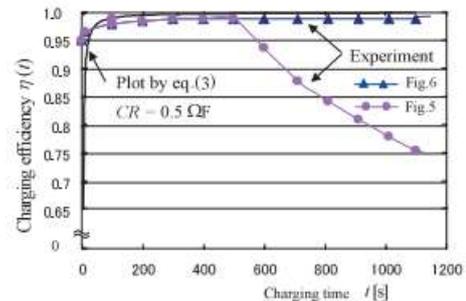Fig. 12. Gate to source voltage characteristics of each MOSFET in Fig. 8.

Fig. 13. Gate to source voltage characteristics of each MOSFET in Fig. 8.

In the experiment detailed in Section A, the full voltage V_{full} = 12.2 V, slightly lower than the

Financial Engineering
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theoretical full voltage of 12.5 V. However, in the circuit of Figure 8, relaxation charging (constant voltage charging) is performed, setting $V_{full}l$ = 12.5 V as the full voltage. Figure 12 illustrates the charging characteristics of the gate voltage versus ground voltage V_{Gn-E} (n = 1 to 5) for each cell (Q_1 to Q_5). It can be observed from Figure 12 that the full voltage is detected at t = 570 s, and the gate voltage of each cell decreases rapidly. Figure 11 displays the temporal changes in the gate-source voltage VGS of each cell. It is evident from Figure 13 that the gate voltage of each cell is below the threshold, leading to the electronic disconnection of parallel monitors. Figure 14 provides a comparison of the charging current experimental results between Figure 7 and Figure 8. From Figure 14, it can be discerned that in Figure 7, the charging current continues to flow even after reaching full voltage, whereas in Figure 8, it decreases rapidly. Finally, let's determine the charging efficiency $\eta(t)$ of the experimental circuit shown in Figure 8. For the theoretical value, use equation (3), and for the experimental value, use equation (1).

$$\int_0^t i(t)v_c'(t)d\tau = \frac{1}{2}Cv_c^2(t) \qquad (7)$$

$$\int_0^t i^2(t)Rdt = i^2(t)Rt \qquad (8)$$

The relationship $vc(t)$ and $I(t)$ were practically measured and deduced from equation (1). In this context, C = 100 [F]/5 = 20 [F], R = 0.005 × 5 = 0.025 [Ω], and I(t) represent the current and voltage, derived by introducing a 0.1 [Ω] resistor in series into the charging circuit. Figure 13 illustrates a graph depicting the theoretical and experimental values of charging efficiency $\eta(t)$. From Fig. 13, the experimental values in Fig. 6 closely align with the theoretical value in Equation (3), showcasing highly efficient charging characteristics surpassing 90%. Moreover, it is apparent from Fig. 5 that the circuit in Fig. 6 enhances the charging efficiency by over 25% at a charging time of 1100 s during relaxed charging. While the variance between the experimental and theoretical values is minimal, it is presumed to stem from the influence of the initial residual voltage.

To manage this power efficiently, the circuit must implement several design features. Current limiting is essential to prevent excessive current draw from the battery, which can be achieved using a MOSFET or a current-limiting integrated circuit set to approximately 10.19A, with some tolerance for variations. Voltage regulation is also critical, as the battery's output can fluctuate, especially under load. A DC-DC buck-boost converter can be used to stabilize the voltage supplied to the inverter, ensuring consistent performance despite any minor fluctuations in battery voltage.

In practical implementation, the power transfer circuit relies on a high-efficiency buck-boost converter for voltage stabilization, while current regulation can be managed with MOSFET-based current limiting. A control circuit using a comparator (such as A2) with hysteresis engages and disengages the power based on the battery's voltage and the inverter's requirements, adding a level of precision to the power flow. Isolation and safety components, like series diodes and control resistors, are also included to prevent leakage and manage power flow from the MOSFET gate to ground.

Combining these strategies enables effective power transfer from the 12V battery to the 240V inverter, ensuring a stable 110W output to the load while safeguarding the components from overcurrent and inefficiencies.

5 Summary

In conclusion, the design of the power transfer circuit from a 12V battery to a 240V inverter demonstrates effective regulation strategies to ensure stable power output for a 110W load while minimizing energy losses. This circuit uses advanced current-limiting and voltage regulation techniques, incorporating MOSFET-based control, a high-efficiency buck-boost converter, and protection components like diodes and resistors for optimal performance. To uniformly charge each cell initially to full voltage in a series-connected EDLC charging circuit, the addition of a parallel monitor is essential for monitoring the withstand voltage of each cell. This paper introduced a parallel monitor with a minimalistic design, utilizing only a single MOSFET and two resistors. Unlike traditional parallel monitors, which continuously draw current during relaxed charging, this monitor can electronically disconnect during this phase, simplifying the circuit and improving efficiency. Experimental tests on a five-cell EDLC charging circuit validated the effectiveness of this monitor,

Financial Engineering
DOI: 10.37394/232032.2025.3.11

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showing it to be both cost-effective and highly practical for applications with fixed charging currents, such as cordless devices. Future work will focus on enhancing the accuracy of the parallel monitor, modularizing it for flexible use, and adapting it to handle variable charging currents.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.

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