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Impact of Gate Insulation Material and Thickness on Pocket Implanted MOS Device

Muhibul Haque Bhuyan

Abstract**—**This paper reports on the impact study with the variation of the gate insulation material and thickness on different models of pocket implanted sub-100 nm n-MOS device. The gate materials used here are silicon dioxide (SiO_2), aluminum silicate (Al_2SiO_5), silicon nitride (Si_3N_4), alumina (Al_2O_3), hafnium silicate ($HfSiO_4$), tantalum pentoxide (Ta_2O_5), hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), and lanthanum oxide (La_2O_3) upon a p-type silicon substrate material. The gate insulation thickness was varied from 2.0 nm to 3.5 nm for a 50 nm channel length pocket implanted n-MOSFET. There are several models available for this device. We have studied and simulated threshold voltage model incorporating drain and substrate bias effects, surface potential, inversion layer charge, pinch-off voltage, effective electric field, inversion layer mobility, and subthreshold drain current models based on two linear symmetric pocket doping profiles. We have changed the values of the two parameters, viz. gate insulation material and thickness gradually fixing the other parameter at their typical values. Then we compared and analyzed the simulation results. This study would be helpful for the nano-scaled MOS device designers for various applications to predict the device behavior.

Keywords**—**Linear symmetric pocket profile, pocket implanted n-MOS Device, model, impact of gate material, insulator thickness.

I. Introduction

THE long-channel conventional bulk MOS devices have homogeneous doping concentration and accordingly the threshold voltage model was derived for them [1]. However, as the channel length of such devices was downsized to deep-sub-micrometer or beyond the 100 nm regime, Short-Channel Effects (SCE) started to arise. For the short-channel bulk MOS devices, the SCE includes the threshold voltage reduction, augmented leakage current during off-state, and punch through the bulk [2]. The SCEs are witnessed due to the 2-D nature of the surface potential and higher electric fields along the device channel. To combat these effects, horizontal channel doping engineering exploiting halo/pocket implant near the source and drain regions was found very useful, and as such corresponding MOS models for various parameters were developed [3]-[7]. If the doping concentration becomes non-homogeneous along the channel then it experiences the opposite effect on the threshold voltage called the Reverse Short-Channel Effect (RSCE) [8] that can annul the SCE of the MOS device [9]. In several earlier works of pocket implanted MOSFET modeling, it was shown that those models are capable of describing the behavior of the pocket implanted MOSFET for the channel length up to 50 nm [10], [11]. Those models incorporated several shapes of pocket profiles, like linear [12], Gaussian [13], and hyperbolic cosine [14] profiles. It was shown that the linear profile also works very well taking less simulation time [12]. However, as the channel length goes down, we have to reduce the gate insulation thickness and increase the gate dielectric constant to avoid threshold voltage lowering further and hence to improve the device performance parameters. It has already been established that by increasing the dielectric strength that is using high-*k* dielectric materials or by decreasing the gate insulation layer thickness, we can improve the performances of the conventional and advanced MOS devices [15]-[19]. However, this study was not extended to the pocket implanted nano-scaled devices. Therefore, in this work, we have studied various models of the pocket implanted MOS devices by changing the gate insulation materials and gate insulation layer thickness and analyzed their impacts on the device performance in the nano-scaled regime.

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II. Pocket Doped MOS Device Structure

The pocket embedded n-MOS device construction is shown in Fig. 1. The presumed co-ordinate scheme is presented at the right-hand part of the device construction.

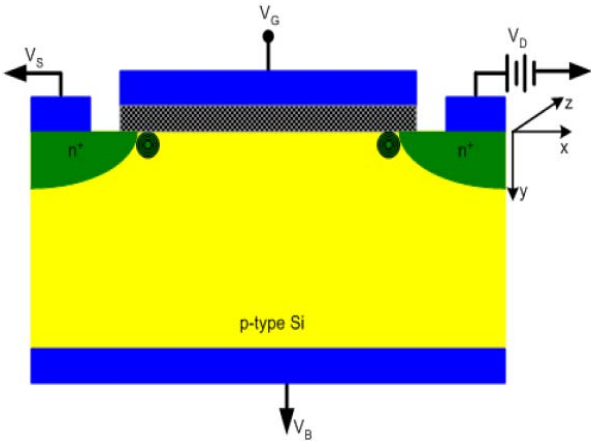

Fig. 1 Pocket embedded n-MOS construction with symmetric pockets both at the source and drain wings [21]

Table I shows all the device dimensions and parameters along with their symbols, values, and units used in this work. The device dimensions are measured according to the coordinate system of Fig. 1.

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TABLE I
DEVICE DIMENSIONS AND DEVICE QUANTITIES [10]

Device Dimension/Quantity	Symbol	Value	Unit
p-Si substrate doping concentration	N_{sub}	4.2×10^{17}	cm^{-3}
Peak pocket doping concentration at source/drain side	N_{sub}	1.5×10^{18}	cm^{-3}
Source or drain doping concentration	N_{sd}	9.0×10^{20}	cm^{-3}
Channel length	L	50	nm
Pocket length	L_p	20-30	nm
Junction depth	r_j	25	nm
Insulator thickness	t_{ox}	2-3.5	nm
Fixed oxide charge density	Q_f	10^{11}	cm^{-2}
Relative dielectric constant of the insulator	$\varepsilon_{r,ox}$	3.9-30	-
Relative dielectric constant of Si	$\varepsilon_{r,Si}$	11.8	-

Dielectric constant/permittivity is the characteristic of a material. It is defined as the amount of electric flux traversing through a particular material as compared to the vacuum of free space. This material is used as the gate insulation material for various types of MOS devices. Table II shows some widely used gate insulation materials for the MOS devices and their corresponding dielectric constants. In this work, we will use these materials to observe their impact on various operational parameters of the pocket implanted n-MOS devices. Table II shows relative dielectric constants of various gate insulator materials used in this structure.

TABLE II
GATE INSULATION MATERIALS AND THEIR DIELECTRIC CONSTANTS [17]

Material Name	Molecular Formula	Dielectric Constant
Silicon dioxide	SiO_2	3.9
Aluminum silicate	Al_2SiO_5	5.5
Silicon nitride	Si_3N_4	7.0
Aluminum oxide	Al_2O_3	9.0
Hafnium silicate	$HfSiO_4$	11.0
Tantalum oxide	Ta_2O_5	22.0
Hafnium oxide	HfO_2	25.0
Zirconium Hafnium	ZrO_2	26.0
Lanthanum oxide	La_2O_3	30.0

III. POCKET DOPED MOS DEVICE MODELS

Device models are developed under some contextual situations to allow the device engineers to inspect the functionality of the designed device to diverse input signals before manufacturing it in real-time. Moreover, such type of model affords the device engineers to have a greater intuition of the device's performance. As such, any kind of MOS device modeling begins from an elementary theoretical concept focusing on the dominant phenomena and then transforming them into a set of mathematical expressions. These models are also called the analytical models. There are certain types of typical trade-offs among generality, accuracy, development cost, and execution speed for such types of MOS transistor models. There are already several models for the pocket implanted MOS transistors to test the effect on the variation of the device dimensions and parameters. These models are useful for the device design engineers or the process engineers to estimate the device performance due to the horizontal doping distribution in an n-MOSFET demonstrating RSCE.

The derived models of the pocket implanted MOS transistors in the next sub-sections allow us to compute the impacts on the various operating parameters of this device due to the variation of the gate insulation thickness and materials. The models used in this work assume to have the shape of a straight line for the pocket doping concentration profile. The straight-line equations employed to define this shape were specified in [12]. Using those equations, an effective doping concentration equation was derived to use in various models of pocket implanted MOS device as shown in (1):

$$N_{eff} = N_{sub}\left(1-\frac{L_p}{L}\right)+\frac{N_{pm}L_p}{L} \quad (1)$$

Some important parameters that are used in this thesis for modeling the pocket implanted n-MOSFET are presented in Table III. The model parameters are briefly described in the next sub-sections.

TABLE III
LIST OF THE MODEL PARAMETERS STUDIED IN THIS WORK [10]

Name of the Model Parameter	Symbol of the Model	Unit
Threshold Voltage	V_{th}	V
Surface Potential	ψ_s	V
Inversion Layer Charge	Q_{inv}	C/cm^2
Pinch Off Voltage	V_p	V
Effective Mobility	μ_{eff}	$cm^2/V.s$
Subthreshold drain current	$I_{d,sub}$	A

A. Threshold Voltage Model

In [10], the threshold voltages (V_{th}) model was derived by solving the 1-D Poisson equation with the application of Gauss's law incorporating the substrate and drains biases effect and the pocket implantation doping concentration profile along the channel and is demonstrated in (2):

$$V_{th} = V_{th,L} + \gamma_B\sqrt{\left[\frac{N_{sub}}{N_{eff}}(2\varphi_F)-V_{BS}\right]} - \gamma_A\frac{N_{sub}}{N_{eff}}\sqrt{[(2\varphi_F)]} - \frac{6t_{ox}}{d_1}[2(\varphi_{bi}-V_{BS})+V_{DS}]\exp\left(-\frac{\pi L}{4d_1}\right) \quad (2)$$

where all the parameters are given in [10].

B. Surface Potential Model

When gate bias is applied to an n-MOSFET, a negatively charged depletion region is created near the surface up to a point in the bulk after which the substrate is neutral. The surface potential (ψ_s) is defined as the potential drop across the depletion region. By applying Gauss's law and solving the 2nd differential equation with appropriate boundary conditions, the desired analytical surface potential model is obtained as given in (3) [20]:

$$\psi_s(x) = \frac{c_1}{\sinh\sqrt{\frac{a_0}{a_2}}L}\sinh\sqrt{\frac{a_0}{a_2}}(L-x)+\frac{c_1+V_{DS}}{\sinh\sqrt{\frac{a_0}{a_2}}L}\sinh\sqrt{\frac{a_0}{a_2}}x-\frac{b_1}{a_0} \quad (3)$$

where all the parameters are given in [20].

C. Inversion Layer Charge Model

The inversion layer charge model derived by incorporating the surface potential [8] and threshold voltage [9] models for

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the pocket implanted n-MOSFET is given in (4) [21]:

$$Q_{inv} = -\sqrt{2q\varepsilon_{Si}N_{eff}}\left[\sqrt{\psi_s + \phi_{th}\exp\left(\frac{\psi_s - 2\varphi_F - V_{DS}}{\phi_{th}}\right)} - \sqrt{\psi_s}\right] \quad (4)$$

D. Pinch-Off Voltage Model

The pinch-off voltage (V_P) is called that minimum drain-to-source voltage at which the surface inversion charge (Q_{inv}) goes down to zero. Therefore, from (4), this model is derived as presented in (5) [21]:

$$V_P = V_{GS} - V_{th} - \gamma_A\left[\sqrt{V_{GS} - V_{th} + \left(\sqrt{2\varphi_F} + \frac{\gamma_A}{2}\right)^2} - \left(\sqrt{2\varphi_F} + \frac{\gamma_A}{2}\right)\right] \quad (5)$$

E. Effective Mobility Model

The effective vertical electric field model is given in (6) [22]:

$$E_{eff} = \frac{C_{ox}}{\varepsilon_{Si}}[\eta(V_{GS} - V_{th}) + V_{th} - V_{FB} - 4\varphi_F] \quad (6)$$

Then the effective electron mobility model is derived based on Coulomb, phonon, and surface roughness scattering models and then finally including the ballistic mobility model as given in (7) [22]:

$$\frac{1}{\mu_{n,eff}} = \frac{1}{\mu_{eqv}} + \frac{1}{\mu_{bal}} \quad (7)$$

F. Subthreshold Drain Current Model

The sub-threshold electron current density from the drain to source terminals is given by (8) [23]:

$$J_n = -qD_nN_{eff}\exp\left(-\frac{\varphi_{bi} - V_{BS}}{\phi_{th}}\right)\frac{\left\{1 - \exp\left(\frac{V_{DS}}{\phi_{th}}\right)\right\}}{\int_0^L \exp\left(-\frac{\psi_S}{\phi_{th}}\right)dx} \quad (8)$$

IV. Results and Discussions

This section explores the impact of gate oxide thickness and gate insulation material variation on different model parameters of the pocket implanted n-MOSFET developed earlier [8]-[10], [20]-[23] through different simulation results for the various device and pocket profile parameters as well as different bias conditions. For simulation purposes, the MATLAB software package of version 2018 is used. Codes have been developed in the MATLAB environment for all the models developed. Pocket profiles are also simulated using MATLAB codes. MATLAB simulation of all the codes has been performed in HP laptop having 1 TB hard disk drive, 512 GB SSD, 8 GB RAM, and an Intel Corei5 processor with a processing speed of 3.4 GHz clock frequency in Microsoft Windows 10 operating system. In the following sub-sections, various simulation results are shown.

A. Impact on Threshold Voltage

Fig. 2 shows the variation of threshold voltage with the variation of oxide thickness. We observe that as the gate oxide thickness is decreased threshold voltage is reduced. However, in all cases, RSCE is maintained. After that, we have simulated the same model for different gate insulation materials. Their relative dielectric permittivity increases from 3.9 for SiO_2 to 30 for La_2O_3. As the dielectric permittivity of the material increases threshold voltages are scaled down for the nano-scaled devices as shown in Fig. 3; because we can accumulate now more flux and charge.

B. Impact on Surface Potential

Fig. 4 shows the variation of surface potential with the variation of oxide thickness along the channel. We observe that as the gate oxide thickness is decreased surface potential is not changed appreciably. After that, we have simulated the same model for different gate insulation materials. Their relative dielectric permittivity increases from 3.9 for SiO_2 to 30 for La_2O_3. As the dielectric permittivity of the material increases, we observe a peculiar behavior at the center and the drain side of the device as shown in Fig. 5. At the central part of the device, we see that as we increase the dielectric constant, the surface potential increases but at the drain side it becomes the opposite.

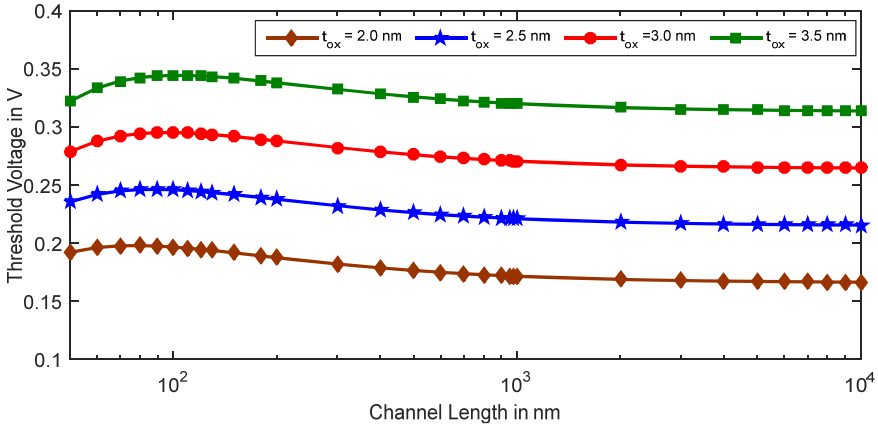

Fig. 2 Threshold voltage variation with channel length with the changing gate insulation layer thickness for SiO_2 as the gate dielectric material

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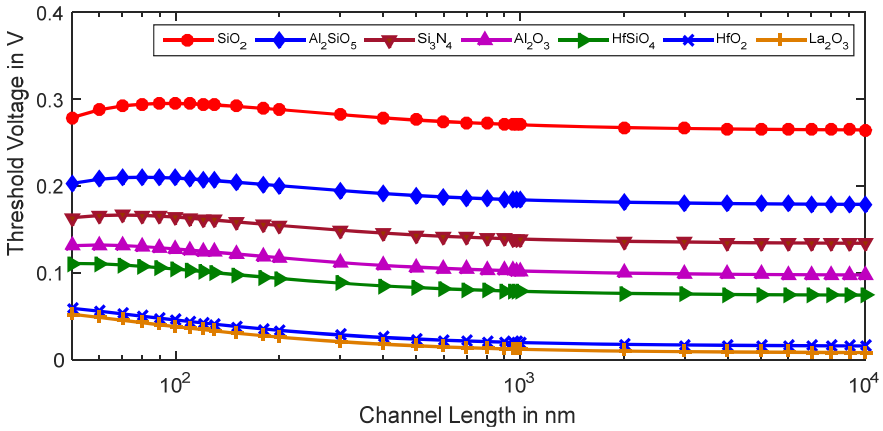

Fig. 3 Threshold voltage variation with channel length with the changing gate insulation materials for the dielectric layer thickness of 3.0 nm

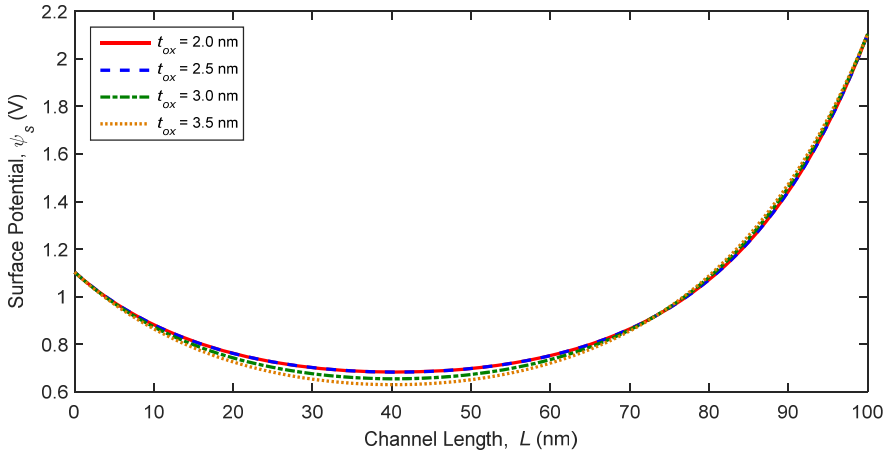

Fig. 4 Surface potential variation with channel length with the changing gate dielectric layer thickness for SiO_2 as the gate dielectric material

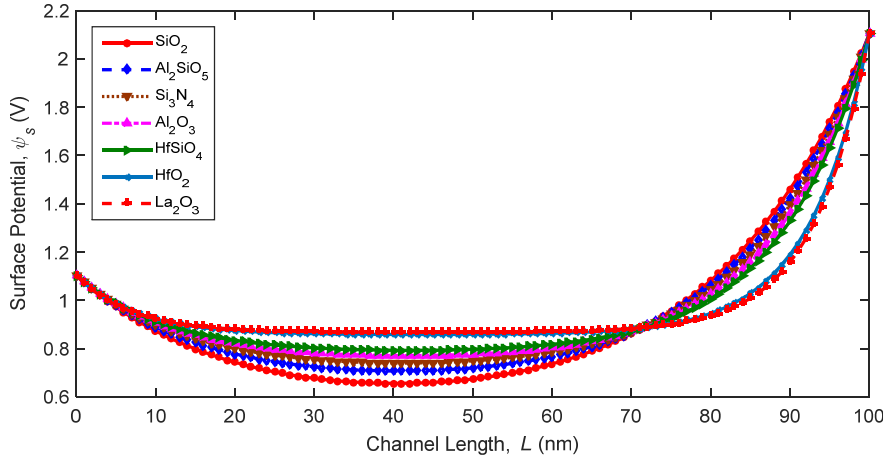

Fig. 5 Surface potential variation with channel length with the changing gate dielectric material for the dielectric layer thickness of 3.0 nm

C. Impact on Inversion Layer Charge

Fig. 6 shows the variation of inversion layer charge per unit area with the variation of oxide thickness along the channel. We observe that as the gate oxide thickness is decreased inversion layer charge is not changed appreciably when both drain and gate voltages are applied. However, in the central part, the inversion layer charge increases with the decrement of oxide thickness when the drain voltage is zero but gate voltage is above threshold voltage as shown in Fig. 7. After that, we have simulated the same model for different gate insulation materials. Their relative dielectric permittivity increases from 3.9 for SiO_2 to 30 for La_2O_3. As the dielectric permittivity of the material increases, we observe a peculiar behavior at the center and the drain side of the device as

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shown in Fig. 8. At the central part of the device, we see that as we increase the dielectric constant, the surface potential increases but at the drain side it becomes the opposite. But this effect is very negligible. However, in the central part, the inversion layer charge increases with the increment of the oxide layer's dielectric constant when the drain voltage is zero but gate voltage is above threshold voltage as shown in Fig. 9.

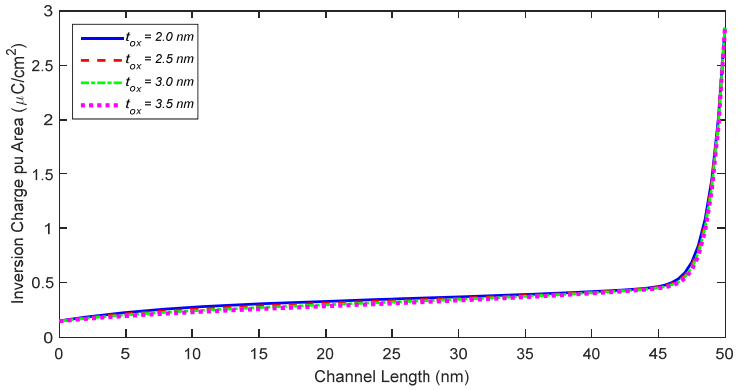

Fig. 6 Inversion layer charge variation with channel length with the changing gate dielectric layer thickness for SiO_2 as the gate dielectric material V_{DS} = 1.0 V and V_{GS} = 1.0 V

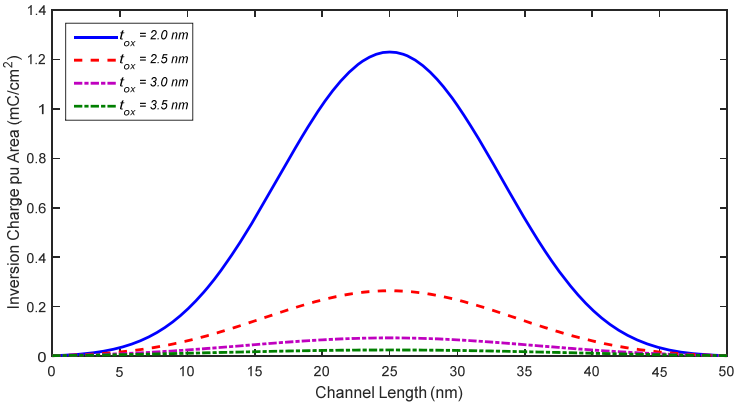

Fig. 7 Inversion layer charge variation with channel length with the changing gate dielectric layer thickness for SiO_2 as the gate dielectric material V_{DS} = 0.0 V and V_{GS} = 1.0 V

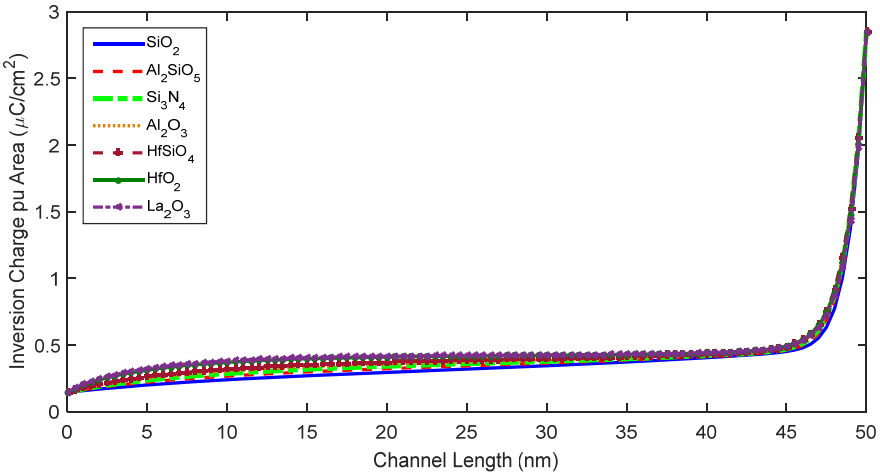

Fig. 8 Inversion layer charge variation with channel length with the changing gate dielectric material for the dielectric layer thickness of 3.0 nm V_{DS} = 1.0 V and V_{GS} = 1.0 V

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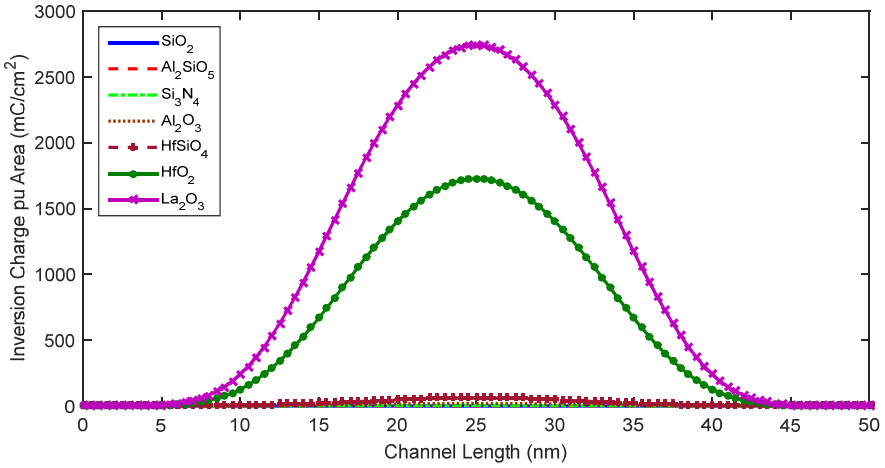

Fig. 9 Inversion layer charge variation with channel length with the changing gate dielectric material for the dielectric layer thickness of 3.0 nm V_{DS} = 0.0 V and V_{GS} = 1.0 V

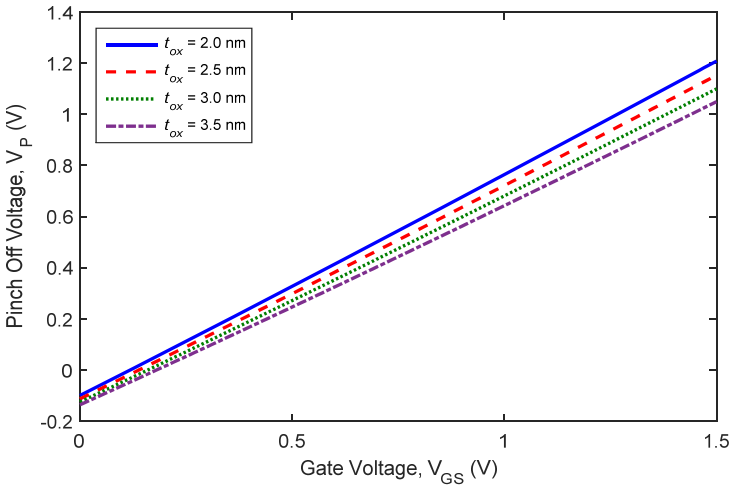

Fig. 10 Pinch-off voltage variation with gate voltage with the changing gate dielectric layer thickness for SiO_2 as the gate dielectric material for V_{DS} = 0.0 V and channel length, L = 50 nm

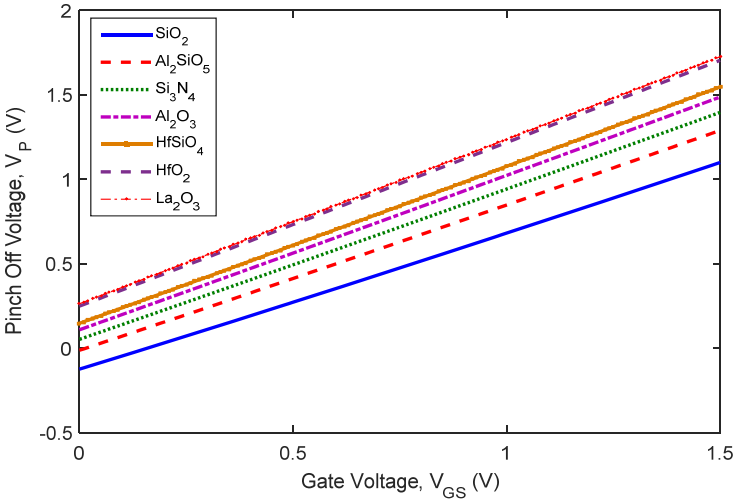

Fig. 11 Pinch-off voltage variation with gate voltage with the changing gate dielectric material for the dielectric layer thickness of 3.0 nm for V_{DS} = 0.0 V and channel length, L = 50 nm

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D.Impact on Pinch Off Voltage

Fig. 10 shows the variation of pinch-off voltage with the variation of oxide thickness versus gate voltage. We observe that as the gate oxide thickness is decreased pinch-off voltage is increased slightly at lower values of gate voltage but it increases greatly if higher values of gate voltage are applied. This phenomenon is observed due to the less amount of inversion charge (Q_{inv}) at a higher thickness of the gate insulating layer as shown in Fig. 7. After that, we have simulated the same model for different gate insulation materials. Their relative dielectric permittivity increases from 3.9 for SiO_2 to 30 for La_2O_3. As the dielectric permittivity of the material increases, we observe that as we increase the dielectric constant by changing the gate insulation materials, the pinch-off voltage increases slightly at lower values of gate voltage but it increases greatly if higher values of gate voltage are applied as shown in Fig. 11. This happens due to the increment of inversion layer charge at the surface with the increment of the dielectric permittivity as per Fig. 9. Therefore, we need a higher amount of gate voltage to replenish this charge and also a higher amount of drain voltage to cease the inversion channel at the drain wing of the device.

E. Impact on Effective Mobility

Fig. 12 shows the variation of effective electron mobility with the variation of oxide thickness versus effective vertical gate electric field. We can have more electric fields if we decrease the oxide thickness or increase the dielectric permittivity of the gate insulation material.

Fig. 13 shows the variation of effective electron mobility with the variation of gate insulation materials versus effective vertical gate electric field. As the gate insulation materials are changed their relative dielectric permittivity increases from 3.9 for SiO_2 to 30 for La_2O_3. As the gate oxide thickness or the dielectric permittivity of the gate material is changed, we observe a little change in the effective electron mobility in Figs. 12 and 13. However, if we look at the linear portion of the curve of Fig. 13 as shown on the inset figure, we see that the effective mobility goes up with the increment of dielectric strength. Besides, the effective vertical gate electric field increases as we increase the dielectric constant by changing the gate oxide thickness or the gate insulation materials. As such, we observe a slight increment of the electron effective mobility along the channel of the device.

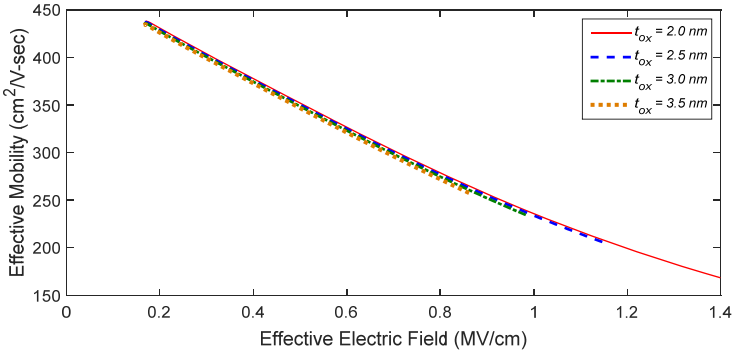

Fig. 12 Effective mobility variation with effective electric field with the changing gate dielectric layer thickness for SiO_2 as the gate dielectric material

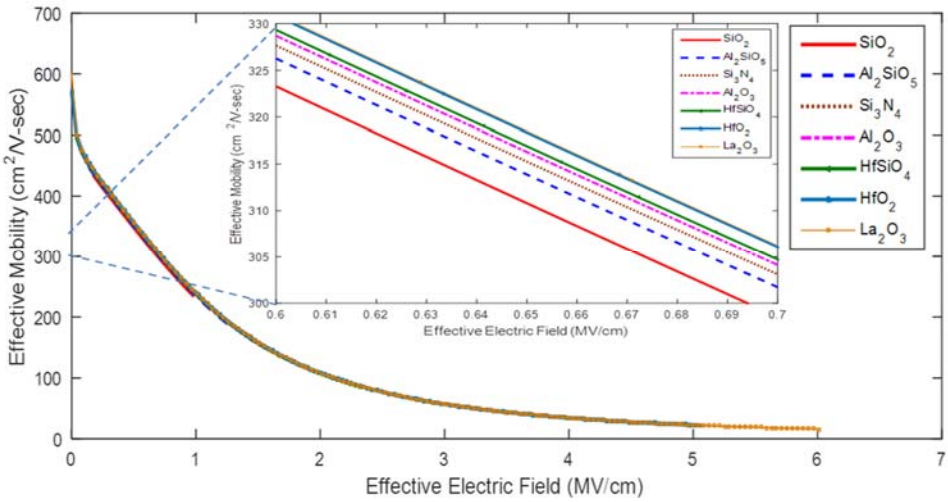

Fig. 13 Effective mobility variation with effective electric field with the changing gate dielectric materials for the dielectric layer thickness of 3.0 nm

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F. Impact on Subthreshold Drain Current

Fig. 14 shows the variation of subthreshold drain current with the variation of gate insulation layer thickness versus gate voltage. We observe that as the gate oxide thickness is decreased subthreshold drain current is increased for a particular gate voltage but it increases slightly if higher values of gate voltage are applied.

Fig. 15 shows the variation of subthreshold drain current with the variation of gate insulation materials versus gate voltage. As the gate insulation materials are changed, their relative dielectric permittivity increases from 3.9 for SiO_2 to 30 for La_2O_3. As the dielectric permittivity of the material is raised, we observe that subthreshold drain current is increased for a particular gate voltage but it increases slightly if higher values of gate voltage are applied. However, for the higher gate voltage, this phenomenon reverses as we increase the dielectric constant by changing the gate insulation materials as it happened in the case of the surface potential model.

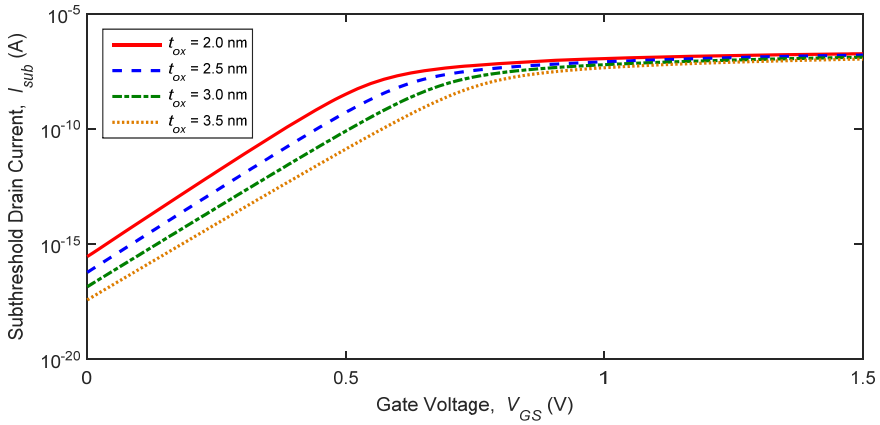

Fig. 14 Subthreshold drain current variation with gate voltage with the changing gate dielectric layer thickness for SiO_2 as the gate dielectric material

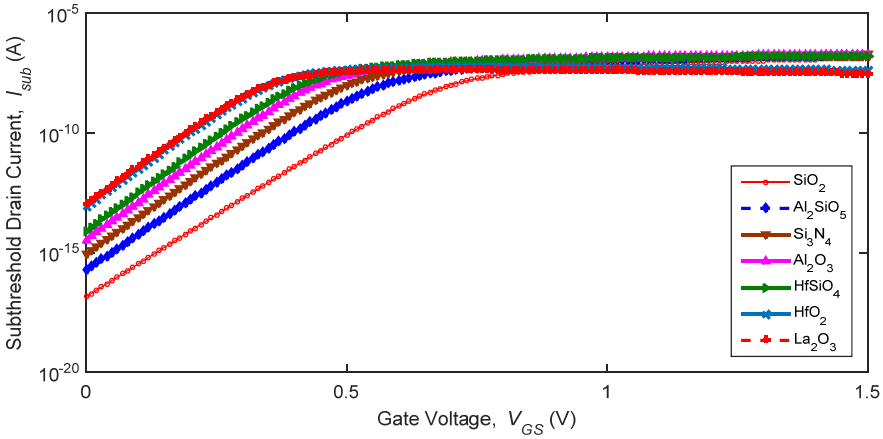

Fig. 15 Subthreshold drain current variation with gate voltage with the changing gate dielectric material for the dielectric layer thickness of 3.0 nm

V. Conclusion

When the thickness of the gate insulating layer decreases beyond 2 nm, the leakage current upsurges significantly due to the electron tunneling process through this layer. As a result, we need to substitute the gate dielectric material, for example, SiO_2 with a substantially wider insulating layer having high-*k* dielectric, such as Ta_2O_5, HfO_2, ZrO_2, La_2O_3, etc. These materials permit the capacitance to rise without raising the leakage current much. Therefore, in this work, different models of the pocket implanted nano-scaled n-MOSFET have been simulated in MATLAB for various values of the gate insulation layer thickness and gate insulation materials having high-*k* dielectric. From the simulation results, we can conclude that in the nano-scaled pocket implanted MOS devices, the lower values of gate insulation layer thickness and gate insulation materials with the higher values of dielectric permittivity (i.e., with high-*k* dielectric materials) should be utilized to get the optimum device performance.

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