Design of high speed VLSI Architecture for FIR filter using FPPE

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Abstract - **Numerous applications based on VLSI architecture suffer from large size components that lead to an error in the design of the filter during the stages of floating point arithmetic. Hence, it is necessary to change the architectural model that increases the design complexity and the time delay effect. The other difficulties in VLSI architecture include competing requirements, application area specialization and knowledge, changing and evolving terms. The issue encountered in the VLSI architecture is the increased number of components in the FIR filter design. For the VLSI architecture reconfigured with reduced register usage, this work provides the Floating Point Processing Element (FPPE) implementation. The FIR filter system retrieves a larger amount of delay components in the circuit that induces the complexity and high delay rate in the logical operation. To obtain the logical operation result with comparatively reduced delay rate, an efficient architecture based on FPPE method is developed.**

Keywords - **FIR filer, VLSI architecture, FPPE, Floating point.**

1. Introduction

Developments in electronic technology affecting the whole design structure caused various difficulties to the digital systems. Hence, the design of architecture requires a clear idea about various aspects that lead to novel VLSI architecture [1]. The multimedia applications and digital signal processing require large amount of data, the real time processing capabilities, and extended computational power. It leads to an increased attention towards the adaptable architectures with run-time reconfiguration capabilities. Thus, various new applications and algorithms evolve to provide a feasible option for the architecture. The traditional Field Programmable Gate Array (FPGA) based reconfigurable solutions terminate, because of their granularity and a huge amount of routing overhead that result in poor efficiency on silicon architecture. In the recent past, exploration has shifted to architectures of reconfigurable computing that offer control over all types of bits at a time. Several architectures such as, RAW, MATRIX, MorphoSys, DAPDNA, AsAP, Ambric, MORA, and so many other architectures work on the regular arrays of processing elements (PEs) that are connected through multiple levels of interconnected networks and they work with shared or local memory resources[3]. The system architectures perform depending on the top level array, interconnection scheme and processing of the individual cell. In the case of shared memory, the architectures are critical to system throughput. Hence, the processing of cells are the important pillars of the system that are equally important to the total throughput. Hence, it is significant to progress extendable arithmetic processing units that allow integrated system design in order to assure maximum throughput from a reconfigurable array based architecture. The important requirement of the media processing and modern DSP application is the capability of Floating Point (FP). The reuse or extension of integer data path leads to a reduction in development time, execution of low-cost system and feasible FPGA data paths.

The existing design approaches in FIR structure mainly focus on the reduction of complexity in adder whereas the complexity in a multiplier of the channel filter contributes a major part to the area and power. Most of the traditional methods do not provide a clear idea about the reduction in memory footprint of channel filter. But the block processing method, enhance the memory footprint of channel filter where the output of the block is computed in parallel. The block processing method provides higher throughput rate and an added advantage in hardware structure such as:

i) When the clock frequency is constrained by the technology, then the size of the block adjusts suitably to meet the targeted sampling rate.

ii) There will be no compromise on sampling rate, the power consumption of the design is reduced by the reduction of clock frequency.

The efficient reconfigurable architecture is used to derive an approach towards the major complexity in VLSI architecture such as, area, speed, and power. The Floating Point Processing Element (FPPE) is an important unit for addition, subtraction, multiplication, etc. of binary data in DSP applications. In the arithmetic calculation, most of the system struggles in the floating point number estimation due to its exponential term.

The floating point helps to predict the operation of both derivation and integration of that given signal. To design an

FPPE model, there are several techniques used for estimating Mantissa value and an exponential term, with minimum usage of logical components, where there are some limitations in those techniques which leads to increase in memory usage and delay.

In DSP processing system, some error may occur in calculating filter value in the stage of floating point. To overcome this drawback, some of the system refers changing architecture of that model. But this will increase the design complexity and also time delay effect. The aim of reducing architecture is to gain reduction in power loss and in area. Here introduce the new concept of Cross Folded Shifting design for ALU unit. Afterwards compare the LUT device utilization summary based previous work with number of register and Flip flops, speed, Power, and Delay in implementation result.

The rest of this paper is organized as follows: The proposed design strategy background is presented in Section2 and the development of FPPE based FIR filter computation and the proposed architecture is presented in Section3. Hardware-time complexities and performance comparison of the proposed structure are discussed in Section4. Conclusion is presented in Section5.

2. Literature Review

Finite Impulse Response (FIR) digital filters are common components in many Digital Signal Processing (DSP) systems [1]. Throughout the years, with the increasing developments in VLSI technology, the real time realization of FIR filter Algorithm with less hardware requirement and less latency has become more and more important. Since the complexity of implementation grows with the length of filter, several algorithms have been made to develop effective architectures for realization of FIR filters in Application below Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA) platforms.

The architecture of two integer reconfigurable data paths is proposed to achieve a distinct cycle of basic operations (addition, subtraction, multiplication, and accumulation). More difficult arithmetic and logical operations were performed to work in multicore platforms. While performing these ranges of operations, the data path has short and uniform critical path. The data path is extendable and they are parameterized to support higher precision arithmetic as well as software assisted variable precision reconfigurable systems. The process used static, domino, and data driven dynamic logic (D3L) to implement eight-bit version of the integer data paths in IBM (90-nm) [2]. Here, the data paths to achieve operating frequencies in the range of 1GHz. A 24-bit extension of the data path is in floating point processing element (FPPE) presented a new single precision. They are

formed by the architectural and circuit analysis on the integer data paths. The typical power consumption of this FPPE has 6.5-mW and it functions at a frequency of 1 GHz. The characteristics of the entire system influence strongly on the throughput, adaptability, and the cost imparted by the arithmetic Processing elements. If the design algorithm is able extend, it allows results and design reuse show a massive reduction in the development time as well as cost and it enhance the performance of PE value. Xydis etal. discussed the impacts of developing efficient programmable arithmetic algorithms to implement flexible architectures [3]. There need a stable interconnection scheme between multiple components is mainly focused to develop an inline flexibility that is allowed into the architecture and achieves computational efficiency. Although, this approach showed an immense difficulty in the interconnect network that is probably a bottle neck performance on basis of power in large array systems.

An additional approach [4] integrates flexibility into the computational algorithm that allow large array to have the essential flexibility with a basic interconnection scheme. The development of digital arithmetic structures is necessary and their impacts on image processing systems are studied. The aforementioned is achieved by using a combination of algorithm and circuit development that lead to flexibility in microprocessor architecture design. In order to work the techniques, many constraints need to be considered on architecture and circuit are placed on the system.

An innovative architecture for floating point in multiple precision, which is named as MAF (Multiply-Add Fused) unit design is proposed [5]. They accomplish floating point of either single precision double a time or double precision one time. When the module is on the critical data path, the traditional double precision MAF unit of each module is vectored and it is shared between multiple precision operations or by duplication of hardware resources. It also extends to other floating point operations such as, multiple precision floating point addition or multiplication.

The implementation of a new split-path of full adder function that is considered as the strongest contender in terms of performance, power efficiency as well as strong drivability [6]. The functions of PROPAGATE and GENERATE are used to realize full adders to obtain an optimum solution from the performance and process viability. They also provide a reduction of capacitance at critical nodes, high drivability, and robustness to process. The adder used in the proposed method is far better than the conventional dynamic domino adders in terms of reliability and robustness to process variations.

A parameterized MAC unit used for DSP core of embedded systems are described in the proposed system [7]. The MAC

unit offers a complete set of instructions for integer and fractional data types. The placement parameters and their architectural implementations are controlled in the current generations. The organized physical assignment to this generation process ensures a fast and predictable performance estimation. They also provide good performance, predictable quantitative analysis, and better optimizations than existing methods for modern technologies. The proposed method is used to govern an optimal DSP core architecture that allows a fast and reliable estimation of the MAC unit to perform the characteristics for various consequences.

The difficulty of a register in the direct-transpose forms of structures of FIR filter is to discover the possibility of the register reuses. The number of registers used in direct form is comparatively less than the transpose form and it allows register reuse in parallel implementation. The proposed system [8] architecture of Distributed Arithmetic (DA) for reconfigurable block-based FIR filter that is capable for bigger block sizes and higher filter lengths. The system function equation is computed by the use of direct form or transposes form structure. Both forms need the same number of arithmetic components such as multipliers, adders and delay elements. Therefore, the number of register bits for both forms is different. In the proposed system, the increase in the block size does not increase the number of registers. The proposed structure of block size consumes less power than the existing structure for the same throughput rates.

3. Design

The main objective of this work, the new novelty of IC chip design using Xilinx software tool for any signal process filtering (FIR). By default any data signal has noises, which need to be removed using any filter IC. So we design new compact integrated chip using Floating Point Processing Element (FPPE), is an important unit for addition, subtraction, multiplication, in ALU method and the binary data in DSP application.

Since in DSP processing system, there is some error may occur in calculating filter value in floating point stage. To overcome this drawback, some of the system refers changing architecture of that model. But this increase the degree of complexity and also time delay effect. The aim of reducing architecture is to gain reduction in power loss and also in area. Here introduce the new concept of Cross Folded Shifting design for ALU unit. The work compare the LUT device utilization summary based previous work with number of registers, number of Flipflops, speed, Power, Delay in implementation result.

There are many methods and approaches to design a FIR filter such as Distributed arithmetic (DA) [8], Canonic Sign

digit (CSD) [18] etc. Here the design of new compact integrated chip using Floating Point Processing Element (FPPE) is an important unit for addition, subtraction, multiplication, (ALU) method and the binary data in DSP application. The architecture introduces the new concept of Cross Folded Shifting for ALU unit.

Any DSP system always produces an output y (n) at every unit time. The transformed output may have experienced the effect of noise and can be degraded. The functional block adder itself makes possibilities of this degradation. The resources used in transformed system are adder, register, and multiplexers. The functional block that is the adder is therefore reduced.

3.1 FPPE Multiplier

A Single-Precision floating-point number occupies 32 bits, so there is a compromise between the size of the mantissa and the size of the exponent .These chosen sizes provide a range of approximately $\pm 10^{-38}$ to 10^{38}.

To multiply two floating point numbers the following steps are involved [9]:

• If one or both operand is equal to zero results zero otherwise;

• The significant bits in the mantissa (X*Y) got multiplied;

• Adding the exponent of two numbers and then the result will be subtracted from Bias (E1+E2 -Bias);

• The result produce the sign bit (X ^ Y);

 • If needed, the result can be normalised one right shift of mantissa and increment result of exponent;

 • Round off the results to the allowed mantissa bits;

• Checking is there any overflow or underflow occurred in the bits.

3.2 Folding

Here the new concept of Cross Folded Shifting design is applied for implementing ALU unit.

 Normally, ALUs can shift the operand by one bit position, whereas more complex ALUs that uses barrel shifters allow them in one operation to shift the operand by an arbitrary number of bits. In all single shift operations, the bit shifted out of the operand appears on carry-out; the value of the bit shifted into the operand depends on the type of shift.
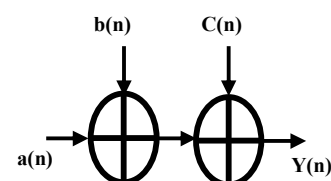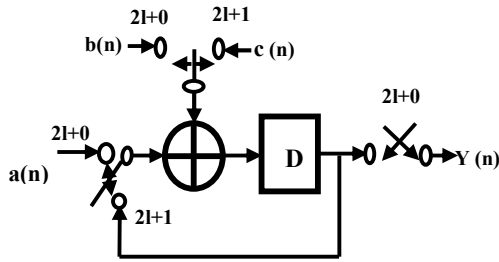
Fig. 1 Folding Technique

Fig.2. Folding Technique with factor 2

Since in DSP processing system, there is some error may occur in calculating filter value in the stage of floating point. To overcome this drawback, some of the system refers changing architecture of that model. But it increase the design complexity and also in time delay effect. The aim of reducing architecture is to gain reduction in power loss and also in area.

Here we introduce the new concept of Cross Folded Shifting design for ALU unit. The number of Flip-Flops (FFs) and Look up Tables (LUTs) used in the proposed architecture is reduced. The power consumption is reduced due to the reduction in the size of the components. This design is synthesized in VERILOG code language and implemented in the Field Programmable Gate Array (FPGA).
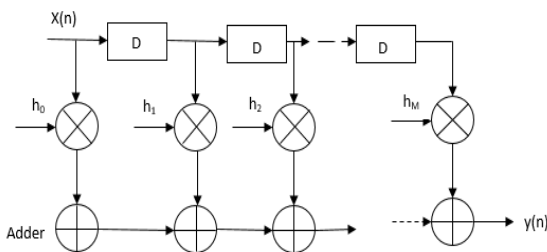

Fig.3. Direct form of M taps FIR Filter

4. ARCHITECTURE

The Floating point processing Element can be implemented as the flowchat given below.

There is one register which produces logical output that holds paring of blocks at each stage. The crossing of bit sequence from input to output will optimize the delay block due to link formation in register.

 Minimum usage of logical components and also reduce the amount of register usage and also we change the structure of shifter and adder logical architecture which will reduce the accumulator size and also reduces FFs and LUTs. , we present a multiplier free FIR filter which is
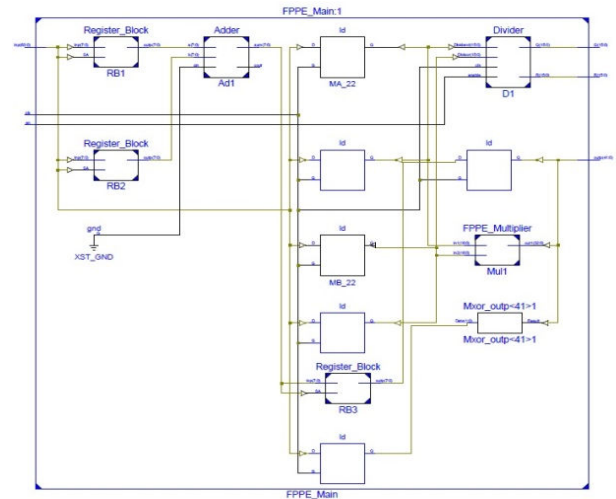
done by using the adder and shifter followed with accumulator to proceed the Floating Point Processing.

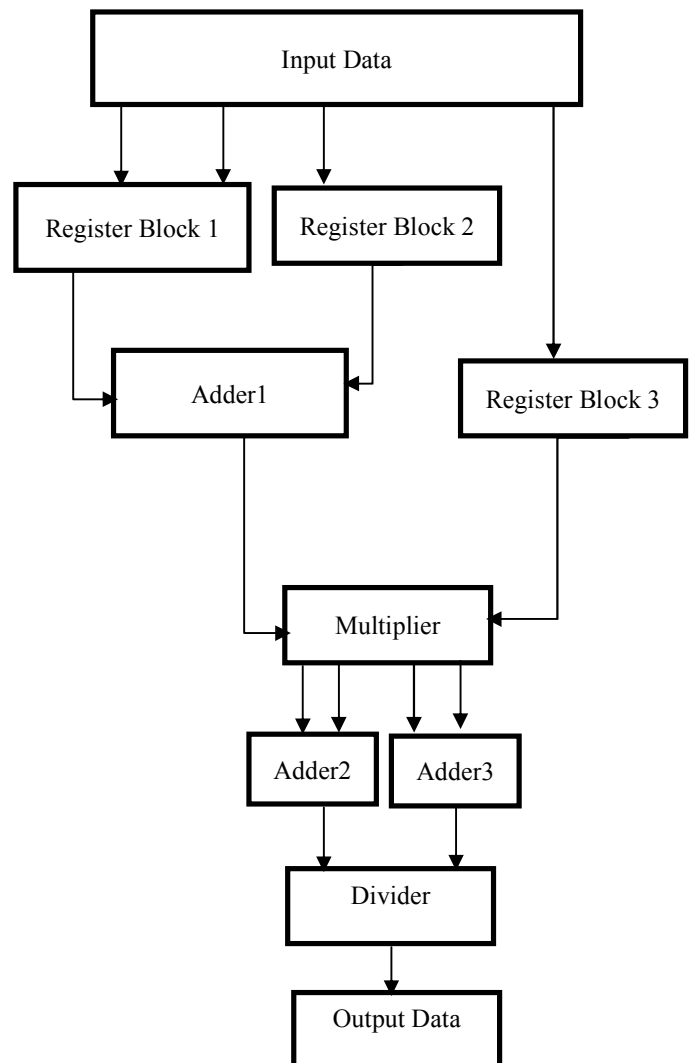*Fig. 4 Architecture of FPPE model in Matlab*
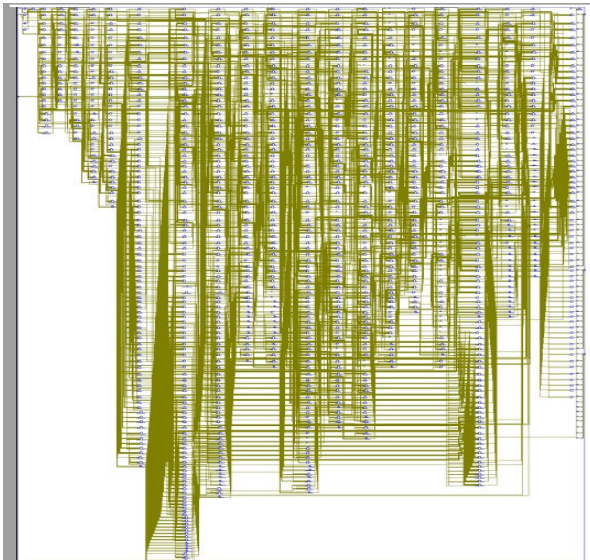

Fig. 5 Flowchart of FPPE Achitecture

Fig. 6 Technology Layout

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Device utilization summary:
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Selected Device : 6slx4tqg144-2

Slice Logic Utilization:
 Number of Slice Registers:              75  out of   4800    1%
 Number of Slice LUTs:                  920  out of   2400   38%
    Number used as Logic:               920  out of   2400   38%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    964
    Number with an unused Flip Flop:    889  out of    964   92%
    Number with an unused LUT:           44  out of    964    4%
    Number of fully used LUT-FF pairs:   31  out of    964    3%
    Number of unique control sets:       21

IO Utilization:
 Number of IOs:                         140
 Number of bonded IOBs:                 128  out of    102  125% (*)
    IOB Flip Flops/Latches:              50

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:                2  out of     16   12%
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Fig.7 Device Utilization Summary

5. RESULTS AND DISCUSSIONS

An optimal FIR filter architecture using Xilinx Verilog is designed and synthesized. The programming is done in verilog for a spartan 6- 100T FPGA as target device.

In this design, the number of logic gates, register and counters has designed such a way that the architecture with lowest number of gates has less in area and number of flip-flops.

In the LUT device utilization summary based power of simulation. If we have low level of LUT, Flip-flops and IOB's based Power is reduced.

Speed of the process is influenced when total time executed based speed will increase. Maximum time display is shown in Summary of the synthesis report.
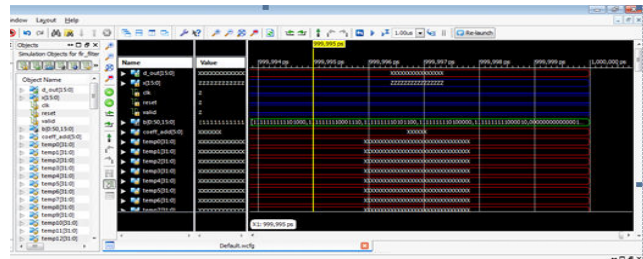
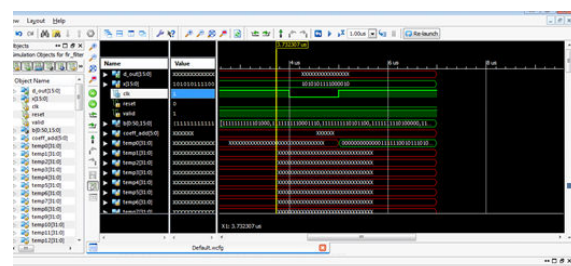

Fig. 8 Initial screen of simulation
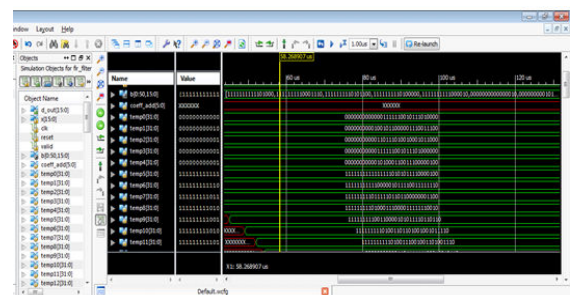

Fig.9 Simulation Results
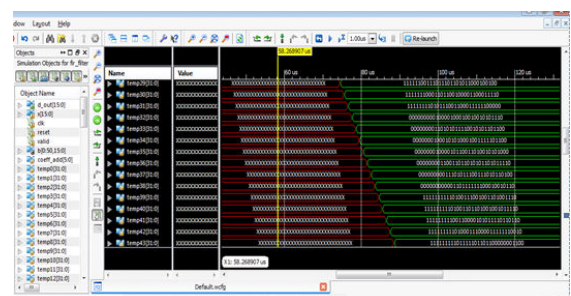

Fig.10 Simulation Results
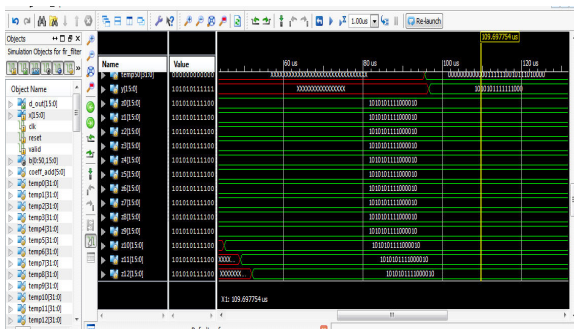

Fig.11 Simulation Results
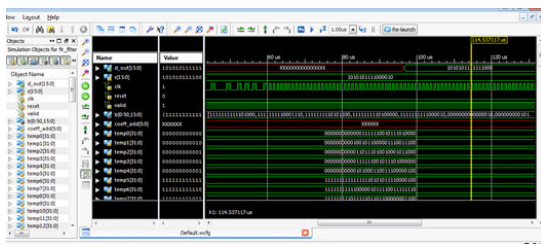
Fig. 12 Simulation Results

Fig.13 Final Result

The performance analysis and comparison of the design with previous architectures are shown in Table 1.

Table 1. Comparison based on various FIR structures.

Parameter	Basic FIR filter[13]	Serial DA [13]	Parallel DA [13]	CSD [14]	FPPE
Delay (ns)	12.697	6.418	3.686	6.312	3.487
Area(Logic Blocks)	204	60% Reduction	20% Increased	60% Reduced	40% Reduced
Power (W)	0.081	0.081	0.081	0.1	0.1

Here compares the LUT device utilization summary based on previous works, basic FIR filter structure, the parallel and serial distributed arithmetic structures with FPPE architecture with number of registers, number of Flip flops, speed, Power, Delay in implementation result. A delay of 50% reduction can be viewed from Serial structure than the basic. More than 40% reduction is obtained by parallel structure of distributed arithmetic. Thus for FPPE architecture the delay is reduced again and can be used in high speed applications.

Minimum usage of logical components and also reduce the amount of register usage and also we change the structure of shifter and adder logical architecture which will reduce the accumulator size and also reduces FFs and LUTs. , we present a multiplier free FIR filter which is done by using the adder and shifter followed with accumulator to proceed the Floating Point Processing.

6. CONCLUSION

The difficulties in VLSI architecture include competing requirements, application area specialization and knowledge, changing and evolving terms. The issue encountered in the VLSI architecture is the increased number of components in the FIR filter design. For the VLSI architecture reconfigured with reduced register usage, this paper provides the Floating Point Processing Element (FPPE) implementation. The FIR filter system retrieves a larger amount of delay components in the circuit that induces the complexity and high delay rate in the logical operation. The cross folded shifting enabled the architecture to get the desired response in accordance with speed, power and area. Future work will involve extensive analysis of the floating-point units to identify more design trade-offs.

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