A Triple Source Thirteen Level Inverter

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Abstract: - Multilevel inverters are attracting the attention of investigators concerning high-power and medium-power applications. Interestingly, an arrangement with a couple of devices is popular in an attempt to enhance efficacy and durability. This work suggests a Triple Source Thirteen Level Inverter based on minimal device count. By integrating three voltage sources with eight semiconductor devices, the proposed design develops thirteen levels. Gating signals are created using the Phase Disposition Pulse Width Modulation (PDPWM) technique. To compute efficiency along with losses PLECS software is used. The successful configuration implementation is investigated using MATLAB/Simulink under various parametric conditions. The proposed topology is tested using Hardware-In-the-Loop (HIL) experiments to validate its feasibility.

Key-Words: - Multi-level inverter, Phase Disposition Pulse Width Modulation, Total Standing Voltage, Total Harmonic Distortion, OPAL-RT(OP4510), reduced switch count, triple source thirteen level.

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1 Introduction

Multilevel inverters (MLI) are in great demand for green technologies for converting the energy in addition to industrial applications owing to their more reliable form of output than two-level inverters. MLIs possess attractive capabilities like nearly sinusoidal output voltage development, low dv/dt stress, minimal power loss, along with low total harmonic distortion (THD). Traditional MLIs are broadly divided into three types: neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB), [1], [2], [3]. Conversely, traditional MLI has restrictions, including capacitor voltage imbalance in NPC and FC. Among these inverters, the CHB MLI necessitates minimal component count than other conventional inverter topologies for creating an identical level of output. CHB inverters are transitioning from a traditional perspective to real-world applications due to capabilities that include high degree of modularity, and the ability to safely link to medium voltage with superior power quality, [4], [5].

The beneficial effects associated with utilizing higher levels involve improved efficiency, lessened filter size, substantial power density, reliability, as well as a wider implementation range. However, researchers experienced some obstacles while reducing component counts, which include enhanced rated voltage of switching devices, loss of versatility, a decrease in the number of associated states, unpredictability demands for bidirectional switches, new control methodologies, and an enormous prevalence of sources to achieve the predicted levels count from current topologies, [6], [7], [8], [9], [10].

The real purpose for creating new MLI arrangements seems to reduce the number of isolated sources, devices, and drivers. Based on these parameters, an enormous number of designs are put forward in previous studies, [11], [12]. In [11], a novel structure utilizing H-bridge produces both positive and negative modes of output. Due to the additional two devices in the topology, it limits to medium voltage applications. Some of the configurations are discussed in [12] and [13], with their own range of benefits and drawbacks. By modifying the circuitry of [11], some of the issues are addressed in [14].

The design suggested in [15], operates as a sub module associated with series. The cascaded setup in [16] relies on half-bridge structured DC voltage sources. These devices in one of the arms of the reconstructed single-unit setup enhance the voltage sources, along with every module possessing a separate H-bridge to recognize its polarity. The modified structure's successive connection lowers the voltage stress of devices, but the switch count rises in comparison with [15]. In [17], it implies a new configuration with minimal sources and devices. Several structures employ modified H-

Bridge (MHB) designs for improved voltage development, [18], [19]. To limit the output voltage peak in all the preceding topologies, it needs two switches. Similarly, the structure of a novel MLI invention increases to reduce switch-blocking voltage, [20], [21]. Each switch in this set of network topologies has a blocking voltage that is less than peak voltage, [22], [23], [24], [25].

Switched capacitor-based configuration utilizing high-frequency control methodology is presented, [26]. Analysis of power losses for a three-level inverter is examined, [27]. For HVDC system applications a modular MLI is designed and described, [28]. Comparative analysis of controllers for an inverter with reference to PMSM driving applications is discussed in [29]. A novel converter is structured for DC motor applications addressed in [30]. Artificial intelligence dependent fault identification methods for inverters are described, [31], [32]. Machine learning based techniques for PV-connected inverter structures are examined, [33].

The objective of this work is to minimize the number of devices and TSV by using TSTL configuration. The remaining work is arranged as follows: Section 2 discusses the proposed topology including operating modes and pulse width modulation technique. Section 3 addresses voltage stress and loss analysis. Section 4 compares the proposed topology to other topologies to evaluate its outcome. Section 5 explores simulation, Thermal modeling, and HIL implementation to help to understand the TSTL inverter performance. Section 6 depicts the work's conclusion.

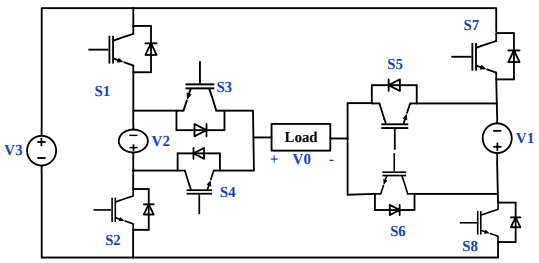


Fig. 1: Proposed Topology

2 Proposed Topology

The TSTL inverter is presented in Figure 1. The circuit configuration involves triple sources with eight components. The sources are arranged in natural sequence and devices are an IGBT connected in parallel with a diode. The device arrangement (S_1, S_2), (S_7, S_8), (S_3, S_4), and (S_5, S_6) are connected in a manner such that conductivity at the identical span leads to maloperation of sources. Therefore, these devices should operate in complementary mode. The switching modes are depicted in Table 1, 0 and 1 represent turning off and turning on the switch respectively. Figures 2 and 3 display the operating modes of the TSTL inverter based on the operating modes listed in Table 1 Green and red in Figure 2 and Figure 3 point to a conductivity and non-conductivity path respectively.

Table1.Switching modes of TSTLI

Switching State ***(S_1-S_8)***	***Output Voltage*** ***(V_0)***
1-0-0-1-1-0-0-1	*+6V_{dc}*
1-0-0-1-0-1-0-1	*+5V_{dc}*
1-0-1-0-1-0-0-1	*+4V_{dc}*
1-0-1-0-0-1-0-1	*+3V_{dc}*
1-0-0-1-1-0-1-0	*+2V_{dc}*
0-1-1-1-1-0-0-1	*+1V_{dc}*
0-1-0-1-0-1-0-1	*0*
1-0-1-0-0-1-1-0	*-1V_{dc}*
0-1-1-0-0-1-0-1	*-2V_{dc}*
0-1-0-1-1-0-1-0	*-3V_{dc}*
0-1-0-1-0-1-1-0	*-4V_{dc}*
0-1-1-0-1-0-1-0	*-5V_{dc}*
0-1-1-0-0-1-1-0	*-6V_{dc}*

2.1 Operating Modes

The positive, zero, and negative modes of the design are explained in subsequent sections.

2.1.1 Positive and Zero modes

Figure 2 depicts the formation of positive and zero modes. The operating modes are represented by the orange color in Table 1.

$0V_{dc}$: Figure2(a) and (b) show two different approaches for obtaining the output voltage as zero. The top leg device (S_1, S_3, S_5, and S_7) or the bottom leg devices (S_2, S_4, S_6, and S_8) create a conducting path to obtain zero level.

$+1V_{dc}$: Figure2(c) reveals a conduction path created by switches S_2, S_4, S_5, and S_8, and source voltage (V_1) comes across the load.

$+2V_{dc}$: Switches S_1, S_4, S_5, and S_7 provide conductivity path and source voltage (V_2) is present across the load displayed in Figure 2(d).

$+3V_{dc}$: The voltage source (V_3) connects to the load for this voltage level using S_1, S_3, S_6, and S_8, as shown in Figure 2 (e).

$+4V_{dc}$: To provide $+4V_{dc}$ as the output voltage level, switches S_1, S_3, S_5, and S_8 create a path of

conduction such that input voltage(V_3+V_1) is linked to the load displayed in Figure 2 (f).

+5V_{dc}: Switches S_1, S_4, S_6, and S_8 offer the current flow path from the source (V_3+V_2) to the load, attaining +5V_{dc} as the voltage level shown in Figure 2 (g).

+6V_{dc}: For this level, the source voltage (V_1+V_2+V_3) is available across the load through conductivity of S_1, S_4, S_5, and S_8 depicted in Figure 2(h).

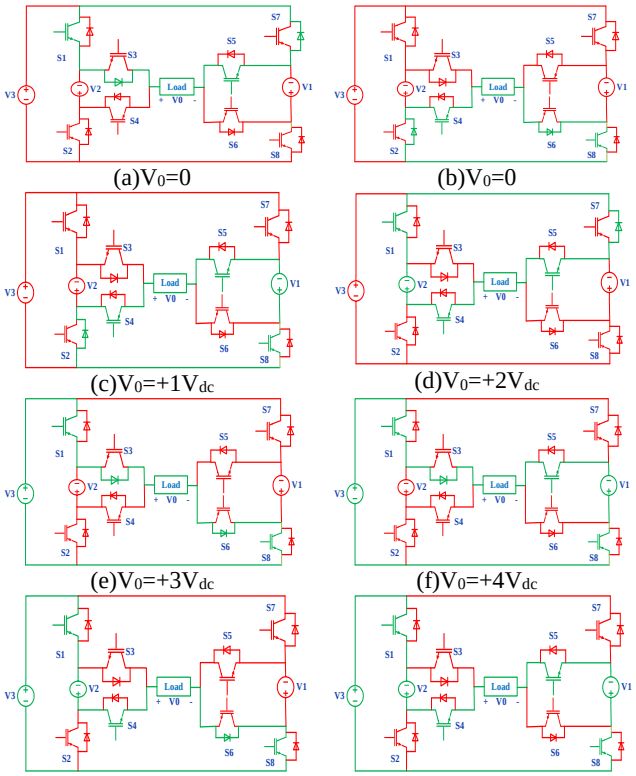


Fig. 2: Operating modes for positive &zero modes

2.1.2 Negative Mode

Figure 3 displays the modes of operation of the TSTL inverter for negative mode.

-1V_{dc}: Switches S_1, S_3, S_6, and S_7 conduct source voltage (V_1) across the load to produce this voltage level, as seen in Figure 3 (a).

-2V_{dc}: To generate -2V_{dc} across the load is depicted in Figure 3(b). By turning on the switches S_2, S_3, S_6, and S_8, the source voltage (V_2) associated with the load is established.

-3V_{dc}: Source voltage (V_3) links to the load via the turn-on of switches S_2, S_4, S_5, and S_7, as indicated in Figure 3(c).

-4V_{dc}: To create this voltage level, source voltage (V_1+V_3) comes across load via the conduction of S_2, S_4, S_6, and S_7. These conducting and non-conducting paths are depicted in Figure 3 (d).

-5V_{dc}: Switches S_2, S_3, S_5, and S_7 provide the conductivity path to appear source voltage (V_2+V_3) across the load at this level. This voltage level is depicted in Figure 3(e).

-6V_{dc}: Three source voltages are acting as a summer and link to the load via conductivity devices S_2, S_3, S_6, and S_7. This voltage level is depicted in Figure 3(f).

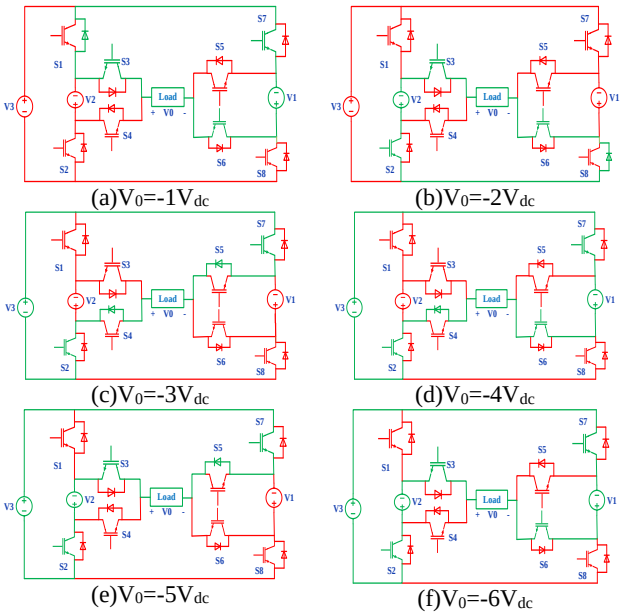


Fig. 3: Operating modes for negative mode

2.2 Modulation Scheme

The PDPWM scheme employing for TSTL inverter is represented in Figure 4. Since it is a thirteen-level inverter, it demands twelve carriers and one reference to send gating pulses to switches. Gating pulses are generated in this modulation scheme by comparing the reference wave to carrier signals. Gating pulses are formed in this modulation scheme employing the comparison of reference wave to carrier waves. Twelve pulses are developed after the comparison. Employing the logic provided in Table 1, these ten pulses generate signals to switches (S_1-S_8).

The peak value of the reference is altered to modify the amplitude of the modulation index (m_a). The reference and output waves have identical operating frequency i.e. fundamental frequency (50Hz). Frequency modulation is modulated by changing the carrier frequency($f_{carrier}$). The harmonic shifts to a greater order as the frequency modulation

grows, decreasing the filter size. Higher switching losses appear due to increased frequency modulation. As an outcome, the carrier frequency($f_{carrier}$) is limited to specified limits; for the present configuration, the carrier frequency is restricted to 5kHz.

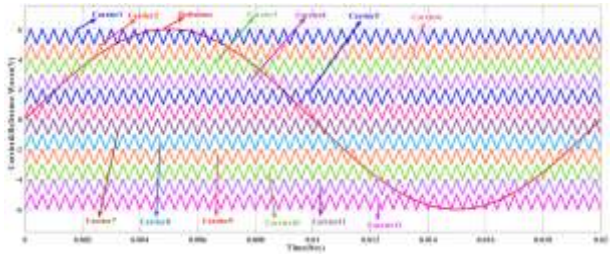


Fig. 4: PDPWM Scheme

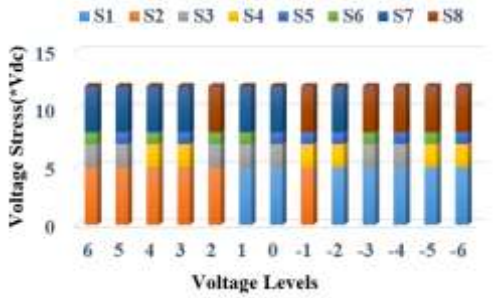


Fig. 5: Bar Chart representation of Voltage Stress

3 Voltage Stress and Loss Analysis

3.1 Voltage Stress

The maximum voltage stress of complementary switches has identical magnitudes for the TSTL inverter. The maximum voltage stress of devices is expressed as (1), (2), (3), and (4).

$$V_{s1} = V_{s2} = V_2 + V_3 = 5V_{dc} \quad (1)$$

$$V_{s3} = V_{s4} = V_2 = 2V_{dc} \quad (2)$$

$$V_{s5} = V_{s6} = V_1 = V_{dc} \quad (3)$$

$$V_{s7} = V_{s8} = V_1 + V_3 = 4V_{dc} \quad (4)$$

where V_{Sn} represents the peak voltage of the switch when it is turn-off.

For this structure, the total standing voltage (TSV) is denoted as equation (5)

$$TSV = 2 * (V_{s1} + V_{s3} + V_{s5} + V_{s7}) = 24V_{dc} \quad (5)$$

The proportion of sum of switch turn-off voltages to peak voltage seems through the load is *TSV* (p.u.). It is 4p.u. in the present state for the proposed topology. Figure 5 portrays a bar chart demonstrating the voltage stress of individual switching devices at various levels. Referring to Table 1, at $+6V_{dc}$ level, S_1, S_4, S_5, and S_8 are in turn on condition and the rest of the devices are in off condition for this level of operation. As shown in Figure 5, the voltage stress of S_2, S_3, S_6, and S_7 are $5V_{dc}$,$2V_{dc}$,$1V_{dc}$, and $4V_{dc}$ respectively. Switching stress voltages for switches S_2, S_3, S_5, and S_7 at $+5V_{dc}$ levels are $5V_{dc}$, $2V_{dc}$, $1V_{dc}$, and $4V_{dc}$, respectively. Figure 5 depicts the switching stress of the devices for the other levels in the same way.

3.2 Loss Analysis

Depending on the unique characteristics and application requirements, using nonlinear electronic diodes in inverter design can present both opportunities and challenges. In frequency-generating and mixing circuits, these are frequently used. They can be applied in specific situations to produce harmonics or integrate various frequencies. Nonlinear components may increase the inverter circuit's losses, which would lower its overall efficiency. When creating an inverter with high efficiency, controlling these losses becomes essential.

Switching and conduction losses are distinct classifications of power losses experienced by switching devices. Conduction losses are brought on by on-state resistance while switching losses are a result of delays in the switch's on/off processes. It is possible to express the switching loss during the turn-on process as

$$P_{swlturnon}(i) = f_{carrier} \int_0^{t_{on}} v(t).i(t)dt = \frac{1}{6} f_{carrier} * V_{sw,i} * i_{on,i} * t_{on} \quad (6)$$

$$P_{swlturnoff}(i) = f_{carrier} \int_0^{t_{off}} v(t).i(t)dt = \frac{1}{6} f_{carrier} * V_{sw,i} * i_{off,i} * t_{off} \quad (7)$$

In this case, $P_{swlturnon}$ *(i),* $P_{swltunoff}$*(i),* and V_{sw} stand for the ith switch's turn-on, turn-off loss, and off-state switching voltage respectively. Currents during the switch's on- and off-states, respectively, are called I_{on} and I_{off}. In terms of the number of switches on (N_{swon}) and the number of switches off (N_{swoff}), the relationship between carrier frequency ($f_{carrier}$) and modulating frequency (f_m) is

$$N_{swon} = N_{swoff} = \frac{f_{carrier}}{f_m} \quad (8)$$

Total switching losses (P_{sw}) are calculated by summing turn-on and turn-off losses.

$$P_{sw}\left(Total\right)=\sum_{i=1}^{N_{sw}}\left(\sum_{j=1}^{N_{on}(i)}P_{swlon}\left(ij\right)+\sum_{j=1}^{N_{off}(i)}P_{swloff}\left(ij\right)\right) \quad (9)$$

where N_{sw} is the total number of switches of the proposed MLI.

Conduction losses appear in a switch during the conduction period due to on-state resistance and voltage drop across the switch. The generalized equation for conduction losses of the diode and switch is as follows:

$$P_{Dcon}=V_{Don}*i_{Davg}+R_{Don}*i_{Drms}^{2} \quad (10)$$

$$P_{swcon}=V_{swon}*i_{swavg}+R_{swon}*i_{swrms}^{2} \quad (11)$$

where P_{Dcon} and P_{swcon} are diode and switch conduction losses, and V_{don} and V_{swon} are on-state voltage drops of diode and switch respectively. R_{Don} and R_{swon} are on-state resistances of the diode and switch, i_{Davg}, i_{swavg}, $i_{Drms,}$ and i_{swrms} are average and RMS currents of the switch respectively.

Table 2.Comparison with other topologies

Topology	N_{sw}	$N_{drivers}$	N_{diodes}	N_c	N_S	***TSV (p.u)***
[20]	9	9	0	2	2	5.33
[21]	10	8	0	0	4	5.33
[22]	10	10	2	0	4	4.5
[23]	10	8	0	0	4	4
[24]	8	8	2	0	4	5
Proposed	8	8	0	0	3	4

4 Comparison

By regulating electricity from distinct distributed energy resources (DERs) such as solar, and wind, along with energy storage systems, multisource inverters are essential to islanded microgrid systems. Wind turbines and photovoltaic power are coupled employing multisource inverters. They successfully deal with these renewable energy sources' erratic and sporadic characteristics. Hybrid UPS systems with multisource inverters are employed in applications in which uninterrupted electricity is vital. In the event of a grid interruption, these networks incorporate multiple power sources to ensure a consistent supply of power and backup.

Table 2 contrasts TSTL with various novel designs for thirteen-level operation. The number of switches, drivers, diodes, capacitors requirement, DC sources, and TSV (p.u.) are the comparison aspects. [20], has fewer switches count and requires two dc sources and two capacitors, however, it suffers from voltage imbalance of capacitors and greater TSV (p.u).

In [21], [22] and [23], the requirement of switch count and sources is more concerning other topologies. In contrast to other designs, [24], makes better use of switch count but it suffers from voltage imbalance of capacitors. Taking everything into consideration, the TSTL inverter requires minimal component count and dc sources along with reduced TSV. It exhibits that the proposed design outcome exhibits sophisticated results.

5 Results& Discussions

5.1 Simulation Results

MATLAB/Simulink platform is utilized for simulating the execution of thirteen-level operation. The source voltages for the thirteen level are categorized as (50V,100V, and 100V) and load parameters are 100Ω and100mH respectively. The frequency at which it operates of the suggested inverter is the fundamental frequency(50Hz). The performance of the inverter for R-load is depicted in Figure (6). Sensitivity analysis is the study of how a system's output reacts to changes or uncertainties in its parameters. This is used to comprehend how changes in important parameters impact an inverter's ability to convert DC power to AC power. The following are some essential inverter sensitivity analysis parameters considered for simulation. The output current appears to be in proportion to the output voltage. Figure 7 represents the inverter's outcomes for thirteen-level operations under various load scenarios.

According to Figure 7, it indicates that output voltage remains constant irrespective of load scenarios, however current is null during unloading, implying voltage for Resistive loads and delays for inductive loads. Figure 8 depicts variations of waveforms related to inductive load fluctuations. Figure 8 shows that as inductance increases, the current falls due to high inductive load leads more lagging of current.

Figure 9 presents the resultant voltage as well as current as the modulation index (m_a) alterations. Figure 9 shows that twelve carriers are contrasted to one reference for 1,0.9 values, yet the size of the waveform reduces for the 0.9 value. Similarly, for the 0.7 value waveform level is lowered and changed to eleven-level. For 0.6 and 0.4 values it functions as a nine-level and seven-level respectively. Comparably for a 0.2 value, it is working as a three-level via contrast of two carriers to reference.

Figure 10 represents the resulting waveforms as the reference frequency(f_m) fluctuates. According to Figure 10, enhancing the reference frequency(f_m) leads to a rise in load inductance. Since incremental load inductance impacts total load impedance, load current falls as reference frequency goes up. The proposed topology appears to be suitable for high-frequency performing appliances.

Figure 11 depicts load waveforms as the carrier frequency alterations. The pulses count for individual level boosts as a carrier frequency($f_{carrier}$) rises. Consequently, the harmonics shifts upwards in order and the size of the filter is reduced. As the carrier frequency ($f_{carrier}$) expands, switching losses elevate due to an increase in pulse count for each voltage level.

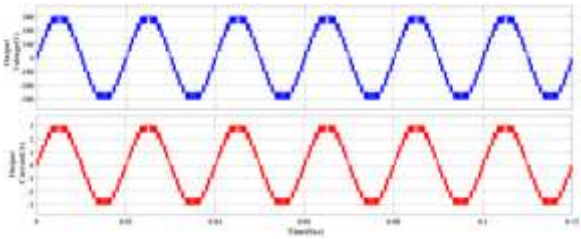


Fig. 6: Waveforms for Resistive-Load

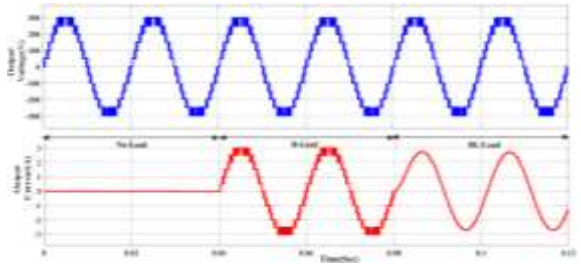


Fig. 7: Waveforms for distinct Load scenarios

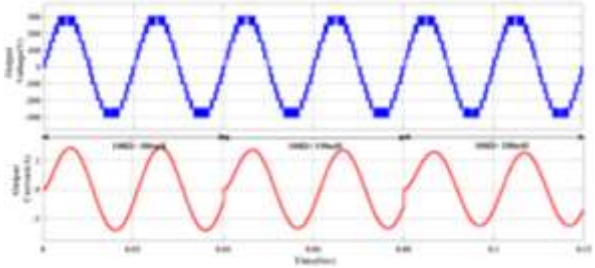


Fig. 8: Waveforms for different RL-Loads

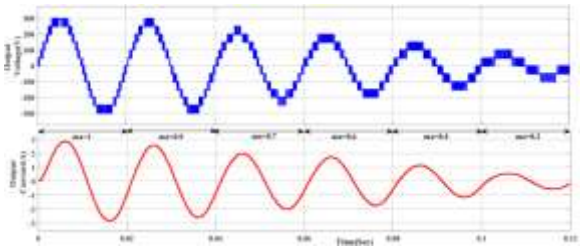


Fig. 9: Resultant Waveforms for modification in the modulation index

Table 3. %THD analysis for various modulation indices

Modulation Index(ma)	*Fundamental Voltage(V)*	*THD (%)*
1	299.2	9.69
0.9	269.1	11.26
0.7	208.1	13.81
0.6	180	17.22
0.4	120.2	25.05
0.2	59.41	46.31

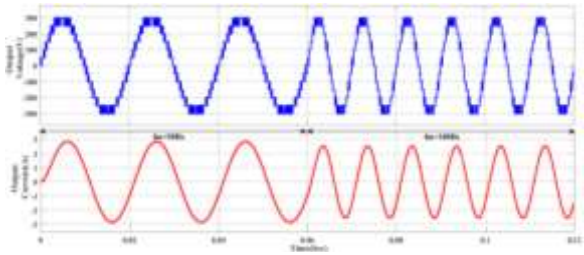


Fig. 10: Load waveforms for regulation in reference frequency

Figure 12 shows thirteen-level inverter's resultant voltage THD is 9.69% and the fundamental output of 498.8 volts. Table 3 displays the variation of the modulation index related to THD (%) along with fundamental output. The switching sequences of devices (S_1, S_3, S_5, and S_7) are depicted in Figure 13 and the rest are in complementary mode. By the simulation outcome, the suggested inverter works for all conditions of load.

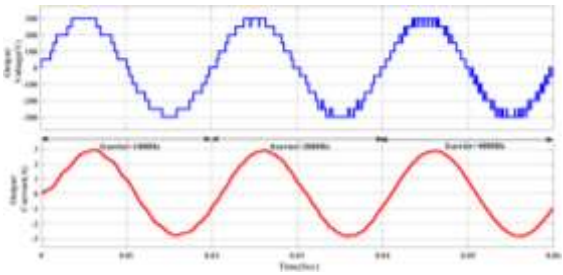


Fig. 11: Load Waveforms for carrier frequency alterations

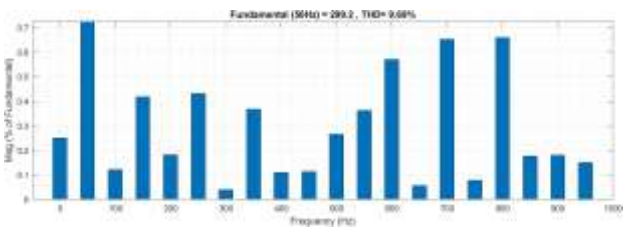


Fig. 12: %THD of resultant voltage

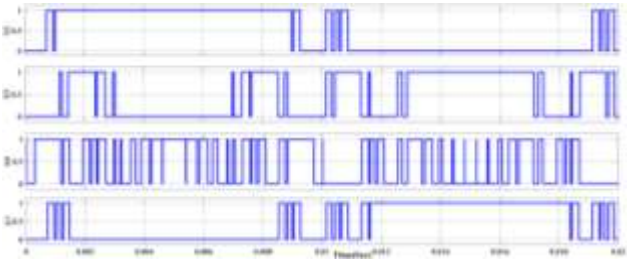
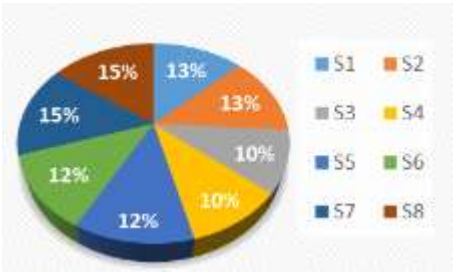


Fig. 13: Switching pattern of switches

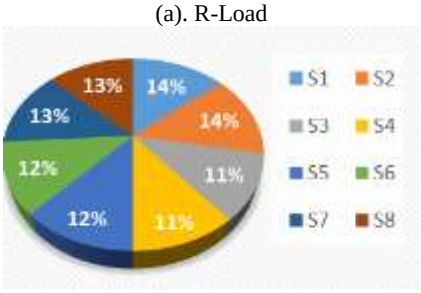
Artificial intelligence (AI) techniques, such as Expert Systems and other AI methods, can facilitate the design of circuits. Computer programs known as expert systems simulate a human expert's decision-making process in each field. An expert system for circuit design might be created to record the wisdom and skill of seasoned circuit designers. It can support troubleshooting, parameter optimization, and component selection. AI algorithms can be used to automate the process of design. For example, circuits that satisfy requirements can be evolved through design space exploration using genetic algorithms. When dealing with optimization problems that involve numerous variables and constraints, this method is especially helpful. Using machine learning (ML) techniques, one can identify patterns and correlations about circuit performance, failures, or optimizations in sizable datasets. From past data, machine learning models can be trained to forecast circuit behavior or suggest design modifications. Virtual design and circuit simulation can be improved with AI techniques. They can accelerate simulation procedures, enabling more iterations and quicker design cycles.

5.2 Thermal Modelling

The objective of the PLECS software is to thermally model devices as per the proposed topology. Figures 14(a) and (b) display the percentage of losses of switches for resistive and inductive load respectively. The efficiency of the system is estimated by using just R loads and shown about the output power (0-5000W). As illustrated in Figure 15, the effectiveness ranges from 98.5% to 96.8%. Since the load rises, the efficiency reduces. Since demand grows, conduction losses increase, causing temperatures to rise and efficiency to decrease.



(a). R-Load



(b). RL-Load

Fig. 14: Switching Losses

Fig. 15: Efficiency Curve

5.3 HIL Implementation

The simulated results are verified utilizing OPAL-RT(OP4510) tested in a Hardware-in-loop environment. Real-time simulations serve as vital to developing and evaluating system performance and certainty since they operate at the identical evaluate as systems in the real world. The OPAL-RT simulator interacts with the Sim Power System in MATLAB/Simulink using the RT-LAB software. The OP4510 pertains to the OPAL-RT RT-LAB and eFPGAsim real-time platforms, in addition to sophisticated Intel processors along with FPGA chips. This multi-rate FPGA-based design enables consumers to design power converters for the HIL program using limited time steps of less than seven s for INTEL CPU-based sections for a period of a smaller nanosecond on the FPGA chip. The OP4510 is also suitable for use as a standalone electronic test system with pre-programmed models. The TSTL configuration is executed by OP4510 as indicated in Figure 16 and represented in this section.

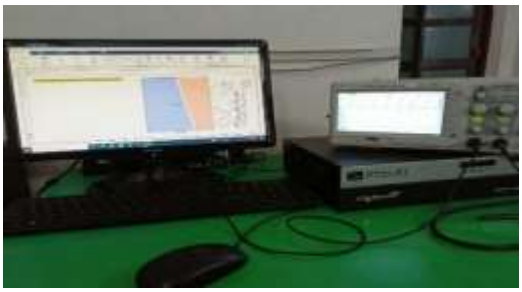


Fig. 16: OPAL-RT Test Bench

Figure17 and 18 display waveforms for load impedance as 100 Ω and 100 Ω +100mH for carrier frequency of 5kHz. Figure 17 and Figure 18 shows that output current implies voltage for Resistive load and delays for inductive load. Figure 19 indicates the pulses of all the devices. All these real-time results show that the proposed topology performs well suitable for all loading conditions corresponding to proposed modulation technique, despite the need for additional regulation methods.

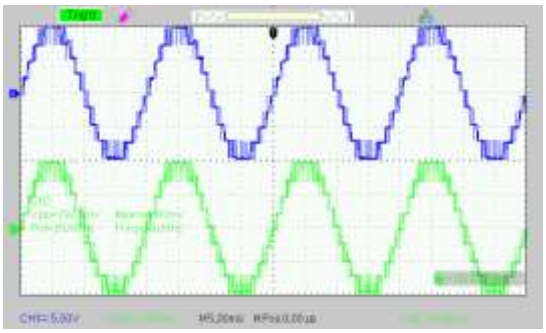


Fig. 17: Output Waveforms for R-Load

When practically designed the efficacy of inverter structures gets affected by many kinds of mistakes or defects. Identifying and resolving problems effectively requires doing an error analysis. For thermal analysis take a temperature reading of the inverter's parts under both working and malfunctioning conditions. By Checking the cooling system and enough ventilation should be provided. To find out communication errors, examine the connections, settings, and communication cables. Before going to run the device Check to make sure the communication protocols are set up correctly. To identify ground faults, verify for insulation flaws, investigate grounding connections, and conduct a ground fault test. If the solar panel is utilized as input observe the input side voltages and currents. Look for damage, shading, or other problems with the solar panel array. Employing power quality analysis harmonics and electromagnetic interface are identified, by placing proper filter size the above problems are mitigated. To identify mechanical failures, physical damage to inverter, loose connections, and signal wear are considered. If issues are taken place damaged components are replaced.

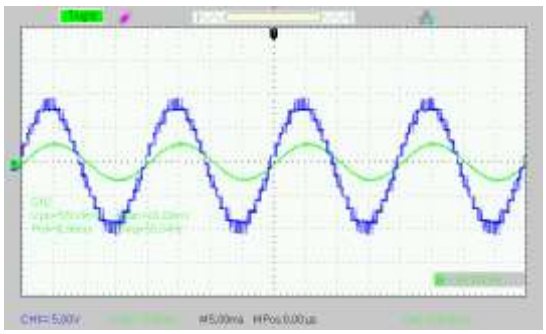
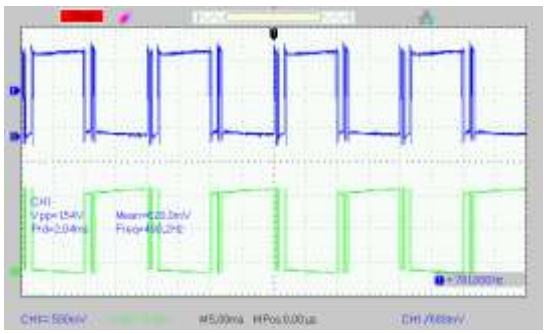
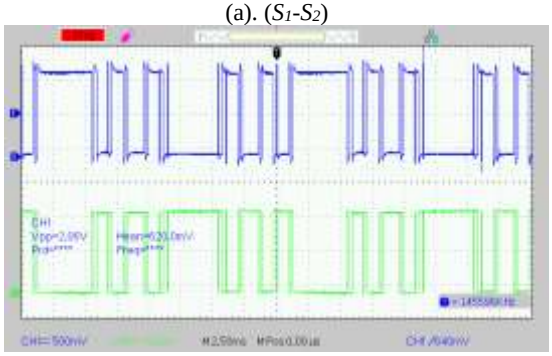
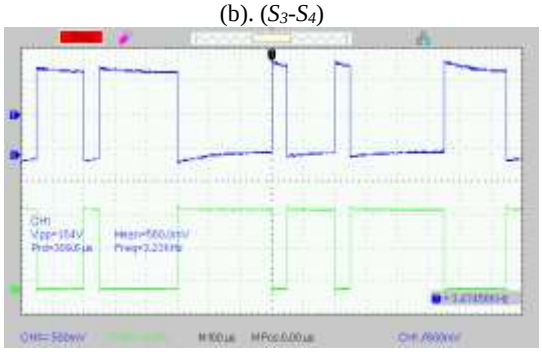
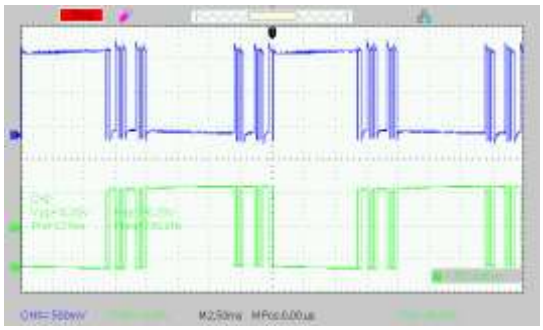


Fig. 18: Output Waveforms for RL-Load


(a). (S_1-S_2)


(b). (S_3-S_4)


(c). (S_5-S_6)



(d). (S_7-S_8)

Fig. 19: Switching Pulses

6 Conclusion

The present work discusses a new thirteen level inverter with numerous capabilities. The above configuration is simulated in MATLAB/Simulink employing various situations such as load, source voltage, modulation index, reference frequency, and carrier frequency variations. Consequently, the proposed configuration is appropriate for all loading facilities. This proposed design is compared to other topologies in the literature to determine its superior features. The proposed topology employs the fewest switches and components while maintaining an acceptable TSV (p.u.). The overall performance of this configuration is also determined by estimating switch losses with the PLECS software. Finally, the successful execution of this structure is examined through the OPAL-RT test bench and results are presented. The results show that the suggested configuration is efficient.

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The authors have no conflicts of interest to declare.