Performance Augmentation, Parameter Modeling and Analysis of Nano-DG-TFET

YASHU SWAMI
Department of ECE,
Aditya Engineering College (A),
Surampalem 533437,
INDIA

Abstract: - In this manuscript, we propose and analyze the properties of an efficient Nano strained-silicon dual-halo high-K dielectric stacked multi-material dual-gate TFET device (Nano-DG-TFET). Compact precise models for this projected Nano TFET are mathematically proposed for the electric field, surface potential, drain current and threshold voltage. Using gate and channel (G&C) engineering, the models are derived by solving the 2-D Poisson equation in silicon-graded channel region by applying suitable boundary conditions. The real-time values of the devices diverge due to various SCEs, second-order effects, and non-idealities present in the device. Hence, the proposed models incorporate the effects of various device parameters such as channel potential, electric field, DIBL, threshold voltage roll-off, and drain current. Also, the fringing capacitance characteristics of the proposed Nano-DG-TFET demonstrate superior performance over Triple Material Double Gate (TMDG) and Single Material Double Gate (SMDG) TFET structures. The proposed Nano-DG-TFET incorporates many other efficient device properties like strained silicon (s-Si) channel, halo implantation, high-K dielectric gate stack, triple material gate terminal, and many more. Therefore, it is evident that the proposed nanodevice structure provides poor outflow current I_{OFF} (10^{-16}A/µm), and remarkable betterment in ON current I_{ON} (10^{-6}A/µm). The results are demonstrated by extensive 2-D TCAD simulation and confirmed analytically at various technology nodes to validate the robustness of the model.

Key-Words: - Dual-Gate TFET, Threshold Voltage, Dual-Halo, high-K Dielectric, Fringing capacitance, Strained Silicon, Short Channel Effects.

Received: May 3, 2024. Revised: November 13, 2024. Accepted: December 3, 2024. Published: December 31, 2024.

1 Introduction

To augment the device performance and suppress Short Channel Effects (SCE), we need to upgrade the device structure and properties. An efficient Nano strained-silicon dual-halo high-K dielectric stacked multi-material dual-gate TFET device (Nano-DG-TFET) is proposed with enhanced properties. To improve the device carrier properties we use Strained-Silicon (s-Si) material in designing the device, [1], [2]. This improves the lattice crystalline quality and conducting properties of the layer.

Along the Si/SiO_2 interface, the lateral electric field in Nano-DG-TFET generates fixed charges. Because of the Hot Carrier effects (HCEs), these fixed charges lead to the degradation of the current drive capability of the nanodevice, [3], [4]. Furthermore, because of this HCEs, the damaged interface region extends from drain to source with fixed charge density. A number of researchers have investigated the fixed charge degradation in DG TFETs, further stating that these localized charge carriers are trapped in the Si/SiO_2 interface, [5]. For enhancement in output characteristics like low DIBL, higher drive currents, and flatter saturation level, we can use halo implantation in our device. This also improves the breakdown voltages of TFET. The proposed Nano-DG-TFET shows a significant reduction in SCE. We observe the decline in threshold voltage (V_{TH}) value with falling channel length (L) and increasing drain voltage (V_{DS}). This contrary SCE V_{TH} roll-off effect is the barricade to the upcoming TFET technologies.

In this manuscript, we also demonstrate the influence of using multiple gate materials in the enhancement of proposed DG TFET electrical parameters like surface potential, the electric field drain current (I_D). The work function of the drain-side gate material (M3) is lower than the source-side gate material (M1). Using this multi-gate material technology, the V_{TH} performance is also enhanced by the Nano-DG-TFET structure, [6], [7]. Therefore, in the source-side gate region (tunneling gate), we obtain step-equivalent profile potential.

The tunneling gate region (auxiliary gate) is partitioned from V_{DS} beyond saturation because the auxiliary gate ingests additional V_{DS}, limiting the SCEs. In the tunneling area, we used germanium as the source material and intrinsic silicon as the channel material, making a hetero-junction. Furthermore, G&C engineering is also used in our proposed Nano-DG-TFET to lower both SCEs and HCEs, [8].

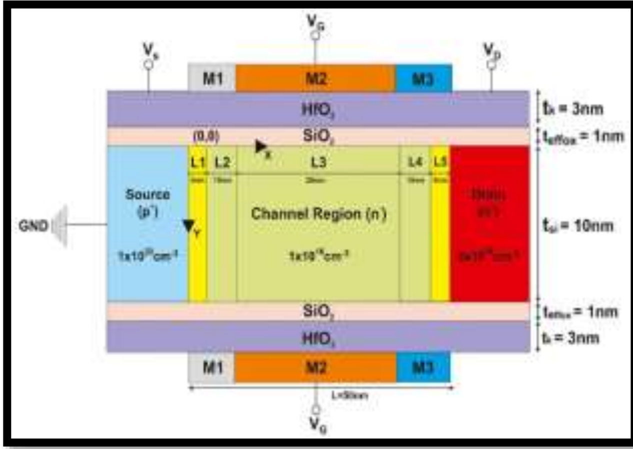

Fig. 1: 2-D sketch of the proposed nanodevice structure (Nano-DG-TFET)

Many researchers have already described numerous analytical approaches for obtaining V_{TH} features of SOI and DG-TFETs, [9], [10]. The analytical model of s-Si on Silicon-Germanium-on-Insulator TFET, V_{TH} and roll-off approach is developed in [10]. Furthermore, the parameters of effective gate oxide and channel were carefully chosen to improve V_{TH} and roll-off. Few research works have developed a 2-D analytical modeling of ambipolar characteristics for asymmetric TFETs, how different front-gate and back-gate biases affect the position of the charge centroid and anticipated the range and straggle parameter to optimize V_{TH} and roll-off characteristics. However, no work has shown the analytic modeling of V_{TH} and effective oxide thickness (t_{OX}) of dual-halo high-K dielectric stacked Triple-Material DG-TFET with SCEs. With the development of substrate bias, a significant quantity of body impact coefficient causes large variation in V_{TH}, adding complexity to the circuit design. Double halo doping has been used as a sort of G&C engineering to manage these outcomes. A compact model is proposed for fully depleted nano-scale dual-halo high-K dielectric stacked Triple-Material DG-TFET. The model formulation has been mathematically proposed for the electric field, surface potential, I_D and V_{TH}. The proposed mathematical models incorporate the device properties like fixed charge density at HfO_2/SiO_2 stacked oxide interface, t_{OX} and numerous device parameters applied to 2-D Poisson equation. Hence, the projected models are in accord with the obtained TCAD simulation results.

2 Device Structure and Modeling

Figure 1 shows a 2-D sketch of the proposed nanodevice structure. The acronyms L, t_{si}, Φ_M, N_{Ah}, and t_{OX} denote channel length, silicon channel thickness, work functions of triple metal gate materials, halo doping concentration, and silicon t_{OX}, respectively. The Source and Drain are uniformly halo doped with N_S and N_D concentrations individually. The gate work function parameters for M1, M2, and M3 are shown in Table 1. M2 work function is kept higher than others to attain a high I_{ON} to I_{OFF} ratio.

The gate bias voltage (V_{GS}) controls the operation of the proposed Nano-DG-TFET. The ON state of an n-type DG-TFET is determined by increasing the positive V_{GS}, which lowers the energy barrier between the germanium source and the intrinsic region. That is, the intrinsic energy bands are pushed down, and electrons tunnel from the valence band of the $p+$ doped germanium source to the conduction band in the intrinsic silicon body, a process known as Band-To-Band Tunneling (BTBT). Drift-Diffusion then transports the electrons to the $n+$ doped drain region.

Table 1. TCAD Device Simulation Parameters

Parameter	Value
Channel Length, (L)	50nm
Source Doping, N_S(p-type)	1×10^{20} cm^{-3}
Drain Doping, N_D(n-type)	5×10^{18} cm^{-3}
Halo Doping concentration (N_{Ah})	1.2×10^{18} cm^{-3}
Channel thickness (t_{si})	10 nm
Metal M1 Work function (ϕ_{M1})	4.2 eV
Metal M2 Work function (ϕ_{M2})	4.6 eV
Metal M3 Work function (ϕ_{M3})	4.0 eV
Effective oxide thickness (t_{ox})	1 nm
Exterior Fringing Field Capacitance, C_{11}	0.63 fF
Direct overlap Capacitance, C_{22}	3.23 fF
Internal Fringing Field Capacitance, C_{33}	1.06 fF
Channel Width capacitance, W_C	18.07 fF
Body effect Coefficient, γ	0.58 V$^{1/2}$

The suggested device will have improved control over the vertical field because of the gate work function engineering and high-K dielectric Hafnium Oxide (HfO_2) used as the gate dielectric in the stack. This reduces the infiltration of hot careers through the interface and increases the TFET performance.

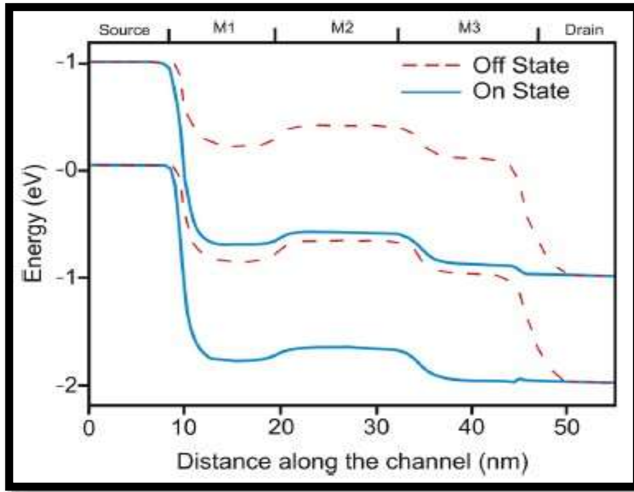

Fig. 2: Energy Band Diagram of proposed Nano-DG-TFET

The ON-OFF state career concentration profiles of the proposed Nano-DG-TFET are shown in Figure 2. It clearly illustrates that because the S-C has a narrow bandgap, the tunneling width (λ) of the careers traveling from S-C is small. As a result, the tunneling rate of the careers moving through S-C is boosted, improving the device ON current (I_{ON}). The use of HfO_2/SiO_2 as gate oxide for TFET devices has been reported to enhance I_{ON}. Although high-K gate dielectrics provide improved device properties, they also cause faults in the dielectric/silicon interface when fabricated on top of the silicon surface.

3 Formulation of the Model

Compact precise analytical models of the device properties for the projected Nano-DG-TFET are mathematically derived and proposed in this section. The logical equations for surface potential, electric field, I_D and V_{TH}, all have been discussed. Applying G&C engineering, the models have been formulated using 2-D Poisson equation. Short-channel effects are also reinforced. As a result, an authentic model of the proposed Nano-DG-TFET is developed.

3.1 Nano-DG-TFET Surface Potential and Electric Field Model

In the channel region, the surface potential, using the 2-D Poisson equation, can be expressed as:

$$\frac{d^2\emptyset_i(x,y)}{dx^2}+\frac{d^2\emptyset_i(x,y)}{dy^2}=\frac{qN_{avgeff}}{\epsilon_{si}}; \quad i=1,2,3,4,5 \tag{1}$$

We neglected the influence of mobile charge carriers on the electrostatics of the channel. In eq (1), electrostatic potential difference (Φ_i (x,y)), electron charge (q), electrical permittivity of silicon (ϵsi) are used. N_{avgeff} is the average doping concentration for a uniform doping concentration profile.

The Poisson equation can be solved using the parabolic approximation technique, and the result is as follows:

$$\emptyset(x,y)=C_{i0}(x)+C_{i1}(x)y+C_{i2}(x)y^2; \quad i=1,2,3,4,5 \tag{2}$$

$C_{i0}(x)$, $C_{i1}(x)$, and $C_{i2}(x)$ are arbitrary x functions that can be resolved using the frontier conditions. The border conditions are required to solve this equation. The frontier conditions for frontal and backward semiconductor oxide interfaces are as follows:

$$\frac{d\emptyset_i(x,y)}{dy}|_{y=0}=\frac{\epsilon_{SiO2}\left[\emptyset_{Si}(x)-V_{GS}+V_{fbi}\right]}{\epsilon_{Si}\ t_{ox}} \tag{3}$$

$$\frac{d\emptyset_i(x,y)}{dy}|_{y=t_{Si}}=-\frac{\epsilon_{SiO2}\left[\emptyset_{Si}(x)-V_{GS}+V_{fbi}\right]}{\epsilon_{Si}\ t_{ox}} \tag{4}$$

Where t_{Si} denotes channel thickness and V_{fbi} denotes the flat-band potential drops of 1,2,3,4 and 5 regions. It can be represented as:

$$V_{fbi}=\Psi_{mi}-\left[\chi_{Si}+\frac{E_{gsi}}{2q}+\Psi_F\right]-\frac{Q_0}{C_{ox}}; \quad i=1,2,3,4,5 \tag{5}$$

Ψ_F, χ_{si}, Q_0 and E_{gsi} are the Fermi potential drop, electron affinity, effective surface charge, and silicon energy band gap.

Surface potential interface for different regions can be calculated as follows:

For region 1 - region 2 interface:

$$\emptyset_1(L_1,0)=\emptyset_2(L_1,0) \tag{6}$$

$$\frac{d\emptyset_1}{dx}|_{x=L_1}=\frac{d\emptyset_2}{dx}|_{x=L_1} \tag{7}$$

For region 2 - region 3 interface:

$$\emptyset_2(L_1+L_2,0)=\emptyset_3(L_1+L_2,0) \tag{8}$$

$$\frac{d\emptyset_2}{dx}|_{x=L_1+L_2}=\frac{d\emptyset_3}{dx}|_{x=L_1+L_2} \tag{9}$$

For region 3 - region 4 interface:

$$\emptyset_3(L_1+L_2+L_3,0)=\emptyset_4(L_1+L_2+L_3,0) \tag{10}$$

$$\frac{d\emptyset_3}{dx}|_{x=L_1+L_2+L_3}=\frac{d\emptyset_4}{dx}|_{x=L_1+L_2+L_3} \tag{11}$$

For region 4 - region 5 interface:

$$\emptyset_4(L_1+L_2+L_3+L_4,0)=\emptyset_5(L_1+L_2+L_3+L_4,0) \tag{12}$$

$$\frac{d\emptyset_4}{dx}|_{x=L_1+L_2+L_3+L_4} = \frac{d\emptyset_5}{dx}|_{x=L_1+L_2+L_3+L_4} \quad (13)$$

Surface potential interfaces at the S-C and D-C can be calculated as:

$$\emptyset_1(0,0) = V_{bi} + V_{FS} \quad (14)$$

$$\emptyset_5(L_1+L_2+L_3+L_4+L_5, 0) = V'_{bi} + V'_{DS} + V'_{FD} \quad (15)$$

The built-in potential (V_{bi}) is represented as:

$$V_{bi} = V_T\, ln\left(\frac{N_{Ah}N_{DS}}{n_i^2}\right) \quad (16)$$

Halo doping concentration around the S-C and D-C regions is symbolized by N_{DS} and N_{Ah} respectively.
Using y = 0 in (2), we get:

$$C_{i0}(x) = \emptyset_i(x,0) = \emptyset_{Si}(x) \quad (17)$$

Using the derivative of (2) in (3) and (4), we get:

$$C_{i1}(x) = \frac{\epsilon_{SiO2}\left[\emptyset_{Si}(x) - V_{GS} + V_{fbi}\right]}{\epsilon_{Si}\ t_{ox}} \quad (18)$$

$$C_{i2}(x) = -\frac{\epsilon_{SiO2}\left[\emptyset_{Si}(x) - V_{GS} + V_{fbi}\right]}{\epsilon_{Si}\ t_{ox}\, t_{Si}} \quad (19)$$

Substituting (17), (18) and (19) in surface potential base equation (2), we get

$$\emptyset(x,y) = \emptyset_{Si}(x) + \frac{\epsilon_{SiO2}\left[\emptyset_{Si}(x) - V_{GS} + V_{fbi}\right]}{\epsilon_{Si}\ t_{ox}} y - \frac{\epsilon_{SiO2}\left[\emptyset_{Si}(x) - V_{GS} + V_{fbi}\right]}{\epsilon_{Si}\ t_{ox}\, t_{Si}} y^2 \quad (20)$$

The characteristic length (λ) of the device is also considered in modeling surface potential as it helps in extracting the amount of electric field inflowing through the drain region. It also assists in modeling the SCE influence on the proposed nanodevice characteristics. As a result, we will be able to develop a robust model.

Using the Poisson equation, a better characteristic length value appears at the intermediate channel region.

$$\lambda = \sqrt{\frac{t_{Si}^2\left(1+\frac{r_{oc}}{4}\right)}{2r_{oc}}} \quad (21)$$

Hence, the channel potential in the intermediate region can be expressed as:

$$\emptyset_{Ci}(x) = \emptyset_i(x,y)|_{y=t_{Si}/2} \quad (22)$$

Using (18) – (20), we simplify (22) as:

$$\emptyset_{Ci}(x) = \emptyset_{Si}(x)\left(1+\frac{r_{oc}}{4}\right) - \frac{r_{oc}}{4}\left(V_{GS} - V_{fbi}\right) \quad (23)$$

The r_{oc} represents the gate oxide to channel capacitance ratio represented as $r_{oc} = \frac{\epsilon_{SiO2}t_{Si}}{\epsilon_{Si}t_{ox}}$

Solving (1) for the intermediate channel, we get:

$$\frac{d^2\emptyset_{Ci}(x)}{dx^2} - \frac{\emptyset_{Ci}(x)}{\lambda^2} = \frac{qN_{avgeff}}{\epsilon_{si}} - \left(\frac{\left(V_{GS}-V_{fbi}\right)}{\lambda^2}\right) \quad (24)$$

Simplifying (24), we can frame it as:

$$\emptyset_{Ci}(x) = M_i e^{Tx} + N_i e^{-Tx} - \frac{\beta_i}{\tau^2} \quad (25)$$

$$\beta_i = \frac{qN_{avgeff}}{\epsilon_{si}} - \left(\frac{\left(V_{GS}-V_{fbi}\right)}{\lambda^2}\right) \quad (26)$$

and $\tau = \frac{1}{\lambda}$ (27)

Using (3) – (15) along with the frontier equation, the *Mi* and *Ni* can be mathematically extracted. Appendix 1 lists the expression of *Mi* and *Ni* for *i* =1,2,3,4,5.

Now the surface potential can be precisely modeled using (20), (23), (25) along with Appendix 1. It may be formulated as:

$$\emptyset_i(x,y) = \left[\frac{M_i e^{Tx} + N_i e^{-Tx} - \frac{\beta_i}{\tau^2} + \frac{r_{oc}}{4}\left(V_{GS}-V_{fbi}\right)}{\left(1+\frac{r_{oc}}{4}\right)}\right] x \left(1 + \frac{r_{oc}}{t_{Si}} y - \frac{r_{oc}}{t_{Si}}^2 y^2\right) - \frac{r_{oc}}{t_{Si}}\left(V_{GS} - V_{fbi}\right) y + \frac{r_{oc}}{t_{Si}}^2 \left(V_{GS} - V_{fbi}\right) y^2;\ i = 1,2,3,4,5 \quad (28)$$

Simplifying (28), the compact model for surface potential can be expressed as:

$$\emptyset_{Si}(x) = \left[\frac{M_i e^{Tx} + N_i e^{-Tx} - \frac{\beta_i}{\tau^2} + \frac{r_{oc}}{4}\left(V_{GS}-V_{fbi}\right)}{\left(1+\frac{r_{oc}}{4}\right)}\right] \quad (29)$$

The electric field pattern along the channel determines the electron transit speed. It's calculated by differentiating the channel potential. The lateral and vertical electric fields can be calculated as follows:

$$E_{xi}(x) = \frac{d\emptyset_i(x,y)}{dx}|_{y=0} = \left[M_i e^{Tx} + N_i e^{-Tx} - \frac{\beta_i}{\tau^2}\right] \quad (30)$$

$$E_{yi}(x) = \frac{d\emptyset_i(x,y)}{dy} = \left[C_{i1}(x) - 2yC_{i2}(x)\right] \quad (31)$$

3.2 Nano-DG-TFET V_{TH} Model

V_{TH} is the voltage applied to the gate in region-1 where the energy barrier begins to saturate. For area 2, the derivative of (29) is equal to zero. As a result, x_{min} defined as the minimum surface potential is shown as:

$$x_{min} = 0.5\lambda \ln \frac{N_2}{M_2} \quad (32)$$

Using (32) in (29), the x_{min} can be simplified as:

$$\emptyset_{S,min} = 2\sqrt{M_2 N_2} - \frac{qN_{avgeff}}{\epsilon_{si}\tau^2} + \left(V_{GS} - V_{fb2}\right) \quad (33)$$

The V_{TH} condition is described as follows:

$$\emptyset_{S,min} = 2\Psi_F \quad (34)$$

and

$$V_{GS} = V_{TH} \quad (35)$$

The V_{TH} condition has been determined using (33–35):

$$2\sqrt{M_2^{th} N_2^{th}} - \frac{qN_{avgeff}}{\epsilon_{si}\tau^2} + \left(V_{TH} - V_{fb2}\right) = 2\Psi_F \quad (36)$$

For $V_{GS} = V_{TH}$, the $M_2^{th} = M_2$ and $N_2^{th} = N_2$; The V_{TH} can be derived using (36).

$$PV_{TH}^2 + QV_{TH}^2 + R = 0 \quad (37)$$

The coefficients used in (37) are described as below.

$$P = 1 + 4\left(k_2 + \sqrt{k_2}\right) - k_7 - k_8 \quad (38)$$

$$Q = -(2V_{THL} + 4k_1 + k_6 + 2k_5k_7 + k_5k_8) \quad (39)$$

$$R = V_{THL}^2 - (4k_3 + k_4 + k_5k_6 + k_5^2k_7) \quad (40)$$

In Appendix 2, the formulas for V_{THL} and $K_1 - K_8$ are simplified.

The analytical solution for V_{TH} can be expressed as:

$$V_{TH} = \left(\frac{-Q+\sqrt{Q^2-4PR}}{2P}\right) \quad (41)$$

The difference between the V_{TH} short channel - long channel TFET is numerically characterized as the V_{TH} roll-off.

It can be formulated as follows:

$$V_{roll-off} = V_{TH} - V_{THL} \quad (42)$$

The long channel V_{TH} is V_{THL}, and it is assumed to be independent of L. In Appendix 2, has been used to express it.

The rate of transition from V_{TH} to V_{DS} has also been defined as the DIBL. It can be formulated as:

$$DIBL = \frac{V_{TH1} - V_{TH2}}{V_{DS1} - V_{DS2}} \quad (43)$$

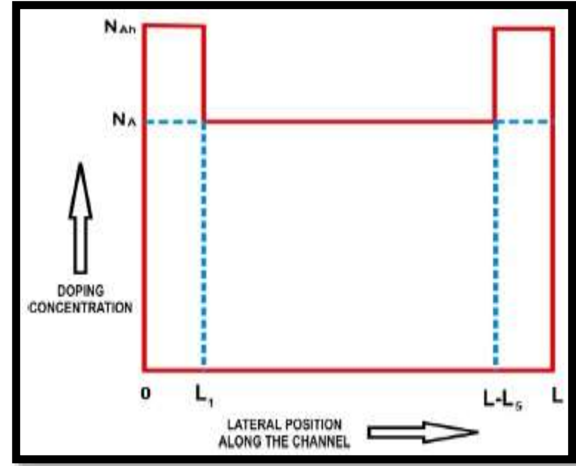

Fig. 3: Doping Concentration along the channel from Source to Drain region

3.3 Nano-DG-TFET I_D Model

The components of the lateral and vertical electric fields are used to compute the tunneling generation rate analytically. [10], was used to determine the tunneling generation rate.

$$G_{BTB} = A_{Kane}\frac{|E|^2}{\sqrt{E_g}} exp\left[\frac{-B_{Kane}E_g^{3/2}}{|E|}\right] \quad (44)$$

We can represent the electric field intensity (E) as:

$$|E| = \sqrt{E_{xi}^2 + E_{yi}^2};\ i = 1,2,3,4,5 \quad (45)$$

using average electric field (E), energy bandgap (Eg). The two parameters for tunneling: A_{Kane} = 4x10^{14} V$^{-5/2}$ S^{-1} cm$^{-1/2}$, B_{Kane}= 1.9x10^{7} V/cm are dependent on career effective mass in different energy bands.

$$I_{DS} = q\int G_{BTB}dv \quad (46)$$

Figure 3 shows the doping Concentration along the channel from source to drain region. It is presented as:

$$N(x) = \begin{cases} N_{Ah}; & 0 < x \le L_1 \\ N_A;\ L_1 < x \le (L - L_5) \\ N_{Ah;}\ (L - L_5) < x \le L \end{cases} \quad (47)$$

The average effective doping concentration can be stated as:

$$N_{avgeff} = N_A + \frac{2L_1(N_{Ah} - N_A)}{L} \quad (48)$$

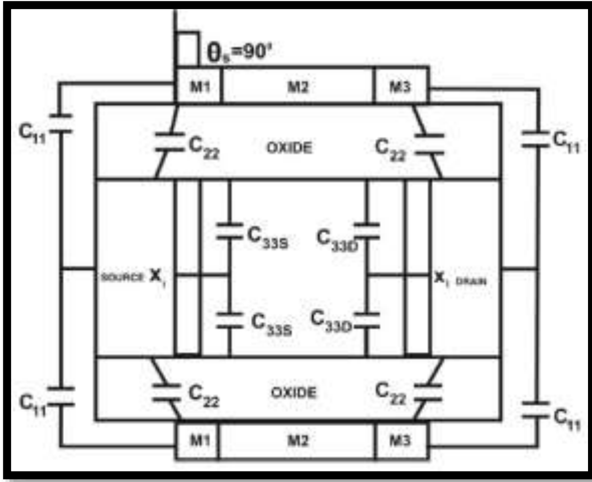

Fig. 4: Representation of the Fringing Capacitance Components C_{11}, C_{22} and C_{33}

The fringing potential has been investigated due to the internal fringing capacitance in order to improve channel potential efficiency. Figure 4 depicts the Fringing Capacitance Components C_{11}, C_{22} and C_{33}. C_{11} is the external fringing field capacitance between the S-C and the D-C electrode on all sides of the frontal and backward gates. The face-to-face overlap capacitance between the S-C junction and the D-C junction is represented by C_{22}. The internal fringing capacitance between the S-C junction and the D-C junction is represented by C_{33}. In Ref., the bias expressions based on C_{11}, C_{22}, and C_{33} are modelled. θ_S and C_{if} are the gate electrode slanting angle in radians, and maximum internal fringing capacitance value respectively. The following referred capacitances has been modeled as below:

$$C_{11} = W_c \frac{\epsilon_{SiO2}}{\theta_S} ln\left(1 + \frac{t_{gate}}{t_{ox}}\right) \quad (49)$$

$$C_{22} = W_c \frac{\epsilon_{SiO2}}{t_{ox}} \left[\frac{t_{effox}}{2}\left(\frac{1-cos\theta_S}{sin\theta_S} + \frac{1-cos\delta_S}{sin\delta_S}\right)\right] \quad (50)$$

$$C_{if} = W_c \frac{\epsilon_{SiO2}}{\delta} ln\left(1 + \frac{X_i sin\theta_S}{t_{ox}}\right) \quad (51)$$

In (49)-(51), we use the following: gate electrode thickness (t_{gate}), channel width (W_c), and source/drain junction depth (X_i), and $\delta = 0.5\Pi$ ($\mathcal{E}_{SiO2}/\mathcal{E}_{Si}$).

Due to internal fringing capacitance, at S-C and D-C the net total charge generated on each gate side is calculated as:

$$Q_{FD} = C_{if} \frac{V_{DS} - V_{DS,eff}}{1+e^{-\left(\frac{V_{GS}-V_{fb}}{30V_T}\right)}} = -C_{if} V_{FD} \quad (52)$$

$$Q_{FS} = -C_{if} \frac{V_{TH} - V_{fb} + 2\Psi_F + \gamma\sqrt{2\Psi_F - V_{GS}}}{1+e^{-\left(\frac{V_{GS}-V_{fb}}{30V_T}\right)}} = -C_{if} V_{FS} \text{ and } \gamma = \frac{\sqrt{2q\epsilon_{Si} N_{avgeff}}}{C_{ox}}$$

and $$\gamma = \frac{\sqrt{2q\epsilon_{Si} N_{avgeff}}}{C_{ox}} \quad (53)$$

where V_{fb} , Ψ_F , ni, γ, V_T are the flat-band voltage , Fermi potential, the intrinsic carrier concentration, Body effect Coefficient, and thermal voltage respectively.

The C_{OX}, $V_{DS,eff}$, V_{FS} and V_{FD} are oxide capacitance, the effective drain-to-source voltage, and fringing potentials at S-C and D-C ends respectively.

4 Results and Discussions

The TCAD simulation outcomes produced are analyzed along with the theoretical results of the V_{TH} and I_D in this section. The drift-diffusion model predicts *V-I* characteristics, while the high-field saturation model considers velocity saturation, the SRH recombination model accounts for recombination effects, the mobility model predicts mobility effects and the Slotboom model accounts for energy bandgap narrowing effects. Table 1 lists the TCAD device simulation parameters.

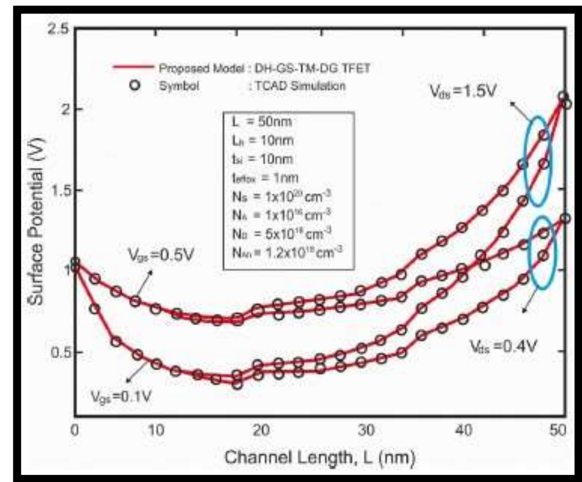

Fig. 5: Variation in surface potential w.r.t channel length (L) of proposed Nano-DG-TFET for V_{GS} = 0.1V, 0.5V, V_{DS} = 0.4V, 1.5V

The channel thickness, t_{si} has been assumed to be 10 nm in this investigation. For t_{si} greater than 5 nm, Quantum Mechanical Effects (QMEs) become unnoticeable. As a result, the suggested model avoids QME. Figure 5 shows the change in surface

potential along the channel length (L). It is self-evident that as V_{GS} rises, the channel potential rises as well. As a result, the S-C potential barrier diminishes, increasing the I_D as more carriers enter the channel from the source. Furthermore, because the S-C potential barrier is reduced as the strain in the channel grows, the I_D increases.

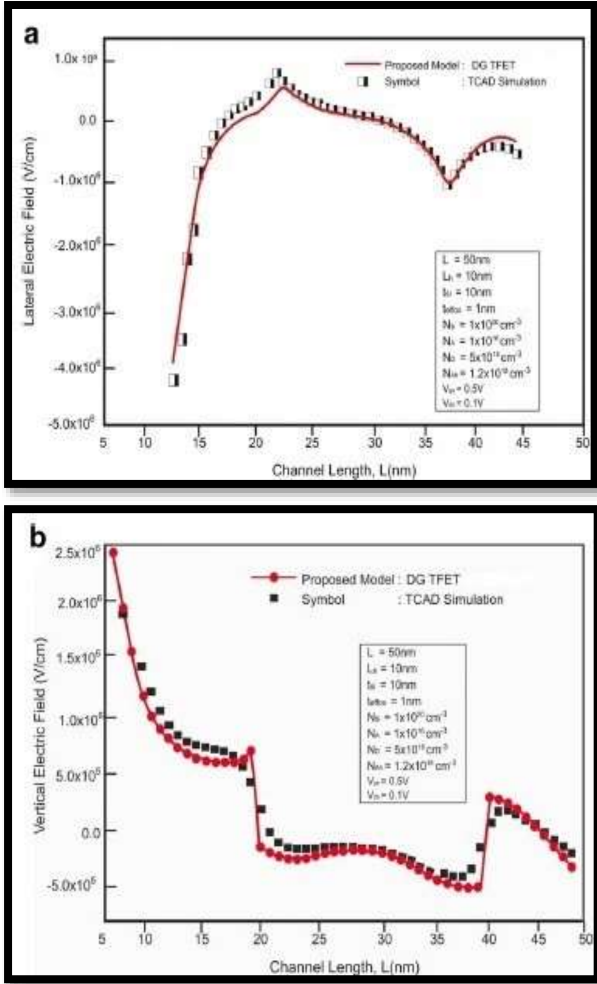

Fig. 6 (a) and (b): Lateral Electrical Field distribution (E_x) and Vertical Electric Field distribution (E_y) in the proposed Nano-DG-TFET channel for V_{GS} = 0.1V and V_{DG} = 0.5V

Figures 6 (a) and (b) show the differences in lateral and vertical electric fields (E_x and E_y) on the channel near the silicon body and the oxide interface surrounding the S-C region to D-C region respectively. Because of the voltage difference between the D-C and S-C region, the lateral electric field is created. The pinnacle electric decrement is rather minimal in the D-C region.

With V_{GS} = 0.1V, V_{DS} = 0.5V, for lateral position along the channel, the alteration in the electric field for proposed Nano-DG-TFET, SMDG-TFET, and TMDG-TFET is shown in Figure 7.

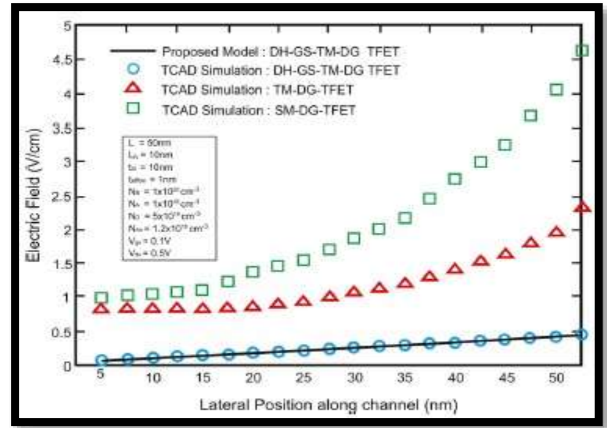

Fig. 7: With V_{GS} = 0.1V, V_{DS} = 0.5V, for lateral position along the channel, the alteration in the electric field for proposed Nano-DG-TFET, SMDG-TFET, TMDG-TFET

Because of the position movement of the minimum channel potential towards the drain side, the increase in the gate length ratio of control/screen improves drain control over the channel. However, as the gate length ratio of control/screen increases, the S-C built-in potential increases (larger V_{TH}), reducing leakage current. Taking the spatial derivative of the channel potential yielded the electric field. The electric field vertex at the drain side of the proposed Nano-DG-TFET structure is (0.220 V/cm), which is 19.47 times reduced w.r.t (3.265 V/cm) SMDG-TFET structure and 9.52 times reduced w.r.t TMDG-TFET structure (1.98 V/cm). As a result, the G&C engineering in our proposed device reduces the SCE and HCE.

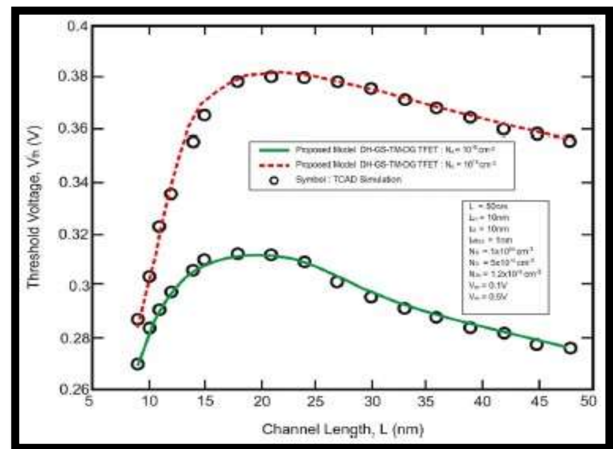

Fig. 8: Variation in V_{TH} with respect to L for distinct substrate doping concentrations. (N_{Ah}=1.2x10^{18}cm^{-3}, N_A=1x10^{16}cm^{-3} and 1x10^{18}cm^{-3} with V_{GS} = 0.1V and V_{DS} = 0.5V)

Figure 8 depicts the variation in V_{TH} with respect to L for distinct substrate doping concentrations,

(N_{Ah}=1.2x10^{18}cm^{-3}, N_A=1x10^{16}cm^{-3} and 1x10^{18}cm^{-3} with V_{GS} = 0.1V and V_{DS} = 0.5V). The S-C built-in potential is evidently enhanced by lowering the t_{ox} and silicon thickness, allowing the gate to exert greater influence over the channel than the drain, lowering the SCEs.

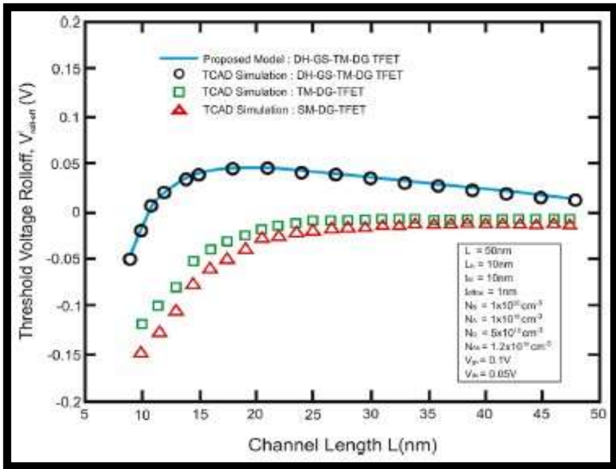

Fig. 9: V_{TH} roll-off vs. L, comparison plot for the proposed Nano-DG-TFET, SMDG-TFET, TMDG-TFET with V_{GS} = 0.1V, V_{DS} = 0.05V

Figure 9 shows the V_{TH} roll-off for the considered TFET devices for comparison. For L below 10 nm, the roll-off for the Nano-DG-TFET structure is lower than SMDG-TFET and TMDG-TFET structures. Hence this SCE is lowest for the proposed Nano-DG-TFET. Figure 10 shows the V_{TH} roll-off divergence for two drain biases for the proposed device. The graph shows that a larger drain bias causes a greater SCE and a higher V_{TH} roll-off value.

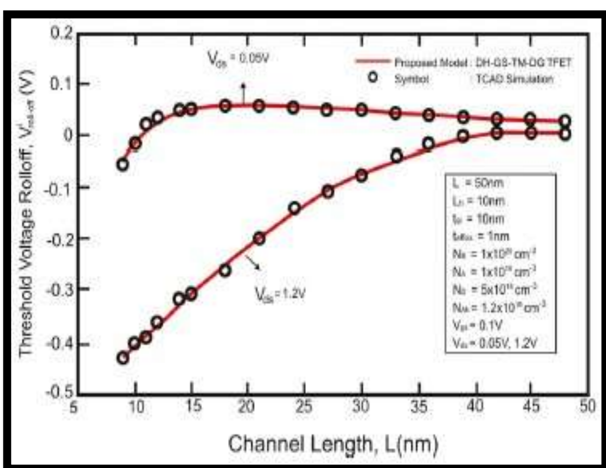

Fig. 10: V_{TH} roll-off vs. L of the proposed Nano-DG-TFET for V_{DS} = 0.05V and 1.2 V

For various thicknesses of gate stacked dielectric materials, Figure 11 depicts the variation of V_{TH} with t_{OX}. The site of the minimum channel potential is shown to vary with fixed charges and halo length.

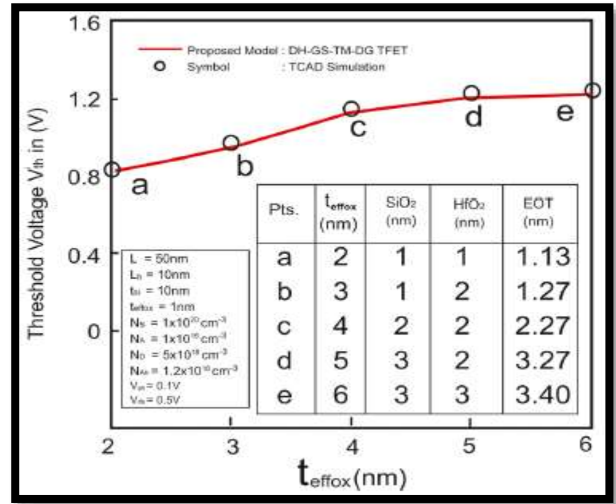

Fig. 11: Model variation off V_{TH} *vs.* t_{ox} of proposed Nano-DG-TFET

The DIBL effect of the proposed Nano-DG-TFET is smaller than the other compared TFET device structures, as shown in Figure 12. The plot reveals that the DIBL grows slightly as the t_{OX} increases. At 50 nm technology node, when the t_{OX} is augmented by the phase of 0.5 nm, the DIBL increases by around 50 mV/V. The simulation outcomes and the proposed model accord nicely.

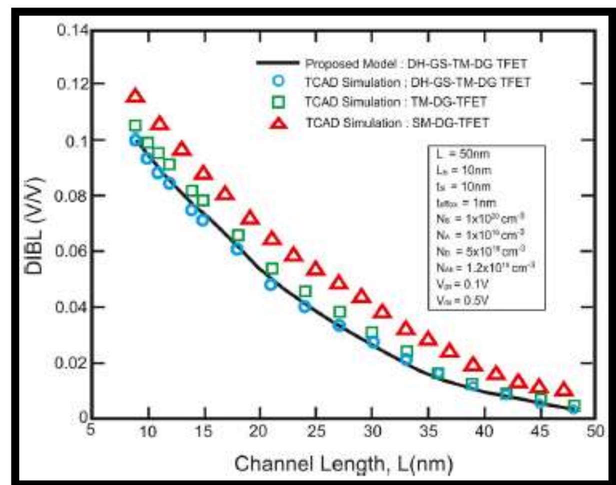

Fig. 12: Comparison plot of DIBL vs. L for the proposed Nano-DG-TFET, SMDG-TFET, TMDG-TFET, (V_{GS} = 0.1V, V_{DS} = 0.5V)

Figure 13(a) shows the Voltage Transfer Characteristics (VTC) of the proposed Nano-DG-TFET with a fixed thickness of 3 nm. The rise in I_D is caused by the increase in high-K HfO_2 thickness,

as shown in the graph. The variations of the V_{DS} vs. I_D for different V_{GS} are shown in Figure 13 (b). We can observe that the upsurge in I_D with V_{GS} is due to the decrease in the S-C barrier distance.

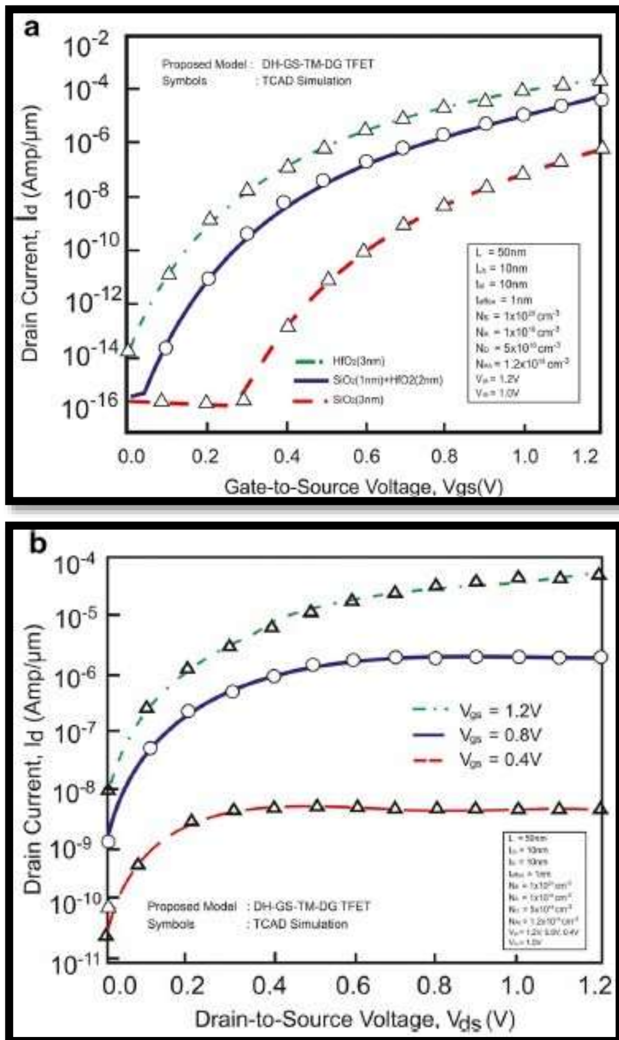

Fig. 13: (a) VTC of the proposed Nano-DG-TFET for different dielectrics at V_{DS} = 1V. (b) Output characteristics of the proposed device for different gate bias values

Figure 14 shows the calibration of the proposed Nano-DG-TFET, VTC comparison of Experimental results vs. TCAD simulation.

The ambipolar characteristic of the proposed Nano-DG-TFET is analyzed along with the other compared TFET device structures in Figure 15. The plot represents the device characteristics, and how effective the device is at restraining ambipolarity. In comparison to SM and TM equivalent structures, the device considered displays increased I_{ON} and minimal ambipolar conduction by choosing the correct materials for S-C gate sides and D-C gate sides. The accuracy of our I_D model is confirmed by the excellent match of our formulated model with TCAD outcomes.

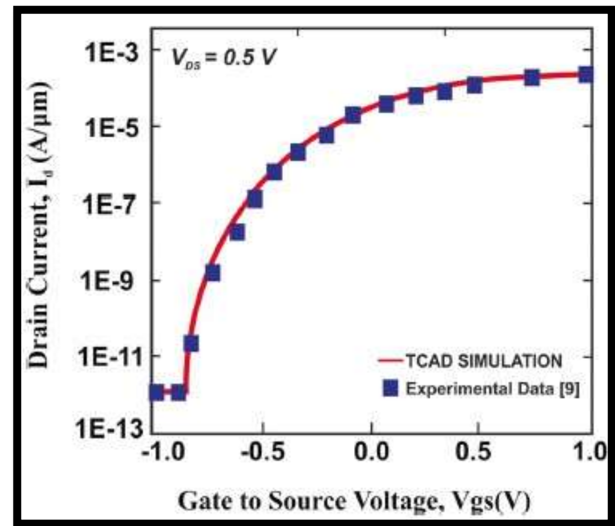

Fig. 14: VTC comparison of Experimental results vs. TCAD simulation

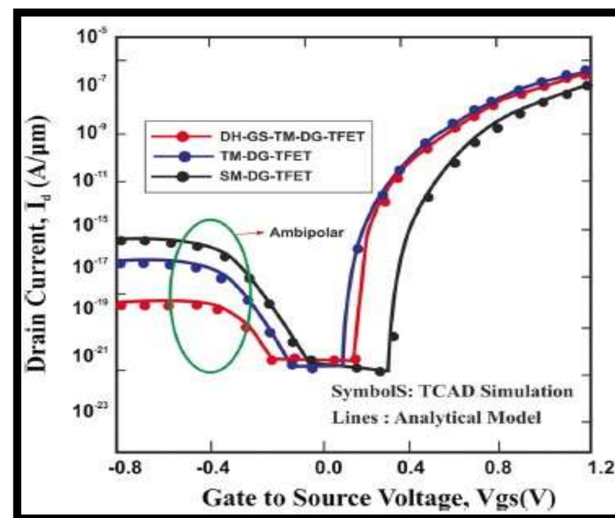

Fig. 15: Ambipolar characteristics comparison for the proposed Nano-DG-TFET, SMDG-TFET, TMDG-TFET, (V_{DS} = 0.5V)

5 Conclusion

Analytically, we derived and analyzed the properties of an efficient Nano strained-silicon dual-halo high-K dielectric stacked multi-material dual-gate TFET device (Nano-DG-TFET). Compact precise models for this proposed Nano-DG-TFET are mathematically formulated for the electric field, surface potential, drain current and Threshold Voltage. Using G&C engineering, the models are formulated by solving the 2-D Poisson equation in the s-Si graded channel region applying suitable boundary conditions. The t_{OX} is used in the

formulation of the V_{TH} model. The impacts of numerous device settings on DIBL and I_D have been thoroughly investigated. Up surging the strain and positive surface charge density, an increase in the electric field current and roll-off have been seen, and vice versa. Furthermore, combining the dual-halo technology with G&C engineering in TMDG-TFETs increases the I_D and ambipolar properties. By matching TCAD outcomes, the suggested model has been validated. The suggested device model and simulated findings demonstrate that the leakage current is reduced by itself to the range of 10^{-16}A/µm to 10^{-14}A/µm. Hence, the I_{ON} is improved (10^{-6}A/µm). The formulated mathematical model and simulation data are in good agreement. The effective surface charge and fringing capacitance are taken into account for accurate simulation. It has been established that the proposed Nano-DG-TFET is the confirmed upcoming device of ultra-low power VLSI and high-frequency applications.

References:

[1] Vimala, P., TS Arun Samuel, D. Nirmal, and Ajit Kumar Panda. "Performance enhancement of triple material double gate TFET with heterojunction and heterodielectric." *Solid State Electronics Letters*, 1, no. 2 (2019): 64-72.

[2] David Cavalheiro, Francesc Moll, StanimirValtchev. TFET-Based Power Management Circuit for RF Energy Harvesting. *IEEE Journal of the Electron Devices Society*, Jan. 2017;5(1):7–17.

[3] Santhosh Kumar Gupta, Satyaveer Kumar, Analytical Modeling of a Triple Material Double Gate TFET with Hetero–Dielectric Gate stack, *Silicon, Springer Nature*; July 2018.

[4] Swami, Yashu, and Sanjeev Rai. "Comprehending and Analyzing the Quasi-Ballistic Transport in Ultra Slim Nano-MOSFET through Conventional Scattering Model", *Journal of Nanoelectronics and Optoelectronics,* 14, no. 1 (2019): 80-91.

[5] Venkatesh, M., and N. B. Balamurugan. "Influence of threshold voltage performance analysis on dual halo gate stacked triple material dual gate TFET for ultra-low power applications", *Silicon,* 13, no. 1 (2021): 275-287.

[6] SwetaChander, Baishya S (2015) A Two-dimensional Gate Threshold Voltage Model, for a HeteroJunction SOI-Tunnel FET with Oxide/Source Overlap. *IEEE Electron Device Letters,* Vol. 36, Issue: 7, July 2015.

[7] Semiconductor Industry Association. "Emerging Research Devices", Chapter of "International Technology Roadmap for Semiconductors 2.0", 2015 Edition annual report, published Jun. 05, 2015, [Online], https://www.semiconductors.org/wp-content/uploads/2018/06/6_2015-ITRS-2.0-Beyond-CMOS.pdf (Accessed Date February 27, 2024).

[8] Sarkar A, De S, Sarkar CK (2013) Asymmetric halo and single halo dual-material gate and double halo double material gate n-MOSFETs characteristic parameter modeling. *Int J. Numer Model,* 26:41–55.

[9] Razavi P, Orouji AA (2008) Nanoscale triple material double gate (TM-DG) MOSFET for improving short channel effects. I*nternational Conference on Advances in Electronics and Microelectronics*, pp 11–14.

[10] Kane EO (1961) Theory of tunneling. *J. Appl Phys.,* 32(1):83–91.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

Yashu Swami performed the Parameter Modeling process and Analysis for the performance augmentation of the proposed Nano-DG-TFET.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The authors have no conflicts of interest to declare.

Creative Commons Attribution License 4.0 (Attribution 4.0 International, CC BY 4.0)

This article is published under the terms of the Creative Commons Attribution License 4.0 https://creativecommons.org/licenses/by/4.0/deed.en_US

APPENDIX

Appendix 1

Appendix-1 lists the expanded expression of *Mi* and *Ni* for *i* =1,2,3,4,5.

$$M_1 = \frac{1}{2\sinh(\tau L)} V_{FD} + V_{bi} + V_{DS} + \frac{\beta_5}{\tau^2}\left(V_{bi} + V_{FS} + \frac{\beta_1}{\tau^2}\right)e^{-\tau L} + \left(\frac{\beta_1-\beta_2}{\tau^2}\right)cosh\{\tau(L_2+L_3+L_4+L_5)\} + \left(\frac{\beta_2-\beta_3}{\tau^2}\right)cosh\{\tau(L_3+L_4+L_5)\} + \left(\frac{\beta_3-\beta_4}{\tau^2}\right)cosh\{\tau(L_4+L_5)\} + \left(\frac{\beta_4-\beta_5}{\tau^2}\right)cosh\{\tau(L_5)\}$$

$$M_2 = M_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{-\tau L_1}$$

$$M_3 = M_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{-\tau L_1} - \left(\frac{\beta_2-\beta_3}{2\tau^2}\right)e^{-\tau(L_1+L_2)}$$

$$M_4 = M_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{-\tau L_1} - \left(\frac{\beta_2-\beta_3}{2\tau^2}\right)e^{-\tau(L_1+L_2)} - \left(\frac{\beta_3-\beta_4}{2\tau^2}\right)e^{-\tau(L_1+L_2+L_3)}$$

$$M_5 = M_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{-\tau L_1} - \left(\frac{\beta_2-\beta_3}{2\tau^2}\right)e^{-\tau(L_1+L_2)} - \left(\frac{\beta_3-\beta_4}{2\tau^2}\right)e^{-\tau(L_1+L_2+L_3)} - \left(\frac{\beta_4-\beta_5}{2\tau^2}\right)e^{-\tau(L_1+L_2+L_3++L_4)}$$

$$N_1 = V'_{bi} - M_1 + \frac{\beta_1}{\tau^2} + V_{FS}$$

$$N_2 = N_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{\tau L_1}$$

$$N_3 = N_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{\tau L_1} - \left(\frac{\beta_2-\beta_3}{2\tau^2}\right)e^{\tau(L_1+L_2)}$$

$$N_4 = N_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{\tau L_1} - \left(\frac{\beta_2-\beta_3}{2\tau^2}\right)e^{\tau(L_1+L_2)} - \left(\frac{\beta_3-\beta_4}{2\tau^2}\right)e^{\tau(L_1+L_2+L_3)}$$

$$N_5 = N_1 - \left(\frac{\beta_1-\beta_2}{2\tau^2}\right)e^{\tau L_1} - \left(\frac{\beta_2-\beta_3}{2\tau^2}\right)e^{\tau(L_1+L_2)} - \left(\frac{\beta_3-\beta_4}{2\tau^2}\right)e^{\tau(L_1+L_2+L_3)} - \left(\frac{\beta_4-\beta_5}{2\tau^2}\right)e^{\tau(L_1+L_2+L_3++L_4)}$$

Appendix 2

Appendix-2 lists the expanded expression of V_{THL} and K_1-K_8.

$$V_{thL} = \frac{qN_{avgeff}}{\epsilon_{si}\tau^2} + V_{fb2} + 2\Psi_F$$

$$K_1 = \frac{V_1(e^{-\tau L}-1)}{2\sinh(\tau L)} - \frac{V_6(e^{-\tau L}-1)}{\sinh(\tau L)} - V_6 - \frac{V'^{th}_{FD}(e^{-\tau L}-1)}{2\{\sinh(\tau L)\}^2} - \frac{V'^{th}_{FD}}{2\sinh(\tau L)}$$

$$K_2 = \left\{\frac{(e^{-\tau L}-1)}{2\sinh(\tau L)}\right\}^2$$

$$K_3 = V_1V_6 - V_6{}^2$$

$$K_4 = \frac{2V_1V^{th}_{FD}}{\sinh(\tau L)} + 4\left[\left\{\frac{V^{th}_{FD}}{2\sinh(\tau L)}\right\}^2 + \frac{V_6V^{th}_{FD}}{\sinh(\tau L)}\right]$$

$$K_5 = V_{fb1} + 2\Psi_F + \gamma\sqrt{2\Psi_F}$$

$$K_6 = \frac{2V^{th}_{FD}e^{-\tau L}}{\{\sinh(\tau L)\}^2} - \frac{4V_6e^{-\tau L}}{\sinh(\tau L)} - \frac{2V_1e^{-\tau L}}{\sinh(\tau L)}$$

$$K_7 = \left\{\frac{e^{-\tau L}}{\sinh(\tau L)}\right\}^2$$

$$K_8 = \frac{2e^{-\tau L}(e^{-\tau L}-1)}{\{\sinh(\tau L)\}^2} + \frac{2e^{-\tau L}}{\sinh(\tau L)}$$

$$V_i = V_{bi} + \frac{qN_{avgeff}}{\epsilon_{si}\tau^2} + V_{fbi}; i = 1,2,3,4,5$$

$$V_6 = \frac{1}{\sinh(\tau L)}\big[V_{DS} + V_5 - V_1e^{-\tau L} + (V_1-V_2)cosh\{\tau(L_2+L_3+L_4+L_5)\} + (V_2-V_3)cosh\{\tau(L_3+L_4+L_5)\} + (V_3-V_4)cosh\{\tau(L_4+L_5)\} + (V_4-V_5)cosh(\tau L_5)\big]$$