# Design of Low Power Ternary Logic Encoder and ADC using CNTFET

VEENA M. B.[1], NIKITHA M.[2]
Department of Electronics and Communication Engineering,
BMS College of Engineering,
Bengaluru,
INDIA

*Abstract:* - Ternary logic has received substantial attention over the past decade due to its compensations of smaller chip area and interconnection compared to outmoded binary logic. Carbon Nanotube Field Effect Transistor (CNTFET) technology is widely used for ternary logic implementation due to its versatile threshold voltages. The increased power consumption in current designs utilizing CNFETs, as linked to binary logic, is attributed to elevated static power dissipation within the design. This work recommends alternative triple encoder designs with a focus on reducing the consumption of power. The model uses an additional $V_{dd}/2$ supply voltage to decrease static power dissipation and encoder power delay. Cadence virtuoso-based circuit simulations are implemented for the proposed encoder design.

*Key-Words:* - CNTFET, Cadence Virtuoso, ternary logic, Encoder, power delay, power delay product, Field Effect Transistor.

Received: April 19, 2023. Revised: February 12, 2024. Accepted: March 13, 2023. Published: April 22, 2024.

## 1 Introduction

Moore's law, which dates to around 1970, gave rise to the brilliant idea of doubling the number of transistors on a single chip every 2 years or eighteen months. There nevertheless was a limitation if the size of the transistors continued to shrink and eventually reached the size of an atom, there would be no more scaling. However, this equation allowed for a rise in chip density, leading to the development of CMOS technology and its eventual popularity over more straightforward MOSFET technology.

Profound sub-micron technologies advance, and secondary effects in CMOS begin to manifest themselves, making it more challenging to manage these effects in CMOS. Low static power and high noise immunity are two of the CMOS device's most important characteristics. Only when CMOS devices switch between the on and off states are significant amounts of power drawn. As a result, CMOS technology produces the least amount of thermal energy of any other technology. [1], current advancements have been made in the study of nanoscale devices. Devices on the nanoscale work with sizes of 100 nm and smaller. At such scales, phenomena like single-electron effects and quantum confinement in electronics begin to materialize. Numerous devices operating at the nanoscale can substitute the present CMOS circuit.

These nano-electric devices comprise graphene FETs, spin transistors, single electron transistors, and nanowire or carbon nanotube transistors. [1], in normal CMOS technology, silicon, which is always used, is replaced by carbon nanotubes (CNTs) as the bulk channel material. These FETs offer enhanced electron mobility, increased current density, high transconductance, advanced sub-threshold slope, better threshold voltage, and robust overall arrangement control.

The late 1990s saw the discovery of carbon nanotubes (CNTs), which are carbon allotropes with a cylinder-like shape. Nanotubes exhibit a length-to-diameter ratio as high as 132,000,000:1. The type of bonds that the carbon nanotubes inherit is precisely what gives them their remarkable strength. The entire molecular bonding of nanotubes is made up of sp2-bonds, the same kind of bonds present in graphite. Compared to sp3 bonds, which are typically found in diamond and alkanes, these sp2 bonds are stronger. Nanotubes have the potential to be employed as interconnects in the future due to their properties such as enhanced thermal conductivity, superior mechanical, current carrying capacity, and thermal stability. [1], crucially, these CNTs are now employed in CNTFETs (carbon nanotube field-effect transistors), which substitute silicon for CNTs, the channel material in conventional CMOS technology. The channel material of CNTFETs is

either an array of carbon nanotubes or a single carbon nano-tube as shown in Figure 1.

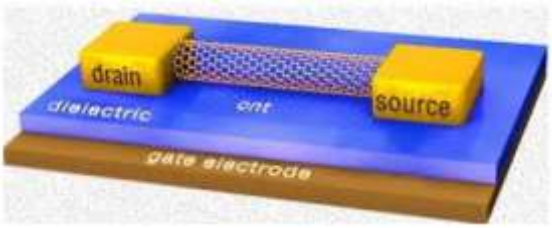


Fig. 1: Carbon nanotube serving as the channel material

## 2 Literature Survey

The paper, [2], provide a new CNTFET-based architecture for a two-bit Ternary Arithmetic Logic Unit (TALU). The proposed TALU design consists of a function select block, a transmission gate block, and functional modules. This design uses a 2:1 multiplexer design methodology to accomplish the functional modules. Compared to previous designs, this reduces the number of transistors by carrying away with the requirement for decoders at the input. In comparison to existing ones, the suggested Adder-subtractor and Multiplier modules use less power thanks to the suggested 2:1 multiplexer-based technique.

Circuits for a one-bit comparator based on CNTFET, [3], are explained and built using the Complementary CNTFET Technique (CCT) and Pass Transistor Logic (PTL) approaches in 32 nm technology. The development of the Power Delay Product (PDP) and Energy Delay Product for the CCT design one-bit comparator circuit are $8140\times10^{-24}$ and 8.1 $f_J$ respectively.

A contemporary ternary combinational digital circuit design, [4], that moderates energy consumption in low-power nano-scale embedded systems and Internet of Thing devices to conserve their battery consumption. The 32 nm CNTFET-based ternary half adder (THA) and ternary multiplier (TMUL) circuits use unique ternary unary operators and contrive two power supplies $V_{dd/2}$ and $V_{dd}$ scarce ternary decoders, basic logic gates, or encoders to minimize the number of transistors used and progress the wide energy efficiency.

This article, [5], introduces the predictable parameter of CNTFET. Where leakage current and power of the proposed D flip-flop had a better design compared with various other circuits. The D flip flop offers excellent effectiveness in leakage power consumption with an average of 10.306nW.

## 3 Methodology

The approach described here uses the decoderless method in tandem with a fast low-power encoder that was projected. Figure 2 illustrates the encoder's schematic. Table 1 exhibits the ternary logic with respect to voltage level values used in the schematic. To generate output 1, a direct path between $V_{dd}$ and *gnd* would still be utilized, [6]. A proposed encoder design aims to mitigate the power consumption associated with encoders in the decoderless approach.

Table 1. Voltages for the circuits

| Voltage Level | Logic Value |
|---|---|
| 0 | 0 |
| 1/2 $V_{dd}$ | 1 |
| $V_{dd}$ | 2 |

Table 2. Truth Table of ternary inverters

| x | STI(x) | NTI(x) | PTI(x) |
|---|---|---|---|
| 0 | 2 | 2 | 2 |
| 1 | 1 | 0 | 2 |
| 2 | 0 | 0 | 0 |

Table 3. Chirality and Threshold voltage of CNTFET's

| Chirality | Diameter of CNT(nm) | Threshold Voltage of N-CNTFET(V) | Threshold Voltage of P-CNTFET(V) |
|---|---|---|---|
| (19, 0) | 1.487 | 0.289 | −0.289 |
| (13, 0) | 1.018 | 0.428 | −0.428 |
| (10, 0) | 0.783 | 0.559 | −0.559 |

The proposed encoder circuit is presented in Figure 2. The inputs of an encoder can never be 1, hence they can be directly connected to the gate of the transistor in the $V_{dd/2}$ path without any NTI or PTI as depicted in Table 2, [7], this prevents the performance decline observed in the proposed STI because of its two stages, and the transition to output logic 1 is not on the critical path. When $F0$ =0 and $F1$ = 0, the transistors M1 and M2 are ON whereas the transistors M3 and M4 are OFF, achieving output $F$ = 2. When $F0$ = 2, transistors M3 and M2 are ON (1), but M1 is OFF (0), detaching $V_{dd}$ supply from the output and resulting in $F$ = 0. Similarly, for $F1$ = 2, transistor M4 will be ON (1) since $V_{GS} = V_{dd/2}$.

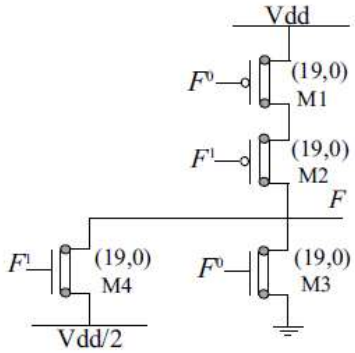


Fig. 2: Proposed Encoder

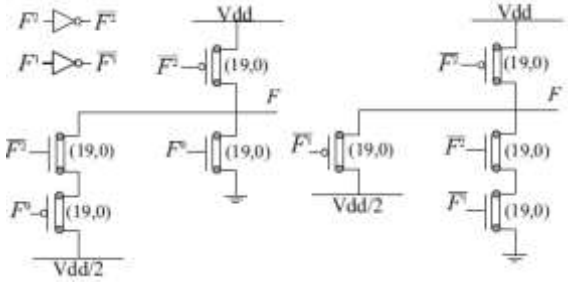


Fig . 3: Proposed Encoder for different inputs

The other operations of the encoder circuits are provided in Figure 3. These encoders can be amenably used with the decoderless approach given in, [9]. The inverted inputs can be generated either through a binary inverted executed with (19,0) CNFETs with threshold volage shown in Table 3, or directly by the decoderless approach. The following approach is suitable to minimize transistor count and Power Delay Product (PDP).

# 4 Results

The main difference between the NTI and PTI circuits is the chirality of the n-type and p-type. In NTI n-type is given as (19,0) and p-type as (10,0) chirality in PTI it is vice versa, [8]. The chirality is to be added by changing the properties of the CNTFET's circuit shown in Figure 4. The symbolic representation of NTI and PTI is in Figure 5

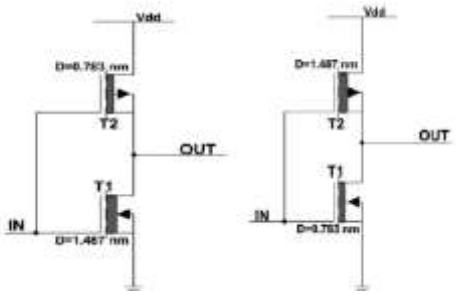


Fig. 4: PTI and NTI circuit diagram

Fig. 5: PTI and NTI Symbol

The standard ternary Inverter (STI) design consists of 3 PCNFET (PTI) and NCNFET (NTI). The diameter, and threshold as mentioned in Table 2 are added to PIT and NIT Field Effect Transistors shown in Figure 6. The power delay of the STI is measured in Cadence and is found to be 5.97e-17 J and the PDP of the STI is 2.07e-16 J as shown in Figure 7.

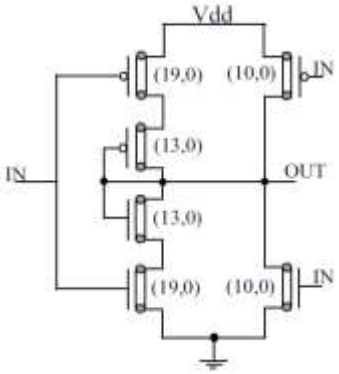


Fig. 6: STI Circuit diagram

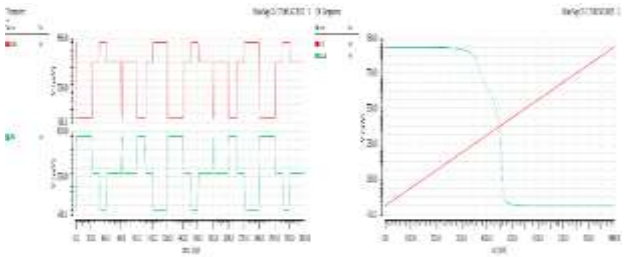

Fig. 7: DC and Transient analysis

## 4.1 1-D Multiplier using Encoder Design

Table 4. Truth Table A) Ternary Half Adder (THA) and B) Ternary Multiplier (TMUL)

a)

| | HS | | | HC | | |
|---|---|---|---|---|---|---|
| A/B | 0 | 1 | 2 | 0 | 1 | 2 |
| 0 | 0 | 1 | 2 | 0 | 0 | 0 |
| 1 | 1 | 2 | 0 | 0 | 0 | 1 |
| 2 | 2 | 0 | 1 | 0 | 1 | 1 |

b)

| | Prod | | | Carry | | |
|---|---|---|---|---|---|---|
| A/B | 0 | 1 | 2 | 0 | 1 | 2 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 2 | 0 | 0 | 0 |
| 2 | 0 | 2 | 1 | 0 | 0 | 1 |

To generate the product proposed one-bit TMUL employs the decoderless approach with the

proposed encoder, [9]. The carry can only be a maximum of 1, as seen in the truth table in Table 4. Here, the carry circuit has been implemented in Figure 8 with no *Vdd* supply. 1D multiplier carries transient analysis is depicted in Figure 9. As it reduces the number of transistors without increasing the propagation delay the following method is employed.

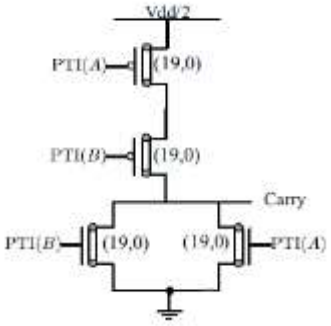


Fig. 8: 1D Multiplier carry

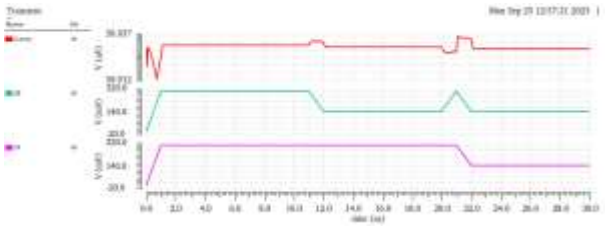

Fig. 9: Proposed 1D multiplier carries transient analysis.

The only case for *Carry* = 1 is for *A* = 2 and *B* = 2. This makes both *PTI*(*A*) =0 and *PTI*(*B*) = 0, turning both the PCNFETs, and making the output to *Vdd*/2. In all alternative input scenarios, at least one of PTI(A) or PTI(B) equals 2, activating one or both NCNFETs and leading to an output Carry of 0. Figure 10 illustrates a decoderless product circuit. To disrate the transistor count *P*2 and *P0* circuits are chosen, which in turn reduces power consumption and propagation delay. The transient response of P2 and P0 is depicted in Figure 11 and Figure 12 respectively.

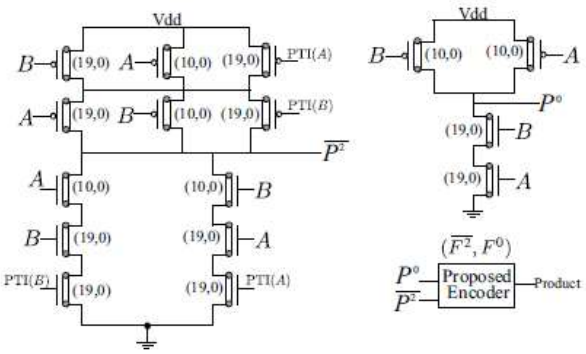


Fig. 10: Proposed 1D multiplier product circuit

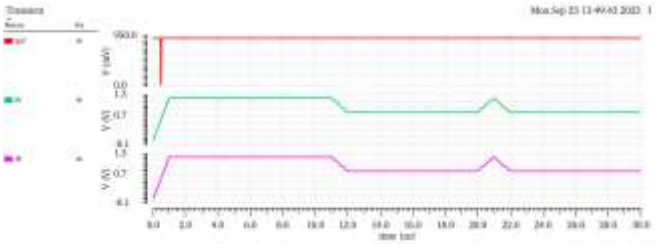

Fig. 11: Proposed 1D multiplier product P2' transient analysis

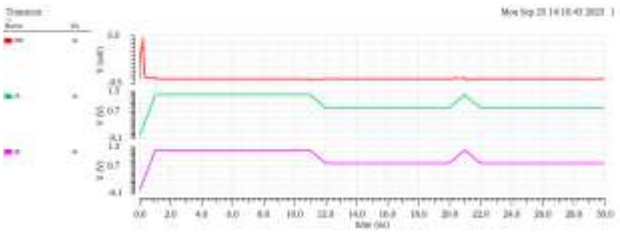

Fig. 12: Proposed 1D multiplier product P0 transient analysis

The use of the *P*1 circuit requires *NTI*(*A*), and *NTI*(*B*) inputs, which increases the transistor count by 4, also raising delay. The two NCNFET paths of the *P*2 circuit's Pull-Down Network (PDN) correspond to $A^2+B^1$ and $A^1+B^2$ unary operators. The Pull Up Network (PUN) is made for complimentary logic. The transient response of P1 Figure 13.

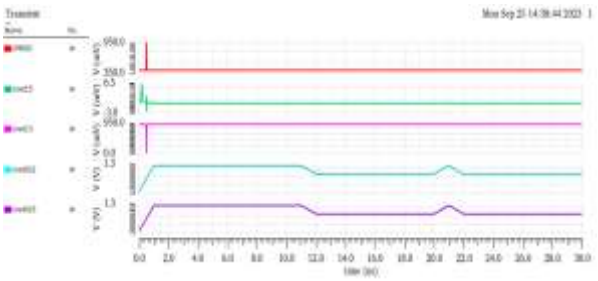

Fig. 13: Proposed 1D multiplier product P1 transient analysis

## 4.2 Ternary Half Adder (THA) using Encoder Design

Figure 14 represents the ternary half adder carry circuit incorporating the proposed encoder. The circuit has a CMOS representation of the carry equation with a chirality of (19,0) and (10,0) for PTI and NTI correspondingly. The transient analysis is displayed in Figure 15.

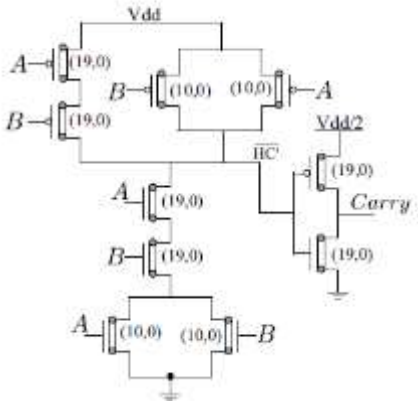


Fig. 14: Proposed THA carry circuit

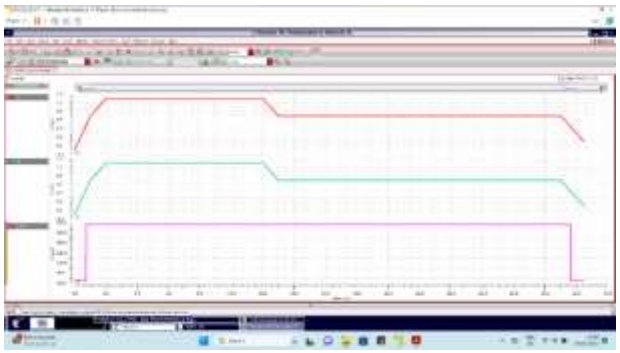

Fig. 15: Proposed THA carry transient response

The generated sum circuit is implemented with the decoders approach in Figure 16 and Figure 18 as seen in, [10]. Figure 17 exhibits transient response of Half adder *HS*0. In this logic, selecting any of the encoders leads to comparable circuits, resulting in the same levels of power consumption, delay, and number of transistors. The proposed (*F*0, *F*1) encoder has been used here defaulted.

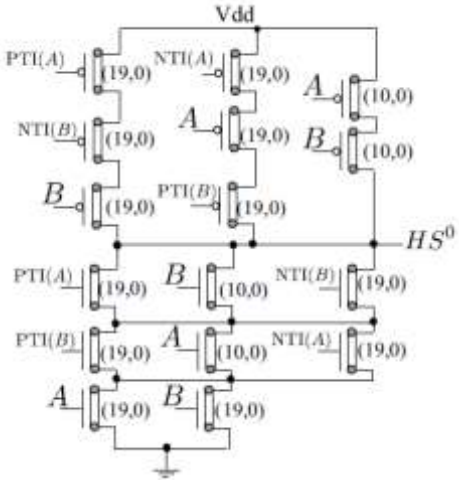


Fig. 16: Half adder *HS*0 circuit

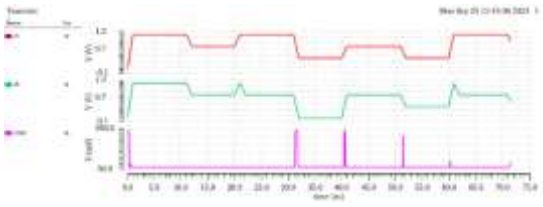

Fig. 17: Half adder *HS*0 Transient response

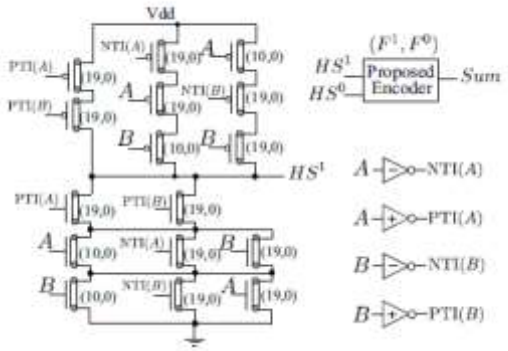


Fig. 18: Half adder *HS*1 circuit

### 4.3 Analog to Digital Converter (ADC)

Using ternary logic, a sine wave can be converted into digital. Each sine wave is effectively mapped into logic levels. The first sample has logic '2' high and all other levels low. For the 2nd sample, logic '2' is high, and '0' is low. The 3rd sample has all logic low levels. The 4th sample again has logic level '2' high, and all others low. In the 5th sample, all the logic levels are high. A sine wave can effectively be represented using ternary logic levels. The ADC uses only 3CNTFETs, which is relatively lesser compared to the traditional ADC technology.

By giving reference voltage the circuit can housed as a comparator. This proposed design consists of multiple threshold CNTFETs and can be enhanced or modified according to the specific requirements as depicted in Figure 19. When the input level reaches 0.8V, both N1 and N2 will be ON (1), and T1 will be OFF (0) until the next detection range. This approach can effectively detect a sine wave and encode it into 5 samples pointed in Figure 20.

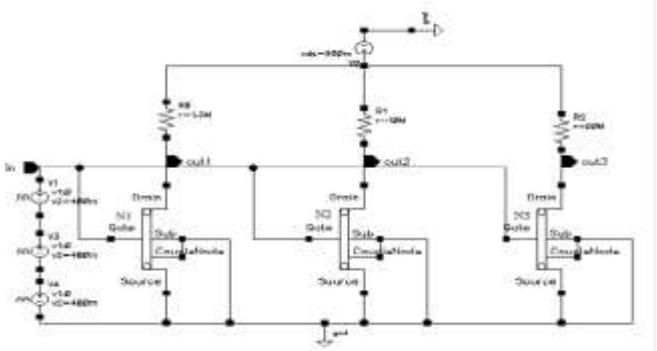

Fig. 19: ADC Level Detector design

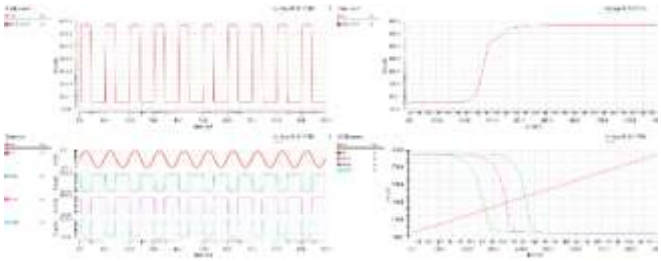

Fig. 20: ADC Level Detector Transient, DC Response, and Power Analysis

# 5 Conclusion

A novel design for the STI, Ternary Encoder, and Ternary ADC has been executed. The design incorporates an additional *Vdd*/2 supply for generating output logic 1, and disconnecting the close path between *Vdd* and g*nd*. The threshold voltage can be adjusted easily by altering its diameter, offering advantages over normal CMOS technology. The simulation is attained using Cadence Virtuoso and the obtained outcomes are illustrated in Table 5.

Table 5. THA, TMUL, and ADC Simulation Results

| | Design Approach | Power Consumption(µW) | Propagation Delay(ps) |
|---|---|---|---|
| **THA** | Decoderless | 0.105 | 42 |
| **TMUL** | Decoderless | 0.045 | 22.83 |
| **ADC** | Out1 | 0.052 | 23.25 |
| | Out2 | 0.055 | 23.5 |
| | Out3 | 0.057 | 23.75 |

*Acknowledgement:*
The authors would like to acknowledge the Ministry of Electronics and Information Technology (MEITY) for the support under “Chips to Startup (C2S) Programmer.

*References:*

[1] Bajaj, Karishma & Gambhir, Shilpa & Singh, Shashank. "*CMOS Technology Vs Carbon Nano Scale FET's*", *International Journal of Computer Science Engineering (IJCSE)*,2016.

[2] S. Gadgil and C. Vudadha, "Design of CNTFET-Based Ternary ALU Using 2:1 Multiplexer Based Approach," in *IEEE Transactions on Nanotechnology*, vol. 19, pp. 661-671, 2020, doi: 10.1109/TNANO.2020.3018867.

[3] R. Rajora, K. Sharma and A. Sharma, "CNTFET-based 1-bit Comparator Design using Low-power Logic Circuit Techniques," *2023 International Conference on Sustainable Computing and Data Communication Systems (ICSCDS)*, Erode, India, 2023, pp. 1028-1031, doi: 10.1109/ICSCDS56580.2023.10104888.

[4] J. M. Aljaam, R. A. Jaber and S. A. Al-Maadeed, "Novel Ternary Adder and Multiplier Designs Without Using Decoders or Encoders," in *IEEE Access*, vol. 9, pp. 56726-56735, 2021, doi: 10.1109/ACCESS.2021.3072567.

[5] J. H. Ridoy, A. Y. Rahman and F. R. Saquib, "Improved Design and Comparison of a Low Power CNTFET based on D Flip-Flop," *2023 International Conference on Electrical, Computer and Communication Engineering (ECCE)*, Chittagong, Bangladesh, 2023, pp. 1-5, doi: 10.1109/ECCE57851.2023.10101615.

[6] R. A. Jaber, B. Owaidat, A. Kassem and A. M. Haidar, "A Novel Low-Energy CNTFET-Based Ternary Half-Adder Design using Unary Operators," *2020 International Conference on Innovation and Intelligence for Informatics, Computing and Technologies (3ICT)*, Sakheer, Bahrain, 2020, pp. 1-6, doi: 10.1109/3ICT51146.2020.9311953.

[7] Chetan Vudadha and M. B. Srinivas, “Design of ternary logic circuits using cnfets,” in Nanoscale Devices: Physics, Modeling, and Their Application by Kaushik, B. Boca Raton. CRC Press, 2018.

[8] K. S. Saketh and P. R. Monica, "Ternary logic implementation and its applications using CNTFET," *2013 International Conference on Advanced Electronic Systems (ICAES)*, Pilani, India, 2013, pp. 304-306, doi: 10.1109/ICAES.2013.6659414.

[9] H. Sirugudi, S. Gadgil and C. Vudadha, "A Novel Low Power Ternary Multiplier Design using CNFETs," *2020 33rd International Conference on VLSI Design and 2020 19th International Conference on Embedded Systems (VLSID)*, Bangalore, India, 2020, pp. 25-30, doi: 10.1109/VLSID49098.2020.00022

[10] Saini, Jitendra & Srinivasulu, Prof. Avireni & Kumawat, Renu, “A Low Power - High-Speed CNTFETs Based Full Adder Cell With Overflow Detection*”. Micro and Nanosystems,* 2019*,* 11. 10.2174/1876402911666190211154634.

**Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)**

Both Veena M. B. formulated the idea, and carried out a literature survey, while Nikitha M. provided the method, carried out simulations, and analysis of the results, and wrote the paper. All authors have read and approved the manuscript.

**Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself**

Authors declare no funding for this research.

**Conflict of Interest**

The authors have no conflicts of interest to declare.