Design and Comparison of Constant Transconductance Architectures

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Abstract: - Constant transconductance (G_m) biasing circuits, as the name suggests, generate a bias current that ensures that the G_m of a MOS transistor remains constant. The G_m of a MOS transistor is a very important parameter as various other parameters of a circuit such as the gain, UGB (Unity Gain Bandwidth, poles, and zeros are strongly dependent upon it. Every analog circuit in a chip is subjected to varying PVT (Process, Voltage, and Temperature) conditions. This leads to a varying G_m of the devices, and hence the parameters such as the gain and UGB also tend to vary. Hence, constant G_m biasing is crucial in systems, where the parameters are expected to be constant regardless of the external factors. The majority of constant G_m biasing circuits make use of an external off-chip resistor. While this is a reasonable solution, it adds to the cost, area, and complexity of the solution. Hence, it is vital to model and design all the required functionalities within the chip, eliminating the requirement for any external components. In this paper, different architectures of constant G_m biasing circuits are designed and simulated in Cadence Virtuoso software. The proposed architecture has an error of 6.42% in the variation of transconductance, which is a significant improvement concerning the other architectures simulated. Additionally, the proposed architecture does not require any off-chip components while the other architectures require an off-chip resistor. Hence, the proposed solution has reduced cost and complexity.

Key-Words: - Constant G_m, off-chip resistor, Gain, UGB, Biasing, Common Mode Feedback.

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1 Introduction

Constant transconductance biasing circuit, or CTB circuit, is an important technique used in electronic circuits to maintain a consistent transconductance (G_m) for active devices like transistors. The transconductance of a device represents its ability to convert changes in input voltage into corresponding changes in output current. By ensuring a constant transconductance, CTB circuits help to achieve stable and predictable performance of active devices across various operating conditions, including temperature fluctuations, process variations, and power supply changes.

The necessity of constant transconductance biasing arises due to several factors. Firstly, temperature variations can significantly impact the behavior of transistors. By implementing CTB circuits, the impact of temperature changes can be compensated, ensuring that the circuit operates consistently over a wide temperature range. Secondly, process variations in integrated circuit manufacturing can lead to differences in transistor parameters. CTB circuits help to mitigate these process discrepancies thus enabling uniform performance across different manufacturing batches. Moreover, fluctuations in the power supply can affect the behavior of transistors and consequently the circuit's overall performance. Constant transconductance biasing reduces the dependency

on the power supply voltage, resulting in improved stability and power supply rejection.

The standard constant G_m bias architecture, described in, [1], employs a supply-independent configuration and a switched capacitor resistor. This ensures that the resistor remains unchanged regardless of process and temperature variations. A modified version of the constant G_m bias architecture is discussed in, [2], where the deviation is limited to 0.5% even with a temperature range of 120°C and a device mismatch of ±4%. Beta-multiplier circuits described in, [3] and [4], generate a G_m that tracks an off-chip conductance ($G_{off\ chip} = 1/R_{off\ chip}$) to maintain consistency with temperature changes and on-chip process variations. However, using an off-chip component increases the cost and the beta-multiplier topology relies on the assumption of square law behavior of MOS devices, which does not apply to modern sub-micron processes, [5].

An alternative approach for achieving a constant G_m without an off-chip resistor is presented in, [6] and, [7]. This temperature-compensated method generates current references that are proportional and constant, compensating for temperature-induced variations in the electron mobility of a MOSFET. Here the assumption of a square law model for the MOSFET's G_m is made. Another technique described in, [8] utilizes a small signal method to generate a fixed transconductance. By applying a small voltage ($I \times R_{off\ chip}$) to a differential pair and adjusting the bias current through negative feedback, the incremental differential drain current is set to I. This method also requires an off-chip resistor.

In, [9], the simulation of the standard constant G_m technique has been demonstrated, revealing the need for high current and reliance on the square law model of transistors. The technique used in, [9], is modified in, [10], in which the current consumption is reduced by sacrificing the circuit speed. Nevertheless, both the architectures are still bound by the square law model assumption. The theoretical understanding and limitations of the conventional constant G_m circuit are emphasized in, [11], where the effect of Channel Length Modulation (CLM) is identified as a crucial factor in maintaining a constant G_m.

In, [12], a unique method is introduced, which achieves constant transconductance by subtracting the output currents of two independent transconductance references. This approach minimizes second-order effects by taking the current difference, resulting in a PVT (Process-Voltage-Temperature) invariant transconductance. [13] and [14], presents a novel 9 nW PVT invariant subthreshold transconductance bias circuit that extracts a transistor's specific current and subjects it to a squaring circuit to provide an invariable transconductance bias over temperature in the subthreshold region.

Furthermore, [15], proposes a new PVT independent constant G_m bias technique applicable to any I_{out} monotonic convex transconductors. This, [16], method transforms the traditional approach of maintaining a constant transconductance bias into an analog computation procedure. It involves using an input current to calculate the desired constant transconductance bias voltage, denoted as V_0. The process is carried out by an analog computer that assesses the effective transconductance obtained from two identical transconductors and then modifies V_0 to align it with the inverse of precise resistance.

2 Design of Constant G_m Biasing Circuit Architectures

In this paper, four architectures are designed, and simulated and a comparative analysis of these architectures is performed. The architectures designed are: Standard beta multiplier circuit, beta multiplier circuit with cascade stage, beta multiplier circuit with Common Mode Feedback (CMFB), and the modified constant G_m circuit, which is also the proposed architecture.

2.1 Standard Beta Multiplier Circuit

The standard beta multiplier circuit, also known as the supply-independent biasing circuit, comprises of four transistors and an external resistor.

Figure 1 represents the standard beta multiplier circuit.

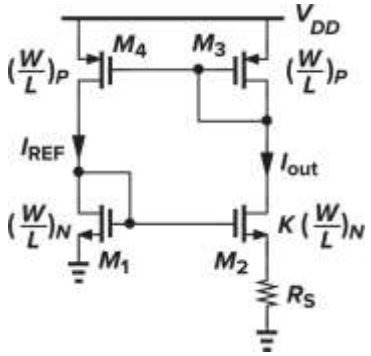

Fig. 1: Standard Beta Multiplier Circuit, [1]

where I_{REF} is the reference current that is to be mirrored, I_{OUT} is the output current or the mirrored current, and R_S is the external resistor that is added

as a constraint to uniquely define the currents. The external resistor R_S decreases the current of mosfet M_2 in 1 while the PMOS devices, M_3 and M_4 require that I_{REF} and I_{OUT} are the same as they have identical threshold voltages and dimensions.

$$V_{GS1} = V_{GS2} + I_{D2}R_S \quad (1)$$

$$\sqrt{\frac{2I_{OUT}}{\mu_n C_{ox}\left(\frac{W}{L}\right)N}} + V_{TH1} = \sqrt{\frac{2I_{OUT}}{\mu_n C_{ox}\left(\frac{W}{L}\right)N}} + V_{TH2} + I_{OUT}R_S \quad (2)$$

Equation 1 and Equation 2 are derived from the standard MOS transistor equations in the saturation region. Further, by neglecting the body effect, equation 2 becomes (3):

$$\sqrt{\frac{2I_{OUT}}{\mu_n C_{ox}\left(\frac{W}{L}\right)N}}\left(1 - \frac{1}{\sqrt{K}}\right) = I_{OUT}R_S \quad (3)$$

$$I_{OUT} = \frac{2}{\mu_n C_{ox}\left(\frac{W}{L}\right)N}\left(\frac{1}{R_S^2}\right)\left(1 - \frac{1}{\sqrt{K}}\right)^2 \quad (4)$$

Equation 4 shows that the current is independent of the supply voltage. Hence the name, supply independent biasing circuit. In the derivation, V_{TH1} is assumed to be equal to V_{TH2} which introduces some amount of error due to body effect as the source voltages of M_1 and M_2 are different. Also CLM is neglected, which will introduce a significant amount of error in lower technology nodes.

The transconductance of a MOSFET is related to the current as follows (5):

$$g_m = \sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)I_D} \quad (5)$$

Hence, the transconductance of M_1 is obtained as follows (6):

$$g_{m1} = \frac{2}{R_S}\left(1 - \frac{1}{\sqrt{K}}\right) \quad (6)$$

2.2 Beta Multiplier Circuit with Cascade Stage

Cascading is a commonly used configuration in amplifier design that offers several advantages over other amplifier topologies. It consists of two transistors connected in a series configuration: a common source transistor on the bottom and a common gate transistor on the top. The output of the common source stage is connected to the input of the common gate stage. The cascade configuration provides enhanced performance characteristics such as high gain, improved linearity, increased output impedance and better bandwidth.

The advantage of cascading exploited in this architecture is the reduced effect of CLM. As mentioned earlier, the derivation of transconductance in the standard beta multiplier circuit assumes that CLM is negligible and hence it is ignored. CLM is the phenomenon in which the current variation of a transistor in the saturation region is proportional to the variation in the drain-to-source voltage, which deviates from the behavior of a current source. In practical cases, the supply voltage varies from the desired value, and hence the drain-to-source voltage varies as well. This leads to an error in the transconductance of the circuit due to CLM.

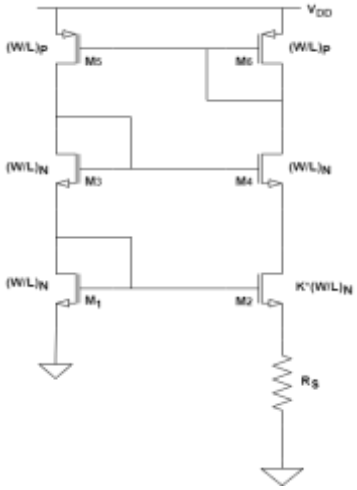

Fig. 2: Beta Multiplier Circuit with Cascade Stage

Figure 2 represents the beta multiplier circuit with a cascade stage. The transconductance is given by Equation 6. Transistors M_3 and M_4 represent the cascade stage which reduces the effect of CLM. The effect of CLM is reduced by the shielding property of the cascade device. The impedance seen from the drain of the cascade stage is very high and hence a variation in the voltage value at the drain translates to a lesser variation at the drain of the input stage (M_1 and M_2 in Figure 2).

2.3 Beta Multiplier Circuit with Common Mode Feedback

The third architecture utilizes CMFB biasing to reduce the effect of CLM significantly, which aids in obtaining a constant G_m. CMFB biasing is a technique used in analog circuit design to stabilize the operating point of differential amplifiers and to ensure proper operation in the presence of common-mode input signals. In differential amplifiers, it is important to maintain a balanced and stable biasing condition to achieve accurate amplification of differential signals while rejecting common-mode signals. CMFB biasing provides a feedback mechanism to monitor the common-mode voltage and adjust the biasing current accordingly.

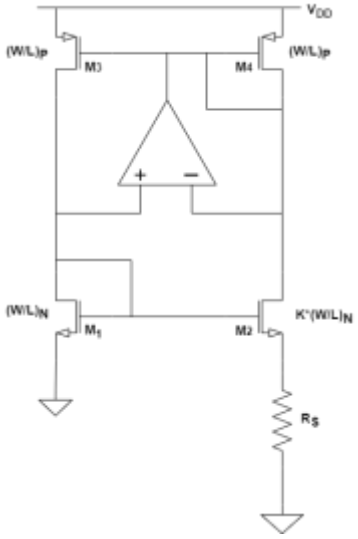

Fig. 3: Beta Multiplier Circuit with CMFB

The CMFB circuit typically consists of a differential amplifier that compares the common-mode voltage at the input with a reference voltage. The differential amplifier produces an error signal that is fed back to the biasing circuitry to control the biasing currents in the differential pair. By dynamically adjusting the biasing currents, the CMFB circuit keeps the common-mode voltage at the desired level, ensuring stable and linear operation of the amplifier.

Figure 3 represents the third architecture. The G_m is once again governed by Equation 6. The three architectures explained so far require an off-chip resistor, which adds to the cost, area, and complexity of the solution.

2.4 Modified Constant G_m Architecture

The fundamental concept of the idea involves creating an on-chip conductance using a MOSFET, operating in its linear region and utilizing it to track the G_m of the transconductance through a negative feedback loop. The success of this solution relies on effectively maintaining a constant conductance of the MOSFET regardless of changes in the operating conditions.

2.4.1 Principle of Operation

The basic idea for the generation of a constant G_m is represented in Figure 4.

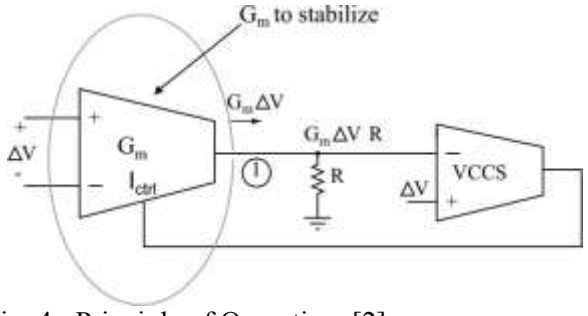

Fig. 4: Principle of Operation, [2]

A small voltage (ΔV) is applied to a transconductor to generate an incremental current (G_m ΔV). This current is then passed through a fixed resistance 'R'. The resistor R is a constant on-chip resistor that is modeled with the help of Op-Amp and a transistor in the deep linear region. The resulting incremental voltage (G_m ΔV R) is compared to the applied voltage (ΔV) and the transconductance value is adjusted through negative feedback by modifying its bias current. The adjustment continues until G_m ΔV R equals ΔV, thereby ensuring that G_m is equal to 1/R. The bias current generated in this process is mirrored in all the on-chip transconductors that require stabilization of their transconductances.

2.4.2 Generation of Constant On-Chip Resistance

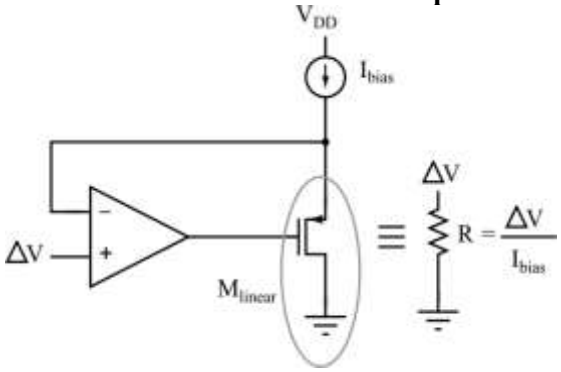

Fig. 5: On-chip resistor, [2]

The depicted on-chip resistance R, in Figure 5 is achieved by utilizing a PMOS transistor (M_{linear} in Figure 5) operating in the deep linear region. A precise current, $I_{SD} = I_{bias}$, is directed through this transistor, while a precise source-to-drain voltage, $V_{SD} = \Delta V$ is maintained through negative feedback. This feedback mechanism ensures that the resistance between the source and drain terminals of the PMOS transistor remains constant at $\Delta V/I_{bias}$, regardless of changes in the surrounding conditions. Importantly, the replicated version of this resistance can be implemented anywhere on the chip to establish a consistent on-chip resistance.

2.4.3 Circuit

Figure 6 represents the modified constant G_m circuit employed for stabilizing the transconductance of a fully differential transconductor. M_{R1} and M_{R2} function as the constant resistors whose gate voltages V_{g1} and V_{g2} are routed from the circuit as explained in Figure 5. These transistors are sized significantly larger to ensure that any random mismatches on the chip have a negligible effect on the conductance. M_1 and M_2 form the input pair of the transconductor where G_m needs to be fixed, while M_0 regulates the bias current through the pair. The cascade transistors M_5 and M_6, are employed to enhance the transconductor' s output resistance. Additionally, the PMOS loads M_3 and M_4 are sized in such a way that their output conductance is negligible in comparison to M_{R1} and M_{R2}.

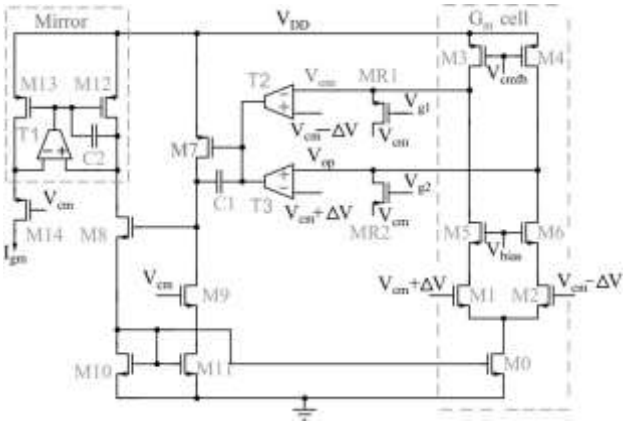

Fig. 6: Modified Constant G_m Circuit, [2]

A small differential DC voltage, 2ΔV is applied to the differential pair M_1-M_2, which operates around the common mode voltage V_{cm}. This results in an incremental current, $G_m\Delta V$ flowing through M_1-M_2 and into M_{R1}-M_{R2}. The incremental voltages, $G_m\ \Delta VR_{MR1}$ and $G_m\Delta VR_{MR2}$ appear at V_{om} and V_{op} respectively, where R_{MR1} and R_{MR2} represent the source-to-drain resistances of M_{R1} and M_{R2}. The circuit's behavior can be understood through negative feedback. If the G_m of M_1-M_2 is too high, V_{om} decreases and V_{op} increases. Consequently, transconductors T2 and T3 drive the gate of M_7 higher, reducing the current through M_{10}. This mirrored current flowing through M_0 into the differential pair corrects the increase in G_m of M_1-M_2. With high loop gain in the negative feedback, the difference between the differential inputs of T1 and T2 is forced to zero. This results in the incremental resistances being identical (that is, $R_{MR1} = R_{MR2} = \Delta V/I_{bias}$). Furthermore, since $G_{m|M1,M2}\Delta VR_{MR1}, R_{MR2} = \Delta V$, $G_{m\ |M1,M2}$ settles to $I_{bias}/\Delta V$.

The current biasing of the differential pair possesses all the necessary characteristics to ensure the insensitivity of $G_{m|M1,\ M2}$ to variations in ambient conditions. As a result, this current is replicated through a precise current mirror consisting of M_{12}-M_{13} and distributed to the transconductors throughout the remaining sections of the chip.

2.4.4 Telescopic Operational Amplifier

Transconductors T_1, T_2, and T_3 are replaced by telescopic amplifier configuration. The telescopic Op-Amp is a commonly used configuration in analog integrated circuit design. It is a variation of the classical two-stage Op-Amp architecture, featuring a combination of a common-source input stage and a common-gate output stage.

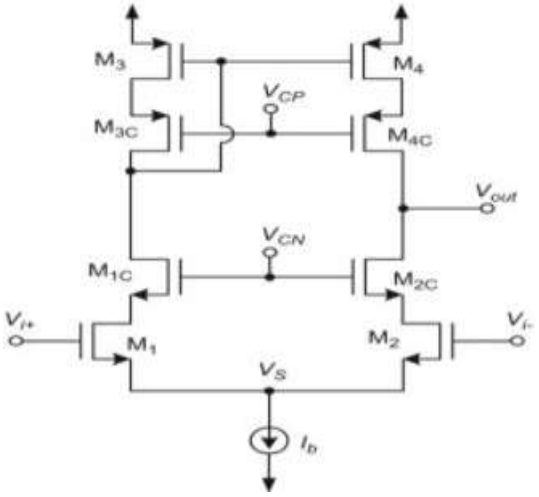

Fig. 7: Telescopic Op-amp Circuit

Figure 7 represents the telescopic Op-Amp circuit. Transistors M_1-M_2 represent the input pair, transistors M_{1C} -M_{2C} and M_{3C} -M_{4C} represent the cascade stages, and transistors M_3- M_4 represent the PMOS current source loads. The gain of the circuit is given by Equation 7.

$$A_V = -g_{M_1} * \left(g_{M_{2C}} r_{O_{2C}} r_{O_2} || g_{M_{4C}} r_{O_{4C}} r_{O_4}\right) \qquad (7)$$

3 Simulation Results

The architectures aforementioned are simulated using the Cadence Virtuoso software tool and the results obtained are analyzed in this section.

3.1 Standard Beta Multiplier Circuit

The G_m of 'M_2' in Figure 1 was swept with process corners and supply voltage (PV variation). Consequently, the G_m of 'M_2' was swept with temperature. The graphs obtained are shown in Figure 8 and Figure 9 respectively.

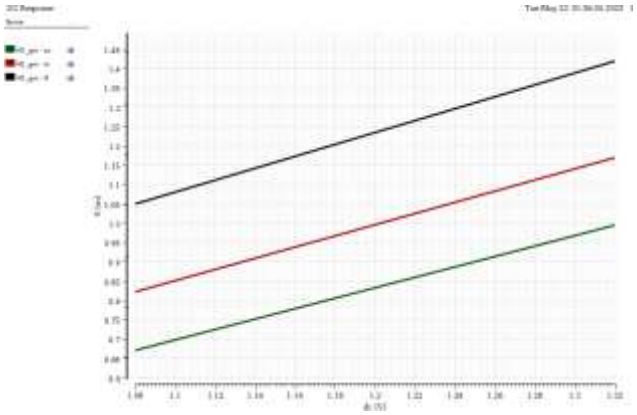

Fig. 8: G_m Variation with Process Corner and Supply Voltage

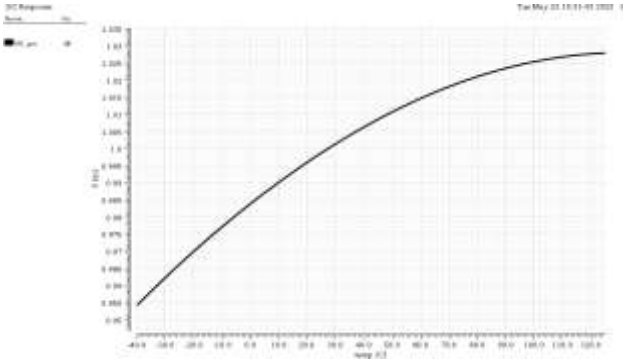

Fig. 9: G_m Variation with Temperature

The variation of G_m of 'NM1' with process corner and supply voltage is shown in Figure 8. As shown in Table 1, for supply voltage varying from 1.08V to 1.32V, the maximum and minimum values of G_m are 1.42mS and 0.671mS respectively, which translates to an error of 35.77% due to PV variations.

Table 1. G_m values at Different Process Corners

Process Corner	Minimum G_m Value (mS)	Maximum G_m Value (mS)
ss	0.67178	0.99544
tt	0.82327	1.17
ff	1.05	1.42

As observed in Figure 9, the value of G_m varies from 0.95418mS to 1.03mS for temperatures varying from -40°C to 125°C, which translates to an error of 3.8%.

3.2 Beta Multiplier Circuit with Cascade Stage

The G_m of 'M_2' in Figure 2 was swept with process corners and supply voltage (PV variation). Consequently, the G_m of 'M_2' was swept with temperature. The graphs obtained are shown in Figure 10 and Figure 11 respectively.

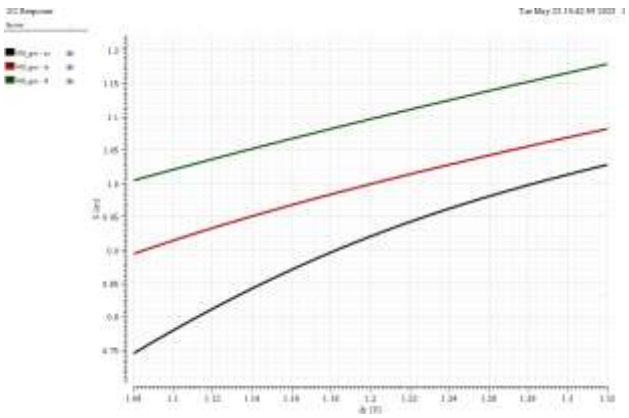

Fig. 10: G_m Variation with Process Corner and Supply Voltage

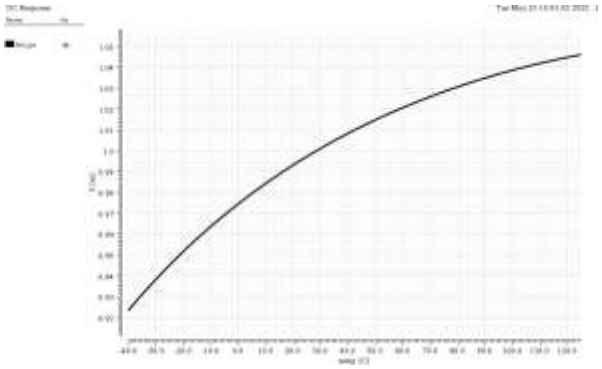

Fig. 11: Gm Variation with Temperature

As observed in Figure 10, the variation of G_m across process corners for a supply voltage varying from 1.08V to 1.32V is obtained and tabulated in Table 2. The maximum and minimum values of G_m are 1.18mS and 0.745mS respectively, which translates to an error of 22.55% due to PV variations. This is an improvement from the standard beta multiplier circuit which arises due to the mitigation of CLM effect by cascade shielding property.

Table 2. G_m values at Different Process Corners

Process Corner	Minimum G_m Value (mS)	Maximum G_m Value (mS)
ss	0.745	1.03
tt	0.89414	1.08
ff	1	1.18

As observed in Figure 11, the value of Gm varies from 0.923331mS to 1.05mS for temperatures varying from -40°C to 125°C, which translates to an error of 6.24%.

3.3 Beta Multiplier Circuit with Common Mode Feedback

The G_m of 'M_2' in Figure 3 was swept with process corners and supply voltage (PV variation). Consequently, the G_m of 'M_2' was swept with temperature. The graphs obtained are shown in Figure 12 and Figure 13 respectively. The Op-Amp is modelled by a VCVS, which is an ideal case of an Op-Amp.

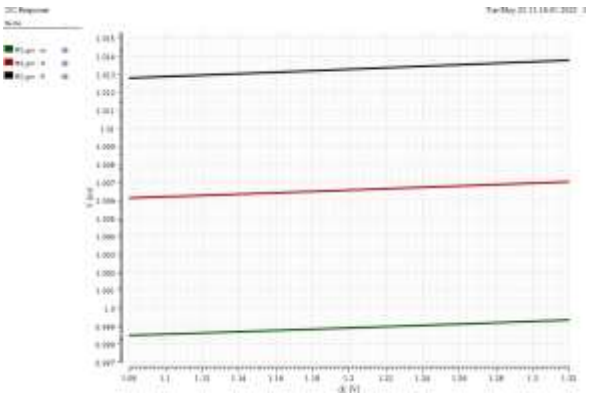

Fig. 12: Gm Variation with Process Corner and Supply Voltage

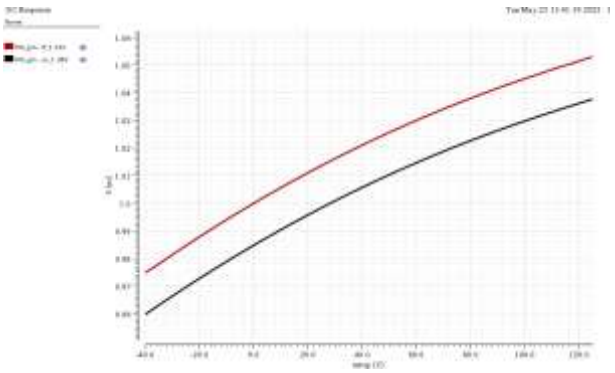

Fig. 13: Gm Variation with Temperature

As observed in Figure 12, the variation of G_m across process corners for a supply voltage varying from 1.08V to 1.32V is obtained and tabulated in Table 3. The maximum value of G_m is 1.053mS which occurs at 125°C in the ff corner. The minimum value of G_m is 0.95972mS which occurs at -40°C in the ss corner. Hence, the error obtained for PVT variation is 4.63%. This is an improvement from the previous architectures and is due to the property of CMFB, which stabilizes the voltages at the input of the CMFB Op-Amp. Monte Carlo simulation was performed for this architecture as the error due to PVT variations is less.

Table 3. G_m values at Different Process Corners

Process Corner	Minimum Gm Value (mS)	Maximum Gm Value (mS)
ss	0.99850	0.99935
tt	1.006	1.007
ff	1.012	1.137

As observed in Figure 14, the standard deviation is 0.0108mS while the mean value is 1.006mS. Hence, the error obtained is 3.24%. It is important to note that the Op-Amp used in this simulation is ideal. A non-ideal Op-Amp would contribute significantly to the mismatch variation and moderately to PVT variations.

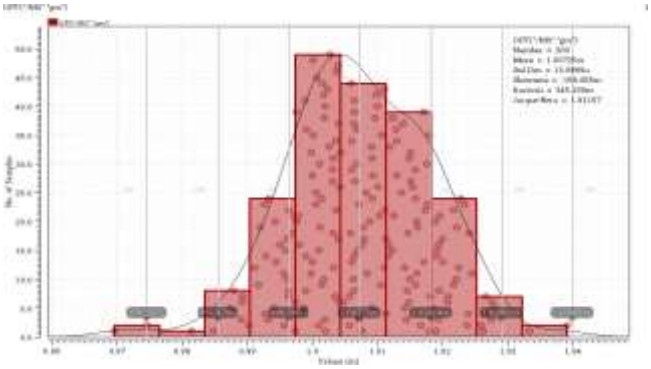

Fig. 14: Monte Carlo Simulation

All the architectures mentioned above use an external off chip resistor which adds to the cost, area, as well as complexity of the circuit.

3.4 Modified Constant G_m Architecture

In this architecture, a differential on-chip resistor is built with the help of an Op-Amp and PMOS biased in the deep linear region as shown in Figure 5. For the design, the value of G_m was chosen to be 1mS while I_{bias} was set to 10µA. As discussed in Section 2:

$$R = {}^{1}/_{G_m} = {}^{\Delta V}/_{I_{bias}} \tag{8}$$

Therefore, from Equation 8 we get R = 1kΩ and ΔV = 10mV.

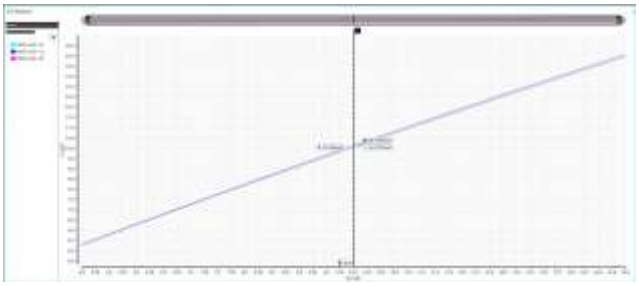

Fig. 15: V-I Curve at Different Process Corners

The current 'I_{gm}' in Figure 6 is mirrored and sent to another test transconductor whose configuration is the same as the 'G_m cell' in Figure 6. The transistor 'M41' of the test transconductor is to be stabilized as hown in Figure 15. The G_m of 'M0' and 'M41' in Figure 6 were swept with process corners, supply voltage, and temperature (PVT variation). 'M0' refers to the NMOS which functions as the tail current source at the input transconductor. 'M41' is the output NMOS whose G_m is to be stabilized.

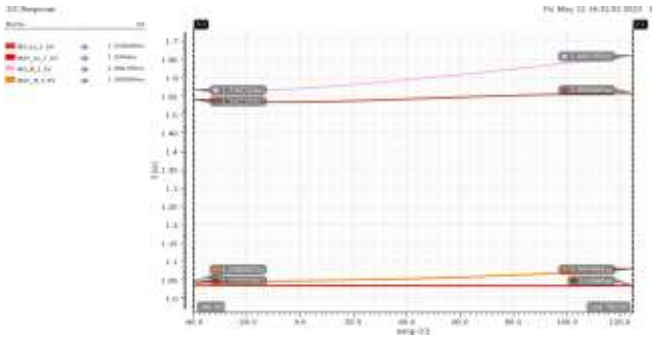

Fig. 16: Gm Variation with Process Corner and Temperature

From Figure 16, it can be observed that the maximum value of G_m is 1.6615mS for M0 and 1.081mS for M41. The minimum value of G_m is 1.5348mS for M0 and 1.036mS for M41. Hence, the error for PVT variation is 3.965% for M0 and 2.108% for M41.

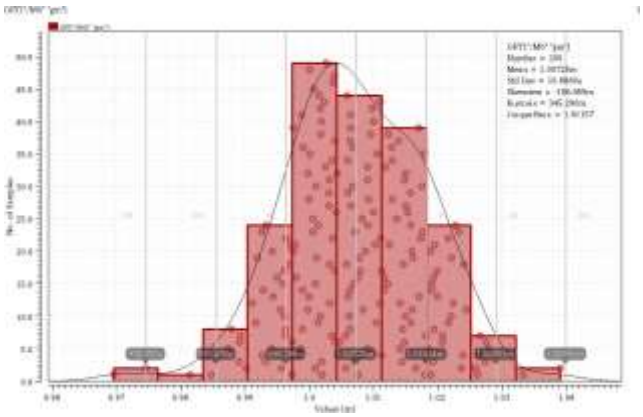

Fig. 17: Monte Carlo Simulation

Figure 17 represents the Monte Carlo Simulation performed for the modified constant G_m architecture. As observed in Figure 17, the standard deviations of 'M0' and 'M41' are 15.1048 µS and 14.9713 µS respectively while their means are 1.55 mS and 1.03 mS respectively. Hence the error in G_m due to mismatch is 2.91% for M0 and 4.32% for M41.

3.5 Comparison of Architectures

The error in the value of G_m across the different architectures is tabulated in Table 4. For the first 2 architectures, Monte Carlo mismatch simulation was not carried out as the error of G_m is very high. Monte Carlo simulation would increase the error while the architecture is rejected due to the high error caused by PVT variations itself. The second architecture shows an improvement from the first architecture by approximately 13%. This improvement is due to the result of reducing the second-order CLM effect, which was assumed to be negligible in theory for the first architecture.

Table 4. Variation of G_m across Architectures

Sl. No.	Architecture	Error in Gm (%)
1	Standard Beta Multiplier Circuit	35.77% (PVT Variations)
2	Beta Multiplier Circuit with Cascade Stage	22.55% (PVT Variations)
3	Beta Multiplier Circuit with CMFB	7.87% (PVT + Monte Carlo Variations)
4	Modified Constant Gm Circuit	6.43% (PVT + Monte Carlo Variations)

As observed in Table 4, architectures 3 and 4 show a similar percentage of error in G_m. Nevertheless, it is worth to note that an ideal Op-Amp is used in architecture 3 while there are no ideal components used in the simulation of Architecture 4. Along with variations in G_m, the first 3 architectures require an external off-chip resistor. This increases the complexity, cost, and area of the circuit. This problem is eliminated in the fourth architecture as an on-chip resistor is designed using transistors.

4 Conclusion

The different architectures were designed and simulated successfully and the error in G_m was noted down. The standard beta multiplier circuit had an error of 35.77% in the transconductance due to PV variations alone. The large value in error is due to CLM. A cascade stage added to the standard beta multiplier circuit showed an improvement of 13.22% as the cascade stage shields the input transistor pair from the supply voltage, hence reducing CLM. Further, the usage of common mode feedback, which reduces the effect of CLM significantly showed an improvement of 17.92% from the cascade version. The aggregate error with using feedback is 7.87%, which includes errors due to PVT variations and Monte Carlo mismatch. The feedback amplifier used is an ideal VCVS. Hence, it is to be noted that in the practical case, the error will increase further due to the usage of nonideal

elements. The proposed architecture, which stabilizes the transconductance through negative feedback with the help of an on-chip resistor shows an improvement of 1.442%.

Additionally, all the architectures apart from the proposed one, require an off-chip resistor. This introduces additional parasitic capacitance and inductance, which can degrade the performance of the circuit by introducing unwanted delays, signal distortion, and noise. Moreover, off-chip resistors require additional space on the circuit board, and also increase the complexity of the manufacturing process, as they need to be individually placed and soldered onto the board.

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