New, Fast, High-Performance Level Shifter for Buck DC-DC Converter in 180nm CMOS Technology

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Abstract: - To reduce power dissipation, the dual supply voltage approach is required for analog circuits in the on-chip integrated circuits. In this paper, a novel circuit of the level shifter for Buck DC-DC Converter using cross-coupled configuration is presented. The proposed work of this paper uses this level shifter to converter voltage of 1.8V to 5V at 180 nm CMOS Technology in Cadence Virtuoso Tool. The propagation delay, energy/transition, and static power were 182.42pS, 0.01 fJ/Transition, and 6 fW, respectively. The final design area is only 60.142 µm2.

Key-Words: - Level Shifter; Gate Driver; Propagation Delay; Dual-Supply; Cross-Coupled, Buck DC-DC Converter.

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1 Introduction

The demand for SOC devices in industries such as automotive has increased in recent years, requiring efficient power management designs and nanoscale CMOS technologies, [1].

DC/DC converters use multiple external components, including inductors, storage capacitors, bootstrap capacitors, and compensating circuit components. By integrating these components onto the chip, the number of external components can be reduced. The level shifter can be the sole component in the high-side power driver, eliminating the need for the bootstrap capacitor, as depicted in Figure 1, [2]. However, the level shifter is an always-on circuit, which results in reduced power conversion efficiency when used as a gate driver due to its high power consumption.

A System-on-Chip (SoC) integrates multiple power supply environments using level shifters to communicate between low and high-voltage power supplies. To reduce power consumption and propagation delay, the design of the level shifter needs to be optimized. [3], [4], proposes a floating voltage level translator that can convert signal levels from low voltage power rail circuit domains to floating power and ground rail circuit domains with high resistance to orbital translation.

Subthreshold shifters in [5] and [6], use self-driven current limiters to detect output errors for robust voltage transitions. The proposed design converts input signals from 0.1 to 1.2V and utilizes a level shifter to convert low voltage levels to high voltage levels, [7], [8].

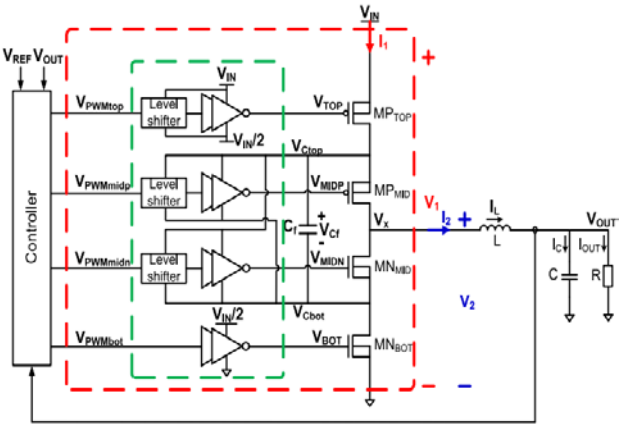

Fig. 1: Three-level buck dc-dc converter topology and driving scheme, [2]

The bootstrap methodology is used to convert the subthreshold supply to the nominal supply, [9], [10]. Other solutions use level-shifting capacitors that are charged to provide higher voltage inputs, resulting in low power dissipation, short propagation delays, a wider switching voltage range, and high operating frequency, [11].

In this work, a cross-coupled configuration transistor-based level shifter for a buck DC-DC converter has been designed, simulated, and layouted in 180 nm CMOS technology. The circuit

offers a low-cost, compact, and high-performance voltage-level conversion solution that operates across a wide range of voltages. Simulation results at 1 MHz indicate that the proposed level shifter has improved delay propagation compared to state-of-the-art designs, [12], [13], [14], [15].

The paper is organized as follows: Section 2 introduces the proposed level shifter for the buck DC-DC converter. Section 3 compares the performance of the proposed design with prior art. Finally, Section 4 concludes the paper.

2 Design and Build a Level Shifter Circuit

2.1 Context

Many level shifter designs have been presented in the literature to solve the problems with the traditional level shifter structures discussed in Section 1. [15], examines and contrasts the level shifter circuit's different properties. However several important and pertinent issues need to be solved.

The structure described in [15] and shown in Figure 2 uses a pull-up configuration that uses a basic current mirror (CM) configuration. This circuit design has a short propagation delay, but the structure uses more than thirteen devices in total; six CMOS transistors (M1, M2, M3, M4, M5, and M6), two capacitors (C1 and C2), one resistor (R1), two inverters, one NAND gate and one diode (D1) this makes it more susceptible to process change and consumes more space.

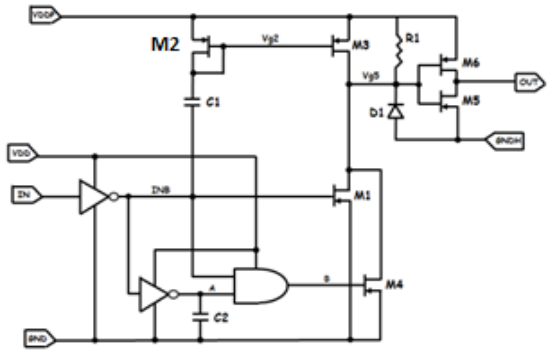

Fig. 2: Conventional level shifters, [15]

Since the transistor, M5 body diode with NPN diode-connected, storage/recovery may not be modeled. Furthermore, M1 may not allow Vgs of the M5 node to be pulled down which means that a one-shot pulse pulls down on Vgs (M5), the device's leakage current is high, which leads to a large current and static power consumption. Another issue is that the propagation delay does not increase well with voltage due to the pull-up transistors' constant weakening.

We propose a new level shifter architecture with fast transition and small area consumption after fully analyzing the advantages and disadvantages of the present designs.

2.2 Proposed Level Shifter

The schematic of the proposed voltage level shifter is shown in Figure 3. The suggested level shifter is developed with the aid of a cross-coupled configuration technique. The proposed architecture of the level shifter includes an input inverter (transistor MN1 & MP1), a cross-coupled configuration (transistor MP5 & MP6), three inverters (transistor MN2 & MP2, MN3 & MP3, and MN4 & MP4), and an output inverter (transistor MN5 & MP7). A CMOS inverter with PMOS and NMOS transistors makes up the input branch. Table 1 shows the transistor sizes that we used in this work.

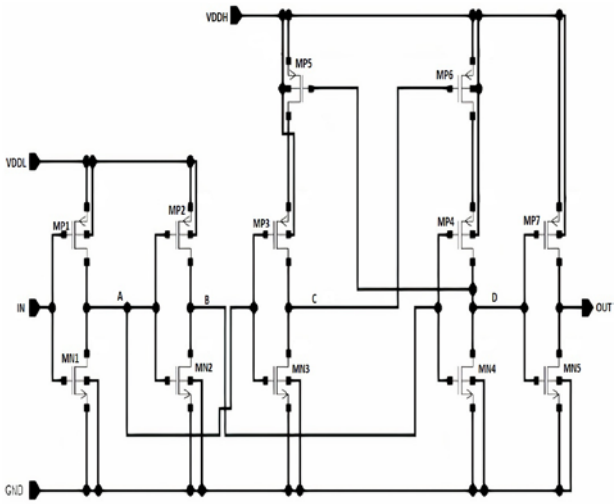

Fig. 3: Proposed Level-Shifter

Table 1. Transistor sizes

Devices	W/L (nm)
MP1, MP2, MP3, MP4, MP5, MP6, MP7	400/180
MN1, MN2, MN3, MN4, MN5	400/180

When the input is LOW, nodes B and C are LOW, while nodes A and D are HIGH. The voltage at node C is zero because the node is HIGH and connected to the ground. The MP6 transistor will switch on when the gate terminal is linked to node C, and the MP6 transistor's drain is connected to node D. Because the node voltage is high, the output

inverter's input is also high, resulting in low output. As a result, the output is similar to that of VIN.

Nodes B and C will be HIGH when the input is HIGH, whereas nodes A and D will be LOW. Because node D is low, MN5 is turned off and MP7 is turned on, resulting in high output, similar to VDDH.

3 Results and Comparison

The proposed level shifter has been designed using 180nm CMOS technology. Its performance was compared with a r eference circuit, [15]. Both circuits underwent various analyses including temperature, frequency, and corner analysis. Temperature analysis was performed at a co nstant frequency of 1MHz, with VDDL = 1.8V and VDDH = 5V, by increasing the temperature from -20 to 100°C.

The four main performance criteria analyzed for good level shifter functioning in this section are propagation delay, power consumption, energy per transition, and silicon area.

The proposed level shifter for a b uck DC-DC converter has been implemented in a 180 nm technology with a single poly and six metal layers. The active area of the level shifter, as shown in Figure 4, is approximately 60.142 μm2 (16.66 μm x 3.61 μm).

The transient results of the proposed level shifter with VDDL=1.8V and VDDH=5V are depicted in Figure 5. At a frequency of 1MHz, the proposed circuit operates at a nominal temperature of 27°C, covering three corners: Nominal-Nominal (N-N), Slow-Slow (S-S), and Fast-Fast (F-F).

The propagation delay of the proposed level shifter varies with changes in VDDL across three corners (N-N, S-S, F-F) and three temperature settings, as depicted in Figure 6. The propagation delay decreases significantly as VDDL increases, which is anticipated. Additionally, when the temperature rises from -20°C to 100°C, the nominal corner's propagation delay decreases from 1.4 ns to 0.74 ns at VDDL = 1.8V.

The propagation delay at 27°C for the N-N corner was achieved at 0.9 ns when the VDDL increased from 1.2 volts to 2.4 volts. The worst-case propagation delay was 7.4 ns at the S-S corner and -20°C, while the best-case propagation delay of 0.42 ns occurred at 100°C in the F-F corner.

Figure 7 illustrates the relationship between power consumption and VDDL for the proposed level shifter. The simulation results indicate that the nominal static power, measured at 27°C with VDDH = 5V and VDDL ranging from 1.2V to 2.4V, saturates at 6fW for 1.2V VDDL. When VDDL is 1.2V below the S-S corner at -20°C, the level shifter consumes just 5.5fW. Its maximum power, at 2.4V below the F-F corner and 100°C, is 20fW.

A 2000-point Monte Carlo simulation was performed at the N-N corner with a VDDL of 1.8 V to evaluate the robustness of our level shifter (refer to Figure 8).

The largest number of samples were collected at 182.42 ps during a delay event, which is as expected. The highest number of samples in terms of static power was reported at 29.52 nW.

Figure 9 shows that as temperatures fluctuate between -20°C and 100°C, the static power differs among various corners. Notably, the F-F corner experiences a much more substantial change in static power compared to the other two corners. Specifically, the static power at the F-F corner rises to 21.5 fW, whereas at the N-N corner, it only increases by 13 fW. However, the S-S corner undergoes a lesser variation in thermal power, with an increase of merely 12 fW.

The proposed level shifter's propagation delay, energy per transition, and total power are compared with those in [15], in Figure 10. At 1.8V, the level shifter in [15], had a delay of 1.2 ns, which is four times greater than the delay observed in our work under the same conditions. This provides strong evidence of the higher speed of our level shifter.

At low supply voltages (VDDL), our proposed level shifter may have a better performance than two other level shifters in terms of energy consumption per transition. As can be observed, at VDDL=1.8V, it uses 0.01fJ, while the circuits proposed in [15], consume hundreds of femtojoules (5pJ) of energy. As a result, our proposed level shifter could outperform the one proposed in [15]. A comprehensive comparison with previous works, is summarized in Table 2.

4 Conclusion

In conclusion, a low-size, fast, and high-performance level shifter for Buck DC-DC Converter using cross-coupled configuration has been successfully designed in 180 nm technology. Circuit design, simulation, analysis, and layout design are all included in this study. The performance of the level shifter is enhanced in this study. The propagation delay, energy/transition, and static power were 182.42pS, 0.01 fJ/Transition, and 6 fW, respectively. The final design area is only 60.142 um2. The level shifter super characteristics

are suitable for various applications such as automotive applications or IoT systems where various devices from different applications and voltage levels are involved.

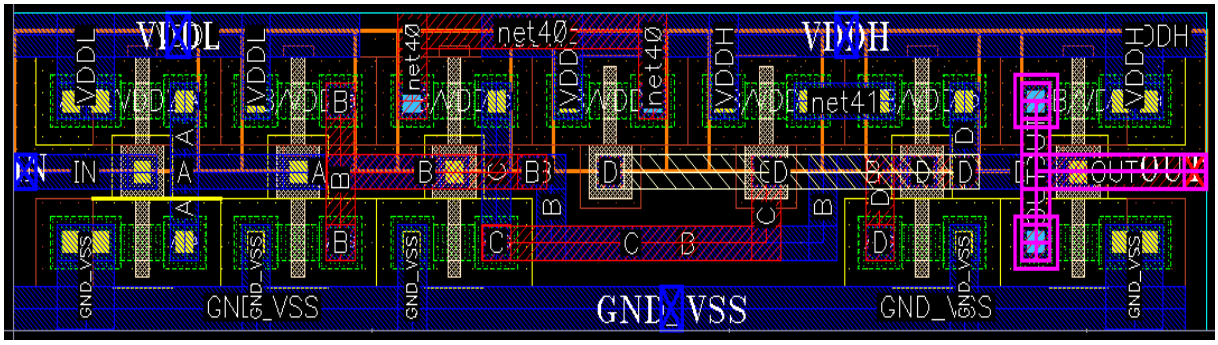

Fig. 4: Proposed level shifter layout

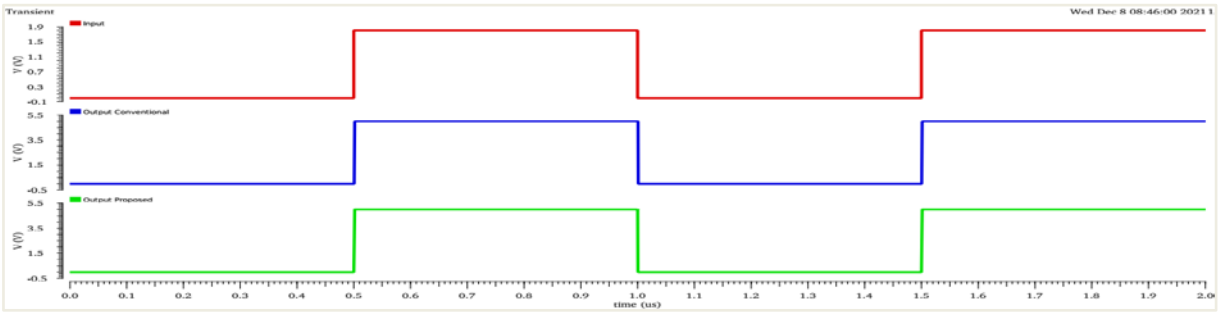

Fig. 5: Level shifter simulation transient results

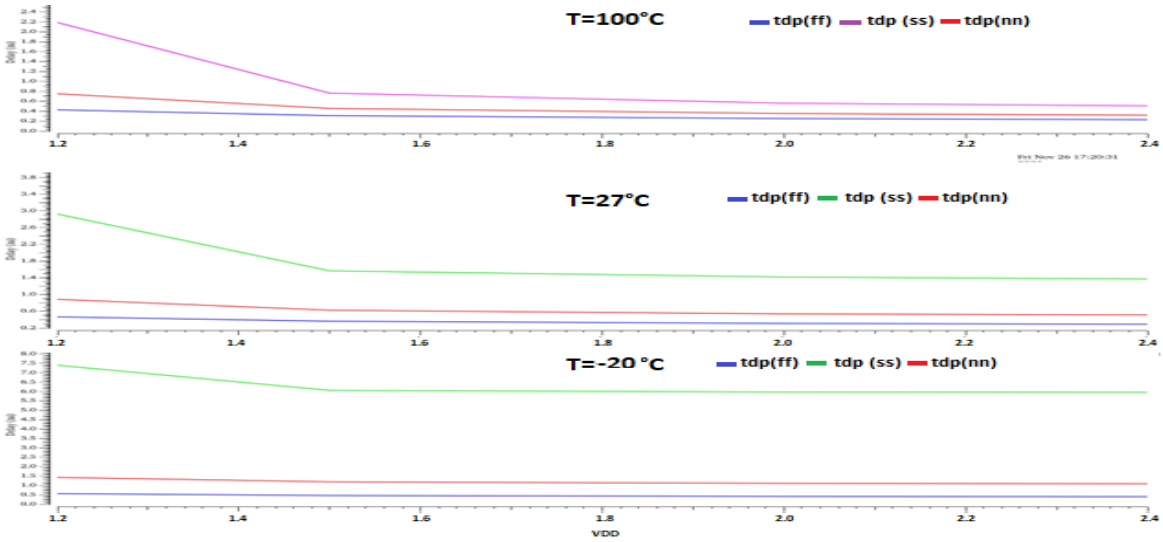

Fig. 6: Propagation delay vs VDDL for three corners at temperatures varies

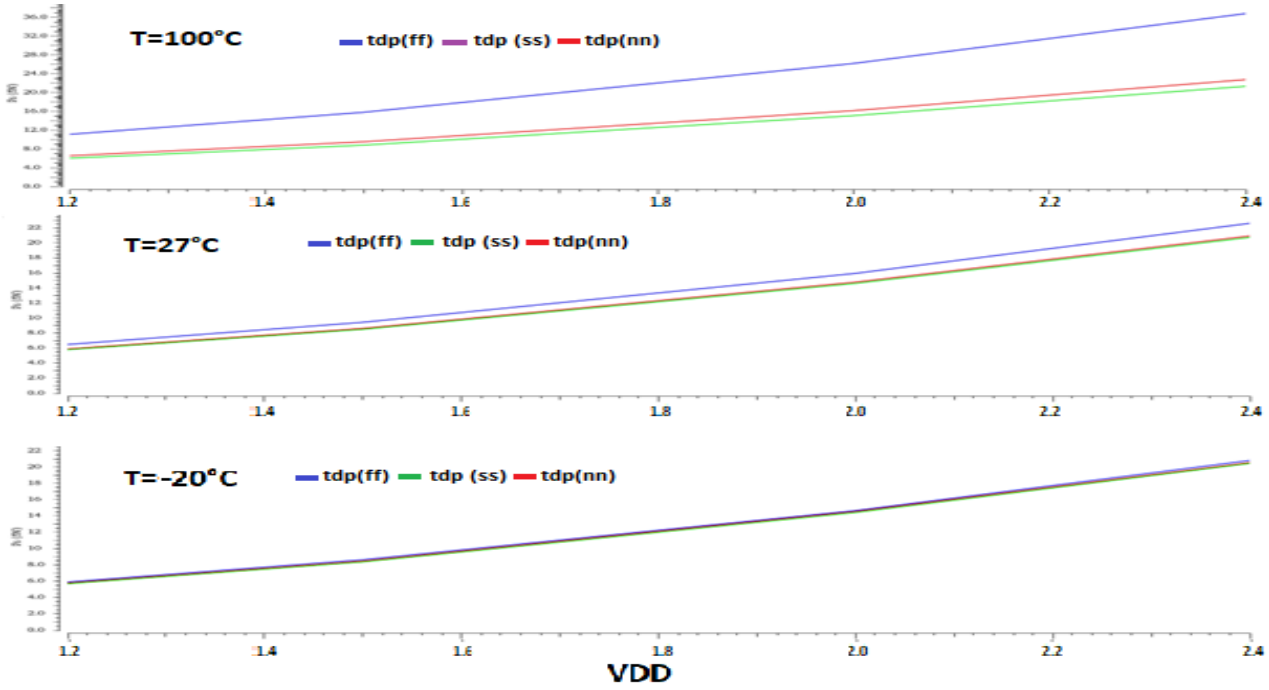

Fig. 7: Static power vs. VDDL variations for three corners at different temperatures

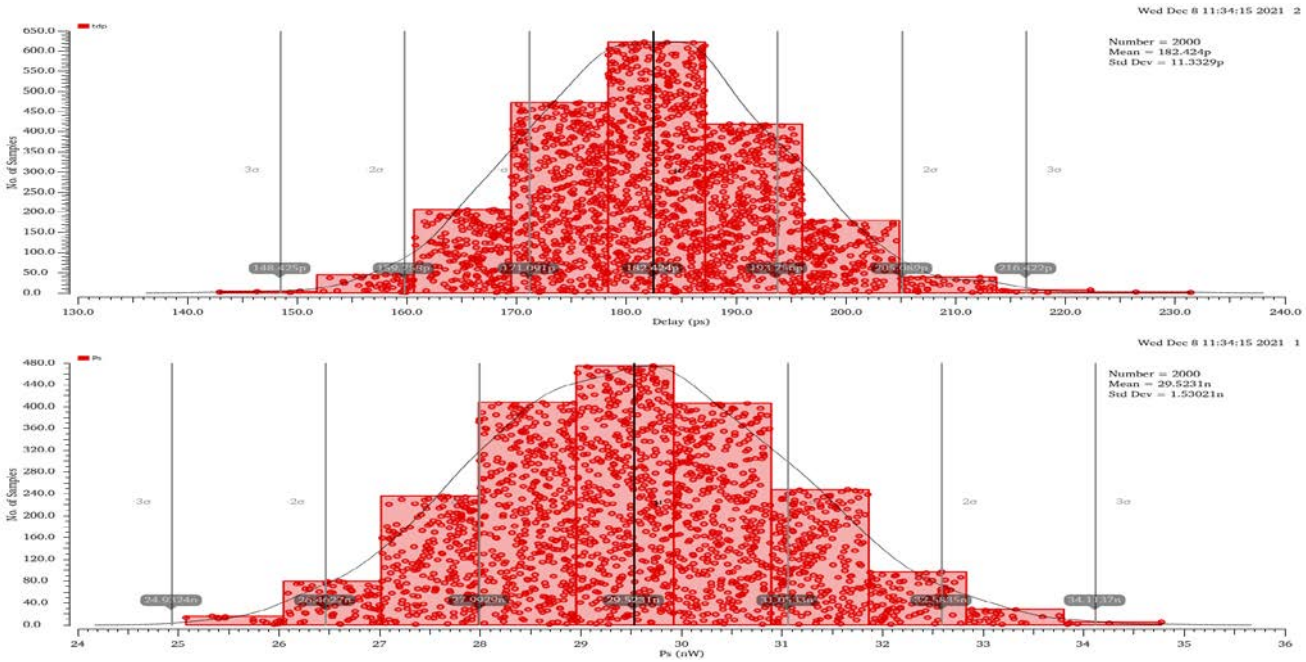

Fig. 8: Monte Carlo simulation of propagation delay and static power consumption

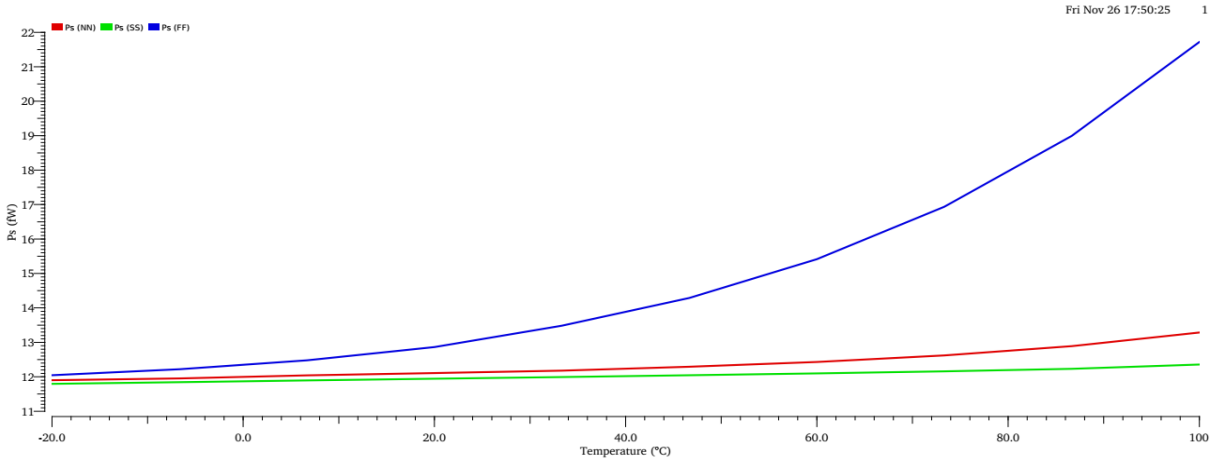

Fig. 9: Static power vs temperature of the proposed level shifter

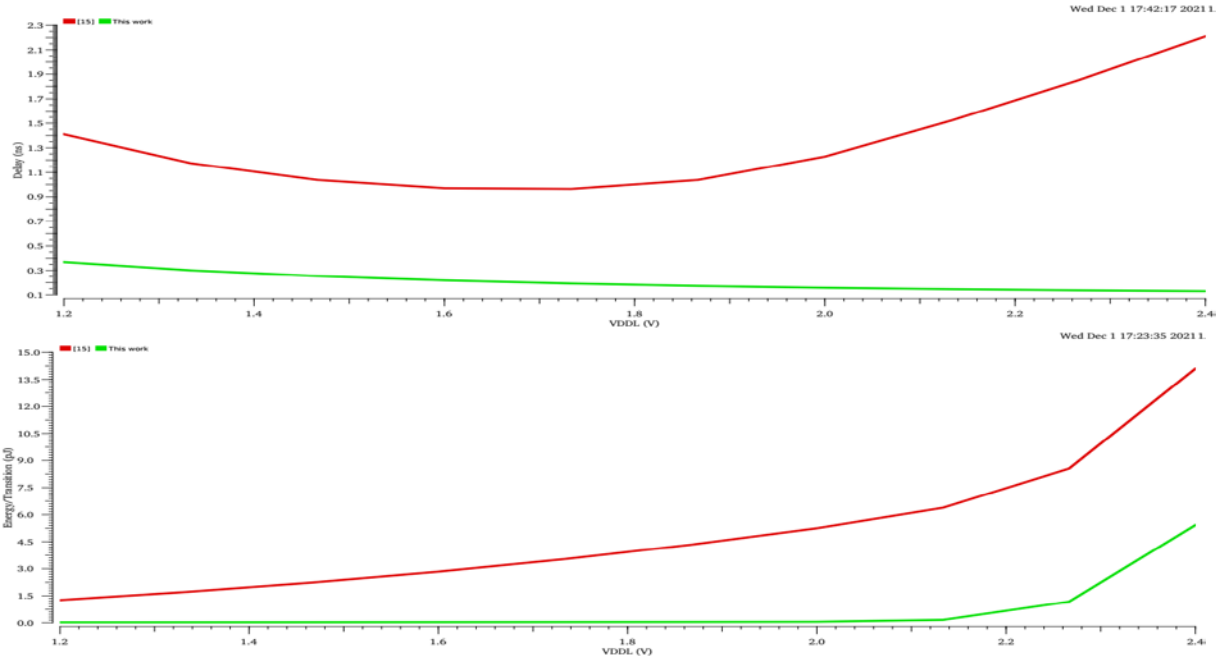

Fig. 10: Delay–energy-characteristics comparison

Table 2. Performance comparison with previous work

	[12]	[13]	[14]	[15]	This work
Year	2021	2021	2020	2019	2022
Technology (nm)	180	180	60	180	180
Results	sim	sim	sim	sim	sim
VDDL (V)		0.24	1.2	1.8	1.8
VDDH (V)	1.8	1.8	6	5	5
Operating frequency (Hz)	100M	100M	800M	1M	1M
Energy(fJ/Transition)	81.7	38.39	-	-	0.01
Pstatic (W)	33.5p	98.3p	113n	-	6f
Delay (s)	854.2p	6.43n	0.63n	1.1n	182.42p
Area (µm2)	-	-	107	50000	60.142

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The author contributed to the present research, in all stages from the formulation of the problem to the final findings and solution.

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The authors have no conflict of interest to declare.