Designs of Electronic Devices using Combinatorial Optimization

VOLODYMYR RIZNYK
Department of Computer Aided Control Systems,
Lviv Polytechnic National University,
79013, Lviv-13, Stepan Bandera Str., 12,
UKRAINE

Abstract: - This paper involves design techniques of electronic devices by combinatorial optimization for improving the quality indices of electronic devices or systems concerning performance reliability, transformation speed, positioning precision, and functionality, using proposals based on remarkable properties and structural perfection of combinatorial configurations, such as difference sets and "Golomb rulers". These design techniques make it possible to configure electronic devices or systems with fewer elements than at present while maintaining or improving on functionality and the other significant operating characteristics of the devices.

Key-Words: - Combinatorial configuration, Golomb ruler, Ideal Ring Bundle, optimization, sequential circuit, code-to-resistance decoding matrix, digital-analog code-to-voltage converter, self-correcting code.

Received: March 13, 2023. Revised: October 12, 2023. Accepted: November 27, 2023. Published: December 31, 2023.

1 Introduction

The Electronics have wide world recognition with connection rapid development in the field of microprocessor and microelectronic technologies within the last few years. Modern electronics is the science of the interaction of fundamental and novel advanced methods for creating electronic devices to convert electromagnetic energy, mainly for the transmission, processing, and storage of information. Circuits constructed from multiple discrete electronic components instead of a packaged IC would typically be extremely high-speed low-resolution power-hungry types, as used in military radar systems. There are problems with improving the quality indices of electronic and mechatronic devices concerning configure code control systems with fewer elements than at present while maintaining functionality, and resolving the ability of the system. S. Golomb developed the idea of using the advantages of multi-bit shift registers with a balanced number of 0 and 1, or 00, 01, 10, 11, revealing in them the absence of autocorrelation, which made it possible to improve encoding systems - decoding signals with correction of errors using sequences generated by shift registers. S. Golomb used versions of these sequences (Reed-Solomon codes) to encode video images of Mars, in CDMA cell phones (Code Division Multiple Access) with multiple access and code separation of communication channels. In 1956, he joined the Glenn L. Martin Company, which later became a defense contractor, [1]. Combinatorial optimization of radio and electronic devices involves techniques for enhancement quality indexes of devices and technologies with non-uniform structures (e.g., linear antennas) based on the theory of combinatorial configurations such as difference sets and "Golomb rulers". The Golomb ruler was named for Solomon W. Golomb. In mathematics, a Golomb ruler is a set of marks at integer positions along a ruler such that no two pairs of marks are the same distance apart. There is no requirement that a Golomb ruler be able to measure all distances up to its length, but if it does, it is called a perfect Golomb ruler. It has been proved that no perfect Golomb ruler exists for five or more marks, [2]. This paper deals with techniques for enhanced positioning precision and discrete resolution of electronic systems, using combinatorial theory [3] and novel mathematical principle, based on the Galois fields theory [4], perfect difference sets [5], and a new conceptual model of electronic devices or systems based on the Ideal Ring Bundles (IRBs). The notion is tied closely to concepts proper of computational intelligence under toroidal reference systems, [6]. Ongoing advances improve the link between computational and physical elements, increasing the reliability and functionality of electronic systems using intelligent mechanisms, using design techniques based on remarkable properties and structural perfection of IRBs. Of very importance in the science is the role of mathematical models for the synthesis and optimization of electronic devices, using a novel design based on combinatorial sequencing theory, namely the concept of Ideal Ring Bundles (IRBs) which can be used for the synthesis of the devices or circuits, for improving such quality indices as reliability, precision, speed, resolving ability, and functionality.

2 Ideal Ordered Combinatorial Constructions

The "ordered chain" approach to the study of elements and events is known to be of widespread applicability and has been extremely effective when applied to the problem of finding the optimum ordered arrangement of structural elements in a distributed technological system.

2.1 Sums On Ordered-Chain Sequence

Let us calculate all S_n sums of the terms in the numerical n-stage chain sequence of distinct positive integers $C_n = \{K_1, K_2, \ldots, K_n\}$, where we require all terms in each sum to be consecutive elements of the sequence. The maximum such sum is the sum $K_1 + K_2 + \ldots + K_n = T$ of all n elements; and the maximum number of distinct sums is:

$$S_n = 1 + 2 + \ldots + n = n\,(n+1)/2 \qquad (1)$$

2.2 Sums On Ordered-Ring Sequence

If we regard the chain sequence C_n as being cyclic, so that K_n is followed by K_1, we call this a ring sequence. A sum of consecutive terms in the ring sequence can have any of the n terms as its starting point, and can be of any length (number of terms) from 1 to $n - 1$. In addition, there is the sum T of all n terms, which is the same independent of the starting point. Hence the maximum number of distinct sums $S(n)$ of consecutive terms of the ring sequence is given by:

$$S(n) = n\,(n-1) + 1 \qquad (2)$$

Comparing equations (1) and (2), we see that the number of sums $S(n)$ for consecutive terms in the ring topology is nearly double the number of sums S_n in the daisy-chain topology, for the same sequence C_n of n terms.

Definition. An n-stage ring sequence $C_n = \{K_1, K_2, \ldots, K_n\}$ of natural numbers for which the set of all $S(n)$ circular sums consists of the numbers from 1 to $S(n) = n\cdot(n-1) + 1$, each number occurring exactly R- times is called an "Ideal Ring Bundle" (IRB), [6].

Here is an example of an IRB with n=5 and $S(n)$ = 21, namely {1, 3, 10, 2, 5}. To see this, we observe:

1=1 6=5+1 11=2+5+1+3
16=1+3+10+2
2=2 7=2+5 12=10+2 17=10+2+5
3=3 8=2+5+1 13=3+10
18=10+2+5+1
4=1+3 9=5+1+3 14=1+3+10
19=5+1+3+10
5=5 10=10 15=3 =10 =2
20=3+10+2+5
21=1+3+10+2+5

Note that if we allow summing over more than one complete revolution around the ring, we can obtain all positive integers as such sums. Thus:

22=1+3+10+2+5+1, 23=2+5+1+3+10+2, etc.

Next, we consider a more general type of IRB, where the $S(n)$ ring-sums of consecutive terms give us each integer value from 1 to M, for some integer M, exactly R times, as well as the value of M +1 (the sum of all n numbers) exactly once. Here we see that:

$$M = n\,(n - 1) / R \qquad (3)$$

An example with n = 4 and R = 2, so that M = 6, is the ring sequence (1, 1, 2, 3), for which the sums of consecutive terms are:

1, 1, 2, 3;
1 + 1 = 2, 1 + 2 = 3, 2 + 3 = 5, 3 + 1 = 4;
1 + 1 + 2 = 4, 1 + 2 + 3 = 6, 2 + 3 + 1 = 6,
3 + 1 + 1 = 5;
1 + 1 + 2 + 3 = 7.

We see that each "circular sum" from 1 to 6 occurs exactly twice (R=2). We say that this IRB has the parameters n=4, R=2.

3 Design of Electronic Devices by Combinatorial Optimization

3.1 Code-to-Resistance Decoding Matrix

Let's consider an example of constructing a code-to-resistance decoding matrix that can be used to synthesize digital functional units for various purposes (Figure 1).

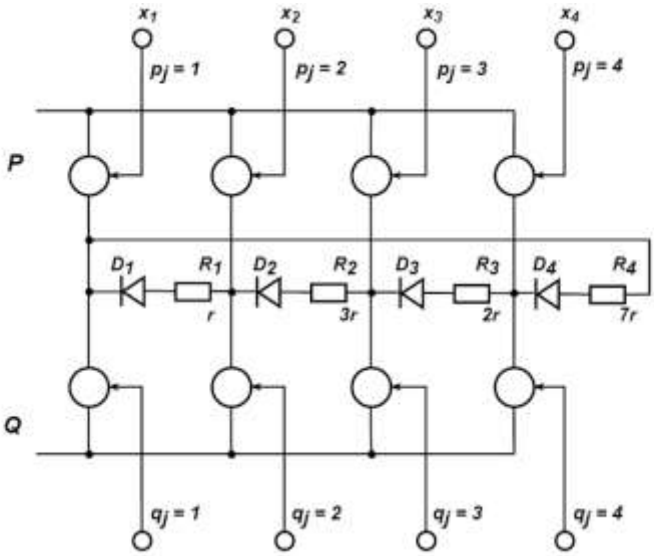

Fig. 1: Code-to-resistance decoding matrix

The matrix (Figure 1) is made in the form of four (n=4) resistors R_1… …R_4 in turn interconnected in series with diodes D_1... D_4. The values of resistances are selected according to the cyclic ratio 1:3:2:7. Two groups of outputs P and Q are connected to the analog output of the digital code-resistance converter "code-resistance" through the code-controlled keys (p_j =1,2,3,4) and (q_j =1,2,3,4). The ratio of least resistance r is equal to $S(n) = (n^2 - n + 1) = 13$-th part of the total resistance of resistors and opened diodes connected in series, where n is the number of keys in each group of the matrix. When the keys are locked in the digits of the same name, the total resistance of the digital converter is equal to zero. For other code combinations, the resistance of the conversion is equal to the appropriate part from the total resistance of the ring circuit connected in series elements, and each code combination (p_j, q_j) corresponds to a new value of resistance from r to $n\cdot(n-1)=4\cdot 3=12r$ with discreteness $r=(R_1+R_2+R_3+R_4)/13$. If the code-to-resistance decoding matrix is designed with the “+” sign of the P side, depending resistance value of the digital converter from code (p_j, q_j) is found in Table 1.

Table 1. Dependence on resistance value of the digital converter from code (p_j, q_j) if the matrix is designed with the “+” sign of the P side

p_j	q_j			
	1	2	3	4
1	0	12r	9 r	7 r
2	r	0	10 r	8r
3	4r	3r	0	11r
4	6r	5r	2r	0

If the code-to-resistance decoding matrix is designed with the “+” sign of the Q side, depending resistance value of the digital converter from code (p_j, q_j) is found in Table 2.

Table 2. Dependence on resistance value of the digital converter from code (p_j, q_j) if the matrix is designed with the “+” sign of the Q side

p_j	q_j			
	1	2	3	4
1	0	r	4 r	6 r
2	12r	0	3 r	5r
3	9r	10r	0	2r
4	7r	8r	11r	0

When one of the keys of group P and one of the keys of group Q are closed in disparate digits, the resistance of the digital converter becomes equal to the total resistance of one or more resistors connected in series, depending on the numbers of the keys to be closed. In this case, each code combination corresponds to a new resistance value. For example, if there are four (n= 4) resistors and four diodes in the decoding matrix, it is possible to implement 12 resistance values with the same increment step, using only two code-controlled keys through which current flows. Such a decoding matrix makes it possible to increase the reliability of digital converters by reducing the number of current-flowed keys, and the code implemented. In turn, in this case, simplifies the detection of single errors, because the presence of more than one unit in at least one of the n-bit combinations, or the presence of all zeros in at least one of the code combinations, indicates an error. If the operating point of the diodes is set at the linear section of the voltage-ampere characteristic, then the value of the resistances of the open diodes remains constant, which can be taken into account. Correctly selected operating mode and load invariability are ensured by circuits, which include DC amplifiers. In the general case, only two current carrying keys are enough to configure a code-to-resistance decoding matrix with any needed step of discreteness $r= (R_1+R_2+…+R_n)/ (n^2 - n + 1)$ and extended operating range using combinatorial optimization based on the IRB-configuration with appropriate parameters.

3.2 Digital-analog Code-To-Voltage Converter

Digital-to-analog converters (DACs) in industrial applications are often used as the controlling element. Digital technology has revolutionized the way most of the equipment works. Data is converted into binary code and then reassembled back into its original form at the reception point. Scheme of digital-analog code-to-voltage converter with minimal number of code-controlled keys through which current flows, given in Figure 2. The device contains two groups of control busbars *P* and *Q* with four (n=4) paired code-controlled keys in group *P*, and four controlled keys in group *Q*.

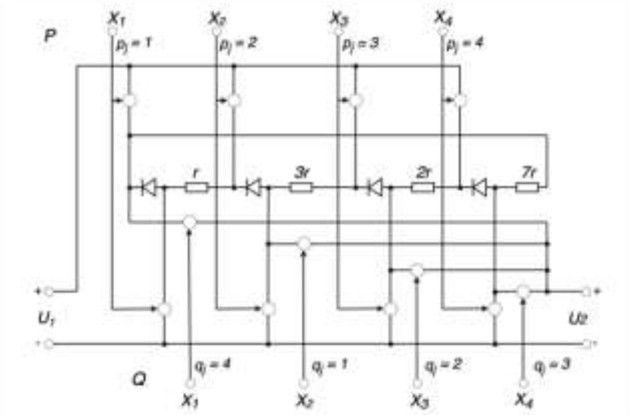

Fig. 2: Scheme of digital-analog code-to-voltage converter

Signals corresponding to the code (p_j, q_j) make it possible to vary the output voltage from 0 to 13u with a step of discreteness $u = U_1/13$ correspondently to Table 3.

Table 3. Dependence on the output voltage of the digital-analog code-to-voltage converter from code (p_j, q_j)

p_j	q_j			
	1	2	3	4
1	u	$4u$	$6u$	0
2	0	$3u$	$5u$	$12u$
3	$10u$	0	$2u$	$9u$
4	$8u$	$11u$	0	$7u$

To see Table 3, we can observe, that the four (n= 4) resistors and four diodes in the decoding matrix make it possible to implement output voltage from 0 to 13u with the increment step $u = U_1/13$. In the general case, only three current carrying controlled keys amply to configure a digital-analog code-to-voltage converters with any needed step of discreteness $u = U_1/ S(n) = U_1/(n^2 - n + 1)$ using combinatorial optimization by selecting IRB with appropriate parameters. Such digital-analog code-to-voltage converter makes it possible to increase the reliability of digital converters by reducing the number of current-flowed keys in a circuit alive. If the operating point of the diodes is set at the linear section of the voltage-ampere characteristic, then the value of the resistances of the open diodes remains constant, which can be taken into account.

3.3 Devices of Forming "Monolithic Codes"

A device of forming monolithic codes designed on the IRB {1,3,2,7} with parameters n=4, R=1 depicted in the scheme (Figure 3).

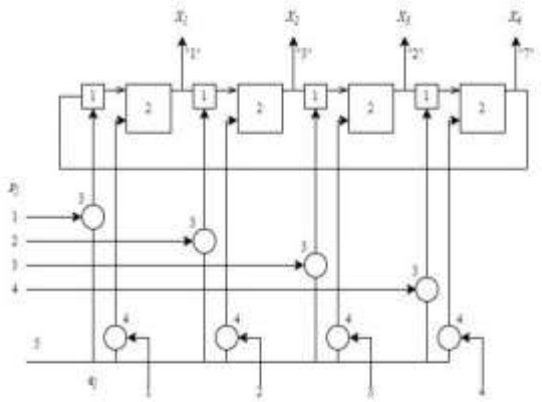

Fig. 3: A device for forming monolithic codes designed on the IRB {1,3,2,7} with parameters n=4, R=1

In the scheme, Figure 3 all logic elements 1 are normally open (NO) contacts, 2 - logic elements OR, while 3 and 4 are code-controlled keys of group *P*, and *Q* correspondently, 5- common power wire. In the initial state keys of both these groups are unlocked, all elements 1 opened, ring chain is de-energized. When one of the keys of group *P* and one of the keys of group *Q* are closed, informative signal "1" enters through selected logic element 2 (OR) into the ring structure, filling the "1" line corresponding numbers connected in series these elements. At this moment signal "1" appears on the output of one or more elements 2 simultaneously, and on the correspondent outputs X_1… X_4 of the device forms a monolithic code combination with digit code weights X_1="1", X_2="3", X_3="2", X_4="7". Forming monolithic code combinations according to digit code weights X_1="1", X_2="3", X_3="2", X_4="7" is in Table 4.

Table 4. Monolithic code combinations according to digit code weights X_1=”1”, X_2=”3”, X_3=”2”, X_4=”7”

Number	Code			
	X_1	X_2	X_3	X_4
0	0	0	0	0
1	1	0	0	0
2	0	0	1	0
3	0	1	0	0
4	1	1	0	0
5	0	1	1	0
6	1	1	1	0
7	0	0	0	1
8	1	0	0	1
9	0	0	1	1
10	1	0	1	1
11	1	1	0	1
12	0	1	1	1
13	1	1	1	1

Here we observe that each allowed code combination forms as a ring sequence of no more than one packets of connected in series symbols “1”, as well as “0”.

Creating monolithic code combinations depending on code (p_j, q_j) based on the IRB {1,3,2,7} is in Table 5.

Table 5. Monolithic code combinations depending on code (p_j, q_j) based on the IRB {1,3,2,7}

p_j	q_j			
	1	2	3	4
1	13	12	9	7
2	1	13	10	8
3	4	3	13	11
4	6	5	2	13

Monolithic code forms code combinations as a ring sequence of solid connected symbols “1” as well as “0” for identifying the correct code words at the receiving end using the majoritarian approach to detect and correct errors. This property makes it possible to use self-correcting signals providing concurrently faster than classic code transmission in a noise channel.

4 Discussion

As is evident, the conceptual model of electronic devices or systems based on the Ideal Ring Bundles (IRBs) demonstrates the advantages of the underlying innovative combinatorial methodology, and values of structural elements (resistances, digit code weights, etc.) are selected according to the cyclic ratio of consecutive terms of the ratio. The mutually unambiguous compliance with a set of indexed elements of a set of binary code combinations formed by this device has been achieved in the system. In turn, it was possible due to reducing the natural redundancy in the system. Instead, Table 1 and Table 2 give examples of the code-to-resistance decoding matrix, depending resistance value of the digital converter according to the cyclic ratio 1:3:2:7 organized from the IRB with parameters n=4, S=13, R=1.

Reasoning along similarly, in the next tables related designing digital-analog code-to-voltage converter (Table 3), forming monolithic code combinations according to digit code weights X_1=”1”, X_2=”3”, X_3=”2”, X_4=”7”, based on the IRB {1,3,2,7} (Table 4), and creating monolithic code combinations depending code (p_j, q_j) (Tables 5). Equations (2) and (3) formalize a large class of one- and multi-dimensional optimized binary IRB-codes from non-redundant vector codes of high performance to coding self-correcting vector data signals with faster than classic codes transmission of multidimensional information by noise communication channels. One of them is an optimum binary monolithic star- code for processing two- or multidimensional vector signals under a toroidal coordinate system, [6]. Digital-to-analog converters (DACs) typically comprise a digital encoder and a set of current steering switches, capacitive cells, other elements such as resistor strings, or a combination of these, bringing about mismatches among the components that make up the DAC introduce nonlinear error. This technique, referred to as dynamic element matching (DEM), eliminates component mismatches as a distortion-limiting factor in many practical cases by making the system linear on average by virtue of its shuffling scheme, [7], [8], [9], [10]. Proposed in [7], DAC can achieve comparable performance as the conventional ones with two fewer MSB bits used for DEM, which simplifies the DEM block significantly by reducing the MUX count. Paper [8], analyzes a calibration technique that circumvents the need for RZ pulse shaping by adaptively measuring and canceling ISI over the DAC’s first Nyquist band. As demonstrated in the paper [9], it is possible to devise algorithms that cancel errors in the Nyquist band of interest. The results apply to most multi-bit DAC architectures and all types of DEM known to the authors, and they reduce to previously published continuous-time DEM DAC results in the absence of ISI. The paper [10], describes two techniques that are inherently more linear than prior-art DACs, namely the virtual-ground-switched resistor DAC and the zapped virtual-ground-switched dual return-to-open DAC. Flicker noise can be eliminated by chopping, but one needs to pay careful attention to minimize chopping artifacts.

5 Conclusion and Outlook

Designs of electronic devices using the remarkable properties and structural perfection of IRBs provide an ability to reproduce nearly double the number of combinatorial varieties the number in the Golomb rulers, so long as an ability to configure electronic devices with a limited number of elements and bonds, while maintaining or improving on resolving ability and the other operating characteristics of the devices. Therefore, a code-to-resistance decoding matrix designed from an IRB makes it possible to increase the reliability of digital converters by reducing the number of current-flowed keys. Moreover, in this case simplifies the detection of single errors. A digital-analog code-to-voltage converter makes it possible to increase the reliability of digital converters by reducing the number of current-flowed keys. If the operating point of the diodes is set at the linear section of the voltage-ampere characteristic, then the value of the resistances of the open diodes remains constant, which can be taken into account. Optimized monolithic code provides detecting and self-correcting signals faster than classic codes. The underlying design techniques provide configure codes that have been defined as the optimized binary weighed ring monolithic codes with a priory any needed step of discreteness and extended operating range, forming a large class of performance self- correcting coded signals with faster than classic codes transmission of information by noise communication channels. These design techniques make it possible to configure electronic devices or systems with fewer elements than at present, while maintaining or improving on functionality and the other significant operating characteristics of the devices. Prospect for further research is the development of combinatorial techniques in electronic devices and systems for improving such quality indices as reliability, transmission speed, positioning precision, and ability to reproduce the maximum number of combinatorial varieties in the system with a limited number of elements and bonds, using remarkable properties and structural perfection of IRBs. The Ideal Ring Bundles provide, essentially, a new conceptual model of electronic devices. Moreover, the optimization has been embedded in the underlying combinatorial models for direct applications in electronic engineering to offer ample scope for progress in sciences, technology, and commerce.

References:

[1] Golomb, B.; Gong, G.; Hales, A., eds. (2023). *The Wisdom of Solomon: The Genius and Legacy of Solomon Golomb*. World Scientific, https://doi.org/10.1142/12211.

[2] Shearer, J. B., (19 February 1998). *"Table of lengths of shortest known Golomb rulers"*. IBM. Archived from the original on 25 June 2017.

[3] M. Jr. Hall, *"Combinatorial Theory,"* 2nd Edition, Wiley-Interscience, 1998, 464 p.

[4] Rotman J. *Galois Theory*. 1998. 106 p. DOI: 10.1007/978-1-4612-0617-0.

[5] E.H. Moore, H.S. Pollatsek, *Difference Sets: Connecting Algebra, Combinatorics, and Geometry*, AMS, 2013.

[6] V. V.Riznyk, "Formalization coding methods of information under toroidal coordinate systems", *Radio Electronics, Computer Science, Control*. 2021. № 2, pp.144-153. DOI.10.15588/1607-3274-2021-2-15.

[7] Wei Mao, Yongfu Li, Chun-Huat Heng and Yong Lian, "High dynamic performance current-steering DAC design with nested-segment structure", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 5, pp. 995-999, May 2018. DOI: 10.1109/TVLSI.2018.2791462.

[8] D. Kong and I. Galton, "Adaptive cancellation of static and dynamic mismatch error in continuous-time DACs", *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 65, no. 2, pp. 421-433, Feb. 2018. DOI: 10.1109/TCSI.2017.2737986.

[9] J. Remple and I. Galton, "The effects of inter-symbol interference in dynamic element matching DACs", *IEEE Trans. Circuits Syst. I Reg. Papers*, vol. 64, no. 1, pp. 14-23, Jan. 2017. DOI: 10.1109/TCSI.2016.2601026.

[10] Enrique Alvarez-Fontecilla; Paul S. Wilkins; Steven C. Rose, "Understanding high-resolution dynamic element matching DACs (feature)," *IEEE Circuits and Systems Magazine*, vol.23, Issue 4, Fourthquarter 2023. DOI: 10.1109/MCAS.2023.3325504.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)
The author contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself
No funding was received for conducting this study.

Conflict of Interest
The author has no conflicts of interest to declare.