On-Chip Tunable Active Inductor Circuit for Radio Frequency ICs

RAJNI PRASHAR, GARIMA KAPUR
Department of Electronics and Communication,
Jaypee Institute of Information and technology,
A-10 Sector 62, Noida, Uttar Pradesh,
INDIA

Abstract: - The work presents a design of a gyrator-based on-chip tunable active inductor (AI) which can become an integral part of high-frequency integrated circuits. The proposed AI uses the Floating gate technology-based PMOS (FGPMOS) simulation model, where the on-chip, non-volatile programming ability of FGPMOS is used as a tunable active feedback resistor. The circuit specifications are first derived for the application at 800MHz to 2GHz. The design is simulated at 350nm CMOS technology and shows a temperature sensitivity of 0.13mV/^{o}C as well as a noise sensitivity of about 10.97nV/Hz. The precise programming range of inductance value from 3nH to 9nH can be achieved. The circuit has a power dissipation of 5.02mV and a moderately high-quality factor of about 120. The layout of the proposed circuit has been designed on Cadence Virtuoso and fabricated at ON-Semiconductor, C5 CMOS process foundry of MOSIS fabrication service, USA. The complete design has a chip area of 18x30µm^2. The fabricated results illustrate the on-chip tuning ability of the proposed AI from 3nH to 7nH with the help of externally applied Tunnelling and Injection voltages, respectively. The proposed design also simulates a tunable bandpass filter and a tunable Low Noise Amplifier.

Key-Words: - Tunable Active Inductor, Floating Gate, Monolithic Microwave ICs, Radio-Frequency ICs

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1 Introduction

Wireless technology is regularly emerging and growing rapidly and it has changed significantly for the past decade. This technology has completely replaced the wired technology and will continue to expand its wings into the near future. The current trend in technology has moved towards employing advanced semiconductor techniques, including silicon germanium (SiGe) and silicon-on-insulator (SOI) technologies, for the integration of on-chip adjustable active inductors. These processes offer improved performance, higher integration levels, and lower power consumption. Modern tunable active inductors aim to provide a wide range of tunability to cover a broad spectrum of frequencies. This is crucial for applications like software-defined radios (SDRs) and cognitive radio, where the operating frequency can vary significantly. o support high-performance RF applications, tunable active inductors are designed with improved linearity to minimize distortion and intermodulation products, ensuring high signal quality. State-of-the-art designs often feature reconfigurable active inductors, allowing for dynamic adaptation to changing operational requirements. This reconfigurability can be achieved through digitally controlled tuning circuits. The integration of digital control interfaces (e.g., SPI or I_2C) allows for precise and flexible control of tunable active inductors. This digital control facilitates system-level optimization and calibration. Power efficiency remains a critical consideration, especially in battery-powered and energy-harvesting applications. New techniques for tuning active inductors include switched-capacitor networks, varactor diodes, and digitally controlled inductance elements. These methods provide fine-grained control over the inductance value. Noise performance is essential in RF and analog applications. Advanced designs incorporate techniques to minimize noise figures and achieve excellent noise performance in addition to high linearity. Tunable active inductors are designed to be more stable over a wide temperature range. The trend is towards monolithic integration of tunable active inductors with other RF and analog circuitry, enabling more compact and highly integrated RF front-end modules. With the deployment of 5G and the ongoing development of beyond 5 G technologies, tunable active inductors play a crucial role in enabling higher data rates and greater spectral efficiency in wireless communication systems.

Over the decade many active inductor circuit designs have been developed so far like in 1994

presenting a monolithic Narrow-band filter that uses the concept of TAI(Tunable Active Inductor) but with a moderate Q value and higher losses, [1]. Subsequently, a fully integrated GaAs MESFET-AI in which both inductance and series loss are independently tuned is proposed by, [2]. However, the fabrication cost was high because of the GaAs technology. In Si technology, various gyrator-based active inductor designs using only transistors have been developed and found their major application in the field of RFIC domain. So, to overcome the drawback AI which works at a 50 GHz mm-wave circuit provides a good Q-factor of 400 at the same frequency, [3]. The current controlled technique to tune the value of inductance is proposed by, [4]. A design of AI and negative capacitance that gives the linear impedance properties, which is useful in broad frequency bands is given by, [5]. The major design issues like the design process and inherent noise sources were reported are elaborated in, [6]. Another approach that can be used to tune the AIs is to use the concept of a floating gate. Many designs have been proposed to realize a large active inductor with a wide tuning range. A floating active inductor-based RF bandpass filter topology which finds diverse application in wireless transceiver and medical science are proposed in, [7].

CMOS active inductors have now become the most integral part of RF/microwave circuit design, this is because quality factor (Q) can be increased. The wide tunability of an active inductor can also be maintained with the advantage of a large inductance value and small chip area, [8]. To achieve tunability various techniques can be used like a current mirror, digital resistive ladder switching, or floating gate approach. One such application of active inductor has been given by, [9], where the filter has been proposed and the direct tuning method is used. Another application of an active inductor is where a fully integrated tunable bandpass filter is designed which utilizes the differential structure to include advantages such as reduced noise effect and increased output voltage swing explained by, [10]. The tuning of the frequency is done with the help of a varactor capacitor. The design uses the current reuse technique to reduce the power consumption of the design and reported the high value of noise figure. Hence in the paper, a CMOS-based AI is designed whose inductance and operating frequency can be tuned using FGMOS technology. The proposed inductor produces inductance ranging from 3nH to 7nH and operates at 800MHz to 2GHz frequencies. The design has been also fabricated using On Semiconductor technology by MOSIS fabrication services, USA, and also tested using Vector Network Analyzer in the Lab. The AI design is compact, consumes low power, and allows stable and precise tuning ability. The first section of the paper proposes AI design, its simulation results, fabricated IC, and fabricated results. The second section of the paper illustrates the vital role of AI designs in several RFIC and MMIC design industries and hence demonstrates our future research work idea.

2 Research Method

RFIC/MMIC systems necessitate components like oscillators, filters, phase shifters, low noise amplifiers, impedance matching circuits, biasing circuits, etc., designed to function within the radio frequency range. An enhanced version of a traditional Gyrator-C active inductor, which incorporates both common-emitter and common-collector configurations with resistance feedback. The static passive resistor is substituted with a tunable active resistor (TAR) to augment the controllability of the active inductor presented by, [11]. One more design that is presented in, [12], implements a gyrator-C-based inductor design but uses a resistor as a feedback path. This design is further improved in this work and the resistor is replaced by FGMOS to introduce the indirect tuning. An important component of these devices is an inductor, and AI implementation in integrated circuits still remains a challenging task. Class AB AI given by, [13], is designed by using two complementary transistors connected in a network, and the value of both inductance and its series resistance value can be varied. In the past, many active inductor circuit designs have been created. Nonetheless, these designs often meet only a limited subset of the desired criteria, including compactness, low-voltage operation, a wide inductance range, low inductance values, a high-quality factor, low power consumption, a broad dynamic range, suitability for RF frequencies, minimal noise, and the capability for precise on-chip tuning. Another component that is used in RFICs is the voltage-controlled oscillator, and the active inductor-based VCO design is proposed in, [14], [16], and the direct tuning of the active inductor is used in place of the MOS varactor. The aim of an on-chip tunable active inductor(TAI) circuit proposed in this paper is to provide a controllable inductance value that can be adjusted or tuned according to the specific requirements of an electronic circuit or system. This type of circuit is particularly useful in integrated circuits (ICs) and radio-frequency (RF) applications where precise control of inductance is needed. The primary goal is to create an inductor whose inductance value can be changed dynamically from 3nH to 9nH where

operating frequency can be tuned from 800MHz to 2GHz. On-chip active inductors are typically smaller in size compared to their passive counterparts, which can be crucial for miniaturizing electronic devices and reducing the footprint of ICs. Active inductors can have a higher quality factor compared to passive inductors. This results in reduced losses and better performance in various RF and analog circuits. The proposed TAI can be integrated with other active components like amplifiers, oscillators, or filters, enabling the creation of compact and highly functional RF front-end circuits. In this work, we showcase a small, adjustable active inductor that we simulated using an FGMOS simulation model and BSIM level MOS models, within a 0.35µm CMOS process environment in Virtuoso (also compatible with T-Spice). This design successfully incorporates nearly all the specifications mentioned earlier while employing an efficient and compact circuit configuration. The design is grounded on a gyrator-based approach, where a single-port circuit is realized with just two MOS devices arranged in tandem. These MOS devices generate an inductive effect at that specific port through their transconductance and junction capacitances. Furthermore, the adjustable FGPMOS resistor within the feedback path allows for the tuning of the inductance, as illustrated in Figure 1(a). The current sources have also been substituted with MOSFETs operating in saturation mode to maintain a steady current under specific sizing (W/L) and biasing (gate voltage) conditions. This facilitates the derivation of the impedance/admittance and the creation of an equivalent passive model for this circuit, as depicted in Figure 1(b).

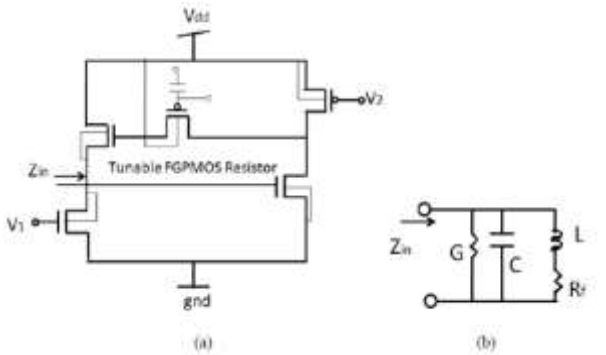


Fig. 1(a): Single-ended Gyrator-C based AI with FGPMOS as an adjustable resistor (b) Gyrator-C based one port AI.

The circuit has been evaluated by replacing the MOS with its small-signal high-frequency model. Consequently, the complete high-frequency circuit model is depicted in Figure 2.

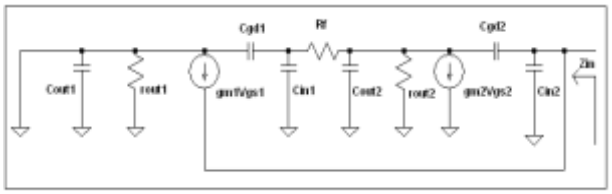


Fig. 2: High-Frequency Model of Single-ended Inductor.

To simplify the analysis, we combine the 'bulk' with its corresponding 'source,' treating both transistors as identical. This leads to identical small-signal model parameters for both MOS devices, which include gate-to-drain capacitances (Cgd), output conductance (gout1, gout2), and transconductance (gm1, gm2). Ideal current sources are used to bias both MOS devices. Consequently, by neglecting the gate-drain capacitances of both MOS devices, we can express the conductance by Eq(1), and Eq(2) and interpret the values of all components illustrated in Figure 1(b)

$$y_{in} \cong sC_{gs1} + g_{ds2} + \frac{(sC_{gs2} + g_{m2})(g_{ds1} + g_{m1})}{sC_{gs2}(1 + R_f . g_{ds1}) + g_{ds1}} \quad (1)$$

$$C \approx C_{gs1}. G \approx g_{ds2} + \frac{g_{m1}}{1+R_f g_{ds1}} L \approx \frac{C_{gs2}(1+R_f g_{ds1}}{g_{m1} g_{m2}} \& R \approx \frac{g_{ds1}}{g_{m1} g_{m2}} \quad (2)$$

Hence, by increasing the feedback resistance value, parallel conductance, and consequently, series resistance can be reduced. This, in turn, enhances the inductance value. Therefore, by adjusting the value of the FGMOS feedback resistor, it becomes possible to tune the inductance value.

2.1 Simulation Model of Tunable Active Inductor

The major advantages of the proposed TAI are typically much smaller than their discrete counterparts, which is essential for miniaturizing electronic devices and enabling the integration of complex RF and analog circuits on a single chip. TAI can be adjusted to match the operating frequency of a circuit or system. This flexibility is crucial in RF applications where the frequency may change dynamically, allowing for wideband and multi-frequency operation without the need for multiple discrete components. Active inductors can have a higher quality factor (Q) compared to passive inductors, resulting in lower losses and improved performance in RF and analog circuits. The ability to tune the inductance value in real-time or based on specific conditions allows for dynamic optimization of circuit performance. Active inductor circuits can be designed to consume less power than equivalent passive inductors, contributing to improved energy

efficiency in battery-powered devices and reducing heat dissipation. Tunable active inductors can be employed in filter and amplifier circuits to achieve precise frequency selectivity and gain control. This is beneficial in applications like wireless communication, where signal bandwidth and power levels need to be adjusted. The proposed TAI can be more resilient to manufacturing process variations compared to passive inductors. This helps maintain consistent performance across different batches of ICs. Tunable active inductors can be customized to meet specific circuit requirements, making them adaptable to various applications and allowing circuit designers to fine-tune their designs for optimal performance. Integration of active components reduces the need for external discrete components, leading to potential cost savings in terms of component procurement, assembly, and testing. Based on the Gyrator-based single-ended grounded Active Inductor and on-chip programming of charge at the floating gate have been explored together to design the proposed TAI. Instead of employing a feedback path resistor, on-chip programmable FGPMOS components have been utilized. Additionally, the default current sources originally utilized in the referenced circuit have been substituted with MOSFETs operating in saturation mode. These MOSFETs ensure a consistent current under specific sizing (W/L) and biasing (gate voltage) conditions.

On-chip tuning Ability: With the help of three voltages at the tunneling junction, drain, and source for the programmer FGPMOS can be used to change the value of inductance extracted from the single end. The resistance at the feedback path value changes with the help of the changing charge at the floating gate. The programming of charge at the floating gate with the help of voltages post-fabrication is non-volatile and highly stable. With the change in feedback resistor, as explained in the equations the value of inductance changes. As shown in the equations the quality factor, and operating frequency can also be programmed with on-chip programming of the feedback resistor value. The programming is also very precise, thus fine-tuning of inductance value can be obtained. The model is designed using BSIM 3 level 49 MOS models, using 0.35um CMOS process, as shown in Figure 3.

The initial results of the AC analysis simulation reveal the inductive behavior of this single-port device, as depicted in Figure 4. It illustrates the frequency response (in GHz) of the voltage at the designated port under an 800MHz input AC signal. Consequently, a peak is observed at the central frequency of 1.2GHz, affirming the presence of inductive traits.

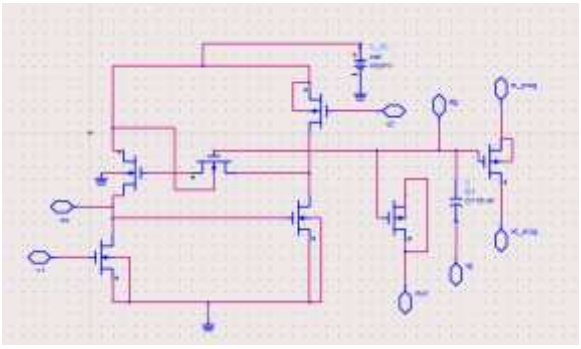


Fig. 3: Proposed active inductor consists of FGPMOS simulation model

Moreover, the on-chip programmable FGPMOS in the feedback path introduces tuning capabilities into the circuit, as shown in Figure 5(a) and Figure 5(b). These figures demonstrate the adjustment of the floating-gate charge through tunneling (Vtun=7.2 to 8.2V), resulting in a self-oscillation frequency range from 700MHz to 1.5GHz. Similarly, with injection (Vinj=6V to -6.5V), the self-oscillation frequencies vary from 600MHz to 1.5GHz, respectively.

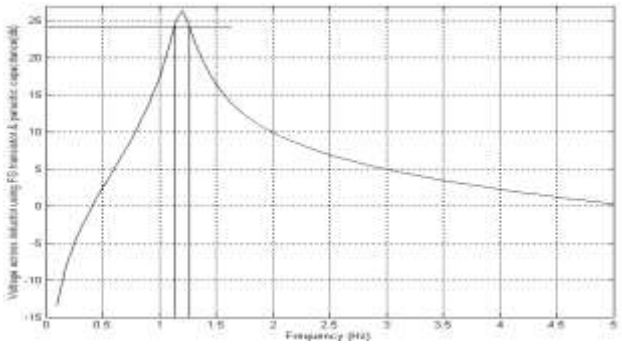


Fig. 4: Frequency response (GHz) of voltage at I/O port with the input signal of 1V ac signal at 800MHz

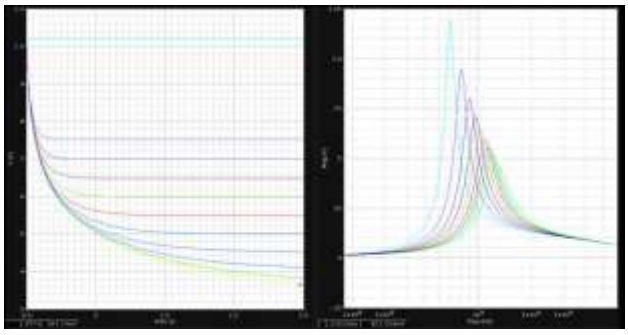


Fig. 5(a): Transient response of floating-gate voltage, $V_{fg,}$ and frequency response of voltage magnitude at I/O port (one port)

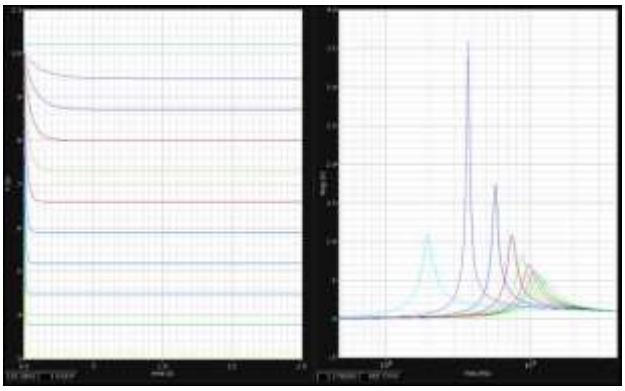


Fig. 5(b): transient response of floating-gate voltage, $V_{fg,}$ and frequency response of voltage magnitude at I/O port

Subsequently, using equations 1 & 2, all the elements within its corresponding passive circuit have been theoretically computed. Consequently, variations in the floating gate voltage (Vfg) result in alterations to the inductor, leading to changes in the feedback resistor (Rf), inductance value, transconductance, and its associated quality factor. These calculations and results have been compiled and presented in Table 1.

Table 1. Component values with respect to floating gate voltages and corresponding operation frequency

V_{fg} (V)	R_f(kΩ)	L (nH)	G (mho)	Q	f_o (GHz)
-0.2	1.8	3.49	146.93	1.21	6.2
-0.8	2.1	3.67	140	1.21	6.2
-1	4.2	4.01	127.95	1.26	4
-1.4	5.1	4.21	122.04	1.8	4
-1.45	6	4.40	116.64	1.54	4
-1.5	7.3	4.68	109.65	1.67	1.7
-1.52	8.15	4.86	105.53	1.67	1.7
-1.55	9.2	5.09	100.83	2.82	1.7
-1.6	11	5.48	93.67	3.33	1
-1.7	16	6.56	78.26	4.2	1

Thus, the inductance programming is within 3nH to 7nH with specific biasing and sizing conditions of the active inductor design. Consequently, impedance at the port has been observed and is shown in Figure 6(a). Subsequently, by applying equations 1 and 2, the theoretical component value is computed. This enabled us to determine how changes in the floating gate voltage (V_{fg}) affect the inductor's value, subsequently impacting the feedback resistor (R_f), and consequently, influencing the inductance, transconductance, and quality factor, as detailed in Table 1. As a result, the programmable inductance spans from 3nH to 7nH, achieved through specific biasing and sizing parameters in the active inductor design. Consequently, we have examined the impedance at the port, and the results are depicted in Figure 6(b)

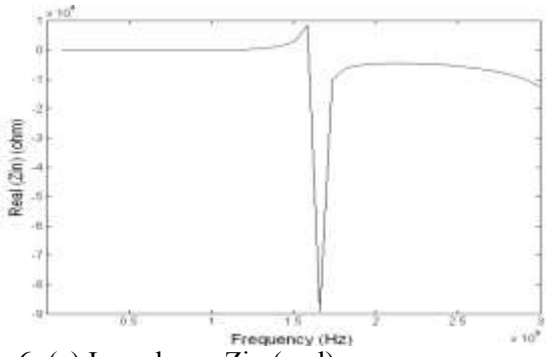


Fig. 6: (a) Impedance Zin (real)

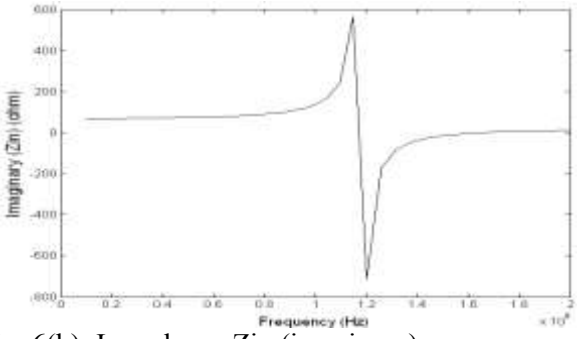


Fig. 6(b): Impedance Zin (imaginary)

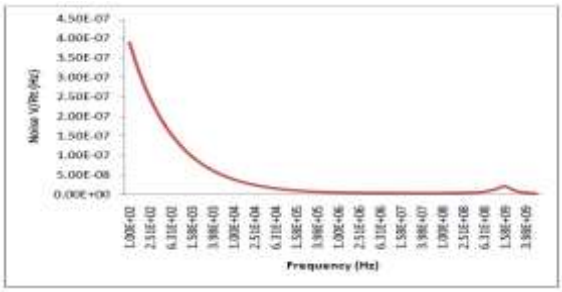


Fig. 7: Noise performance at 0.25v 1Hz noise signals at input port

However, the analysis of circuit sensitivity has been done with noise, change in temperature, and change in supply. Low power dissipation is achieved by reducing the number of transistors. Figure 7 indicates the noise performace of the design when 0.25v 1Hz noise signal has been applied at the input port. And the output noise performance is 10.97sqV/Hz. The supply consumes an average power of approximately 11.88mW. Additionally, the circuit exhibits a temperature sensitivity of approximately 2.5mV/°C, as illustrated in the Figure 8.

The simulation results illustrate that the circuit generates inductive impedance at one port through the use of the gyrator concept. This concept produces inductance (measured in nH) by utilizing MOS transconductance and junction capacitances. Additionally, the presence of FGMOS in the

feedback path allows for the adjustment of this inductance value within a specified range under specific design conditions (ranging from 3nH to 9nH). Furthermore, the circuit exhibits excellent sensitivity to factors such as temperature, noise, supply variations, and more.

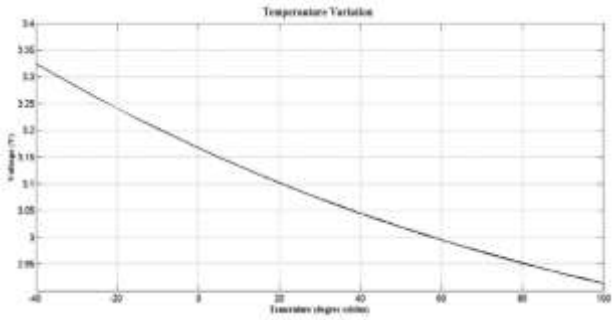


Fig. 8: Change in V_{fg} floating gate voltage with respect to change in temperature from -40ºC to 100ºC.

2.2 Fabricated Active Inductor and its Results

Inspired by the simulated results of the proposed active inductor design, we have created the circuit layout, which is depicted in Figure 9. This tunable AI CMOS circuit has been designed using Cadence Virtuoso. The layout displayed in Figure 9 includes connection points for input/output, and notably, for the floating gate node. However, as illustrated, instead of individual I/O connection points, the necessary pins have been linked to the outermost I/O pins of the complete pad frame. This connection has been achieved using three layers of metallization, and the floating node remains unconnected (i.e., no contact), enclosed on all sides by oxide.

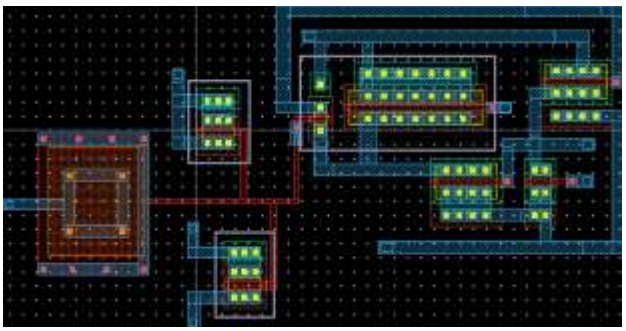


Fig. 9: Layout of the proposed circuit (The occupied chip area is 235×114 μm2)

To fabricate the PCB, Cadsoft Eagle PCB Design software was utilized in conjunction with an automated cutting tool. The PCB was meticulously crafted and polished using these tools. Images of the PCB are presented in Figure 10(a) and Figure 10(b)

Fig. 10(a): Back side of PCB with soldered IC, SMA connector, and connecting wires

Fig. 10 (b): Front side of PCB soldered IC, SMA connector, and connecting wires.

A Vector Network Analyzer as shown is Figure 11 is employed for the measurement of various components, devices, circuits, and sub-assemblies. These analyzers include both a signal source and multiple receivers, typically displaying amplitude and phase information in terms of ratios while performing frequency or power sweeps. It's important to note that a network analyzer continuously examines a known signal in terms of frequency since it functions as a stimulus-response system.

Fig. 11: Active Inductor device testing set-up using Vector Network Analyzer

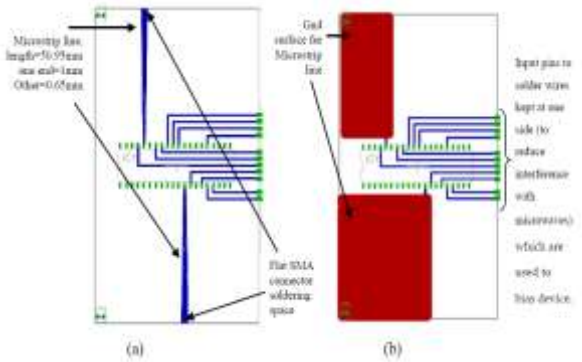


Fig. 12: PCB design final mask provided to automatic PCB designing machine (a) back side where IC pins and wires will be soldered (b) back side where red surface (Cu)

Following the initial level of significant progress, the printed circuit board (PCB) for AI devices was meticulously crafted using the Cadsoft Eagle PCB Design software and precision-cut using automated cutting tools. The final design is presented in Figure 12.

(a) The I/O pads have been protected from ESD, however, the ESD protection from terminals of FGPMOS where high-value voltages need to be provided has been removed. The design is also protected from leakages using double guard rings. The layout of the tunable active inductor, which consists of an FGPMOS feedback resistor, occupies a chip area equal to 235×114 µm2. However active inductor layout consists of a PMOS feedback resistor occupying 131×88 µm2 of chip area. With the help of Vector Network Analyzer, testing of fabricated Active Inductor has been done and S11 has been observed by measuring the magnitude and phase of the incident or reflected voltage signals as the design is one port. After the fabrication of the device, the device has been tested using VNA.

(b) **Smith Chart of Reflection Parameter S11:** The reflection parameter S11 has been observed to measure impedance at one port of the design. The input signal of 800MHz, Vin=1v, has been transmitted at the port, and the reflection coefficient has been observed on VNA. However, Figure 13 illustrates the Smith chart of S11, which shows that at the one port active inductor device, inductive impedance is present whose value is about 7.074nH.

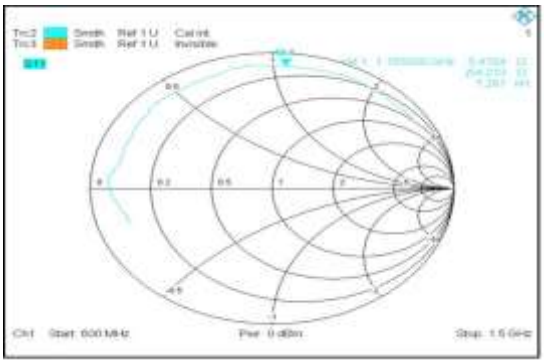


Fig. 13: Smith Chart of reflection parameter S11in Tunable AI using tunable FGPMOS feedback resistor

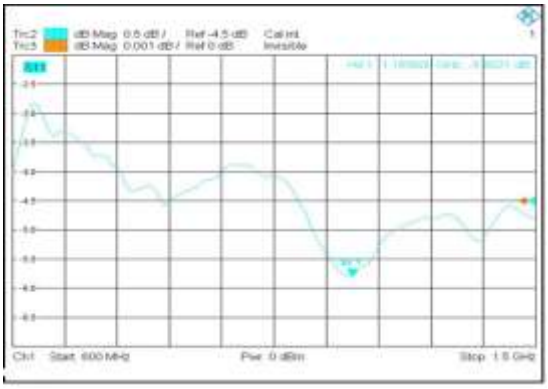


Fig. 14: Frequency response of S11 parameters S11in Tunable AI using tunable FGPMOS feedback resistor.

S11/S21 parameters; As shown in Figure 14 the dip at 1.183 MHz hence the resonance frequency or central frequency is 1.183 MHz (similar to non-tuned AI). For on-chip tunneling the charge from floating-gate, tunneling voltage, V_{tun} is increased from 8v to 10v and then 11v, and then after two successive tunneling, the active inductor S11/S21 parameter has been measured, as shown in Figure 15. The change in resonant frequency from 1.18GHz has now become 856MHz and during the injection, the charge is injected into the floating gate using high potential between the drain and source of programmer PMOS (indirect injection to the floating gate). Thus, to perform the injection, drain voltage of programmer PMOS, V_{dprog} value is increased from -0.5v to -1v, and then after injection again S11/S21 parameters have been measured. Now the resultant self-oscillator frequency becomes 1.194GHz as shown in Figure 16.

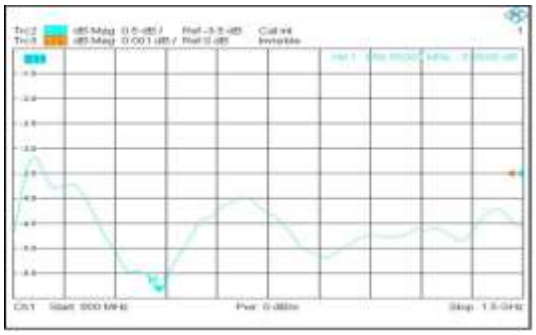


Fig. 15: Frequency response of S11 parameters, in which self-oscillating frequency (i.e. dip in reflections) due to tunneling

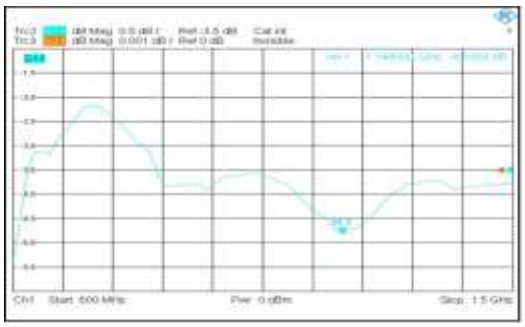


Fig. 16: Frequency response of S11 parameters, in which self-oscillating frequency (i.e. dip in reflections) due to injection

3 Applications of Proposed AI in RFICs and MMICs

The simulation findings for the suggested design of a tunable RF active inductor validate that the compact single-port AI design is capable of generating inductance at the designated port. This inductance can be fine-tuned by adjusting the charge on the floating gate of the FGPMOS feedback resistor through tunneling and injection processes as shown in Figure 17. The simulation result of two parameters such as the Quality Factor and the tuning of the central frequency of the bandpass filter has been shown in Figure 18(a) and Figure 18(b).

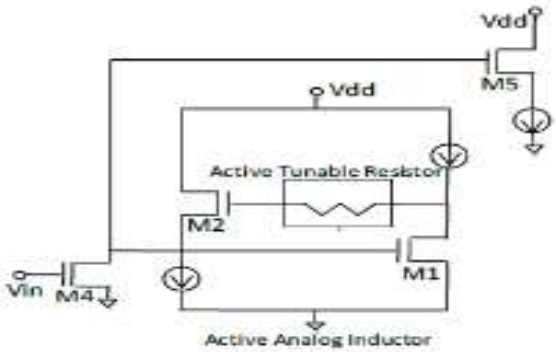


Fig. 17: Circuit diagram of Tunable Bandpass filter simulated on T-Spice using 0.35um CMOS process, which includes our proposed tunable AI design.

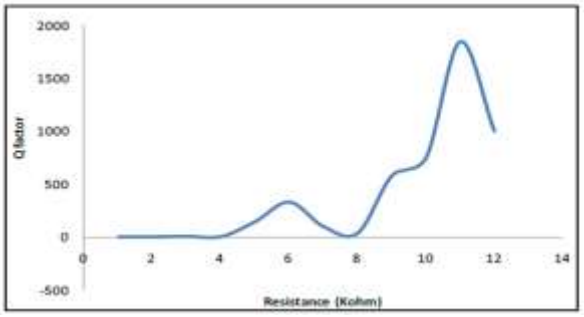


Fig. 18(a) Tuning of the Q factor of bandpass filter

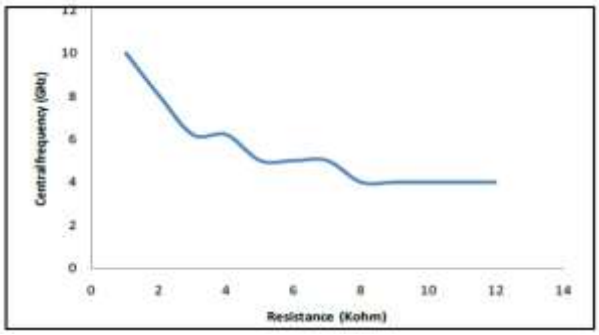
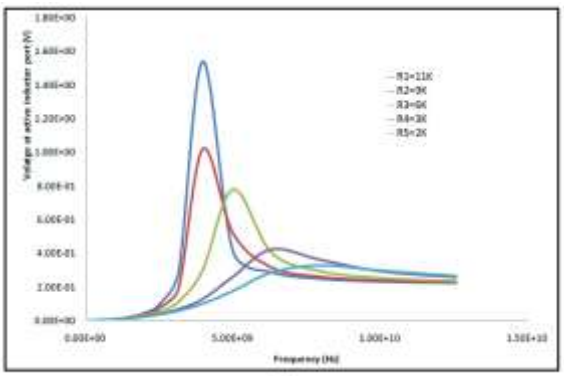


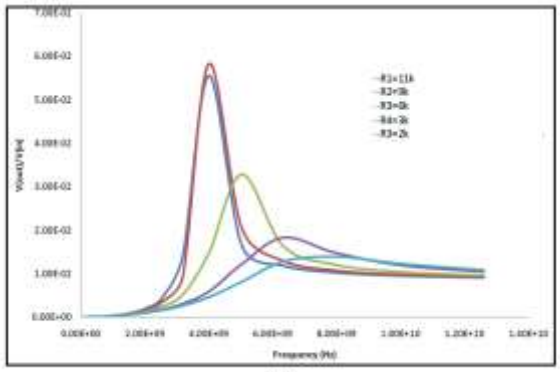
Fig. 18(b) Tuning of the central frequency of bandpass filter, with tuning of resistance across FGPMOS from 2K to 11K

The various resistance values by using the FGMOS resistor are shown in Figure 18(a) and 18(b) and the tuning of resistor can be from 2K to 11K. The variation in voltage and frequency response by using tunable FGMOS resistance is shown in Figure 19(a) and Figure 19(b) respectively.



(a)

Fig. 19(a): Tunable AI with tunable FGPMOS resistance from 2K to 11K



(b)

Fig. 19(b): Tunable Bandpass frequency response with tunable FGPMOS resistance from 2K to 11K.

4 Future Scope of Proposed Active Inductor

An active inductor has various applications in RFICs (Radio-Frequency Integrated Circuits) and MMICs (Monolithic Microwave Integrated Circuits) due to its ability to provide controllable inductance and improve the performance of RF and microwave circuits. Active inductors can be used in the input-matching network of LNAs to provide impedance matching and gain control. VCOs are essential in frequency synthesizers and local oscillators. Active inductors allow for precise frequency tuning and stability. The ability to vary inductance helps in wideband or agile frequency synthesis. Active inductors can be used in the matching networks of mixers to achieve high conversion gain, linearity, and image rejection. Tunable inductors enable frequency-agile mixer designs. Active inductors can be incorporated into RF and microwave filter designs to control center frequencies and bandwidths. PLLs are widely used in communication systems. Active inductors help optimize loop bandwidth and phase noise in PLLs, contributing to improved frequency synthesis performance. Active inductors are employed in VGAs to adjust the gain levels in RF systems. Tunable active inductors enable dynamic gain control. In RF and microwave circuits, impedance matching is critical for efficient power transfer. Active inductors can be used in matching networks to achieve impedance transformation and adapt to changing load conditions. Active inductors can be utilized in the output-matching network of PAs to maximize power transfer and efficiency. Tunable active inductors help optimize PA performance over different frequency bands. Active inductors play a role in frequency multiplication and division circuits, where precise control of harmonics and subharmonics is required. In phased-array antenna systems, active inductors help control the phase and impedance of individual antenna elements, enabling beamforming and steering. Active inductors are integral to the transceiver architecture, where they contribute to the performance of both the receiver and the transmitter. Active inductors are used in SDRs for frequency agility and adaptability across multiple frequency bands. Active inductors are essential in high-frequency applications, including millimeter-wave and terahertz circuits, where they contribute to signal processing and generation. Active inductors are crucial in the development of 5G and beyond-5G communication systems, which require agile frequency tuning and advanced RF front-end designs. Active inductors are used in RFICs and MMICs for space and satellite communication systems, where reliability, efficiency, and frequency flexibility are essential.

The areas of interest where AI plays a vital role are listed below:

Receiver front-end modules (T/R switch, amplifiers, variable gain amplifiers, LNAs, mixers, filters, and demodulators)

- Low-power transceiver circuits like battery-less circuits, wake-up circuits, RFIDs, wireless circuits for low-power operation, and near-field communication systems.
- Voltage control oscillators and frequency synthesizers, frequency dividers, and phase lock loops.
- Mm-wave communication circuits and SoCs.
- Integrated radars
- RF and millimeter-wave system applications.
- Galvanically isolated power transfer circuits are used for RF coupling.

4.1 Low Noise Amplifier

In this day and age, the low-power RF transceiver has become a desirable demand in medical, scientific, and industrial operating bands. Because of the development in wireless technology, the performance of RF receiver is very important and low noise amplifier is the first stage in an RF receiver circuit. Several system requirements such as low power consumption, high gain, input and output impedance matching, noise, and low noise figures need to be fulfilled. There have been several works presented for LNA. The very simple technique that was used in earlier days was the forward bias technique as shown in Figure 20. The major advantage of using this technique is that it has a low power consumption of LNA. The topology was implemented at 180nm technology and has a noise figure of 2.88dB, a gain of 10.1dB, and a power consumption of 0.84 mW.

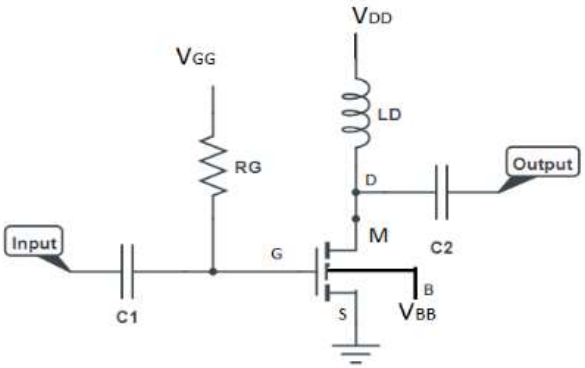


Fig. 20: Schematic of LNA with a forward body bias technique, [15]

Another method that can be used to minimize the power is MOS biasing in a weak inversion zone so that the value of g_m/I_d will be high. With the self-biasing technique the power dissipation of 60µW at 0.4 volts power supply, NF of 5.3dB, and the gain of 13.1 dB. Common source cascade is the most general circuit technique for LNA circuits. The spiral inductor is replaced by CMOS-based AI so that the total chip area can be minimized. Active inductor-based filters that can be effectively used for LTE/WLAN is one of the major application of inductors in the upcoming technologies as depicted in, [17]. Figure 21 shows the low noise amplifier circuit with AI which can be used to have all the selective frequency ranges.

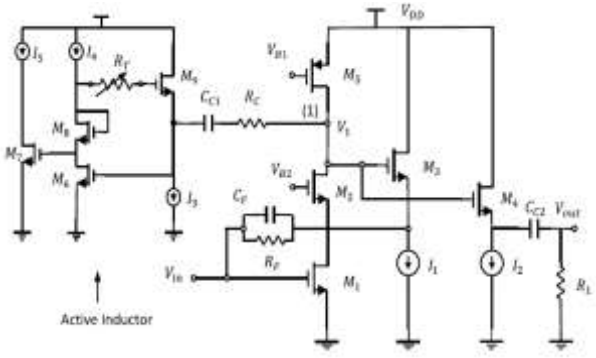


Fig. 21: AI-based LNA circuit

Because of the merits of low noise figures, better linearity, high gain, and good I/O matching, circuits with inductive feedback have been widely used in the wireless transceiver system. In LNA with source inductance negative feedback, the gain, NF, and the impedance matching of the LNA could be optimized, [18]. In recent times, the LNA has been designed for multiband wireless applications, where AI has been used to check the characteristics at lower technology and the phase shifting property that can be used in shifters is indicated in, [19]. The circuit also inculde the capacitor creating a feedforward path which increases the signal to the output node so that BW can be increased. The design is fabricated at 65-nm technology and the negative capacitance has been utilized to compensate the parasitic capacitance. The design presented a gain of 26.7dB and a BW of 4.1GHz.

4.2 Recent Advancements in LNA Architecture

The non-linear parameters of LNA are enhanced by various techniques like feed forward, derivative superposition, and modified derivative superposition. In recent designs, the current reuse technique is one of the popular techniques to improve performance such as low power consumption, low NF, and high power gain. Various types of AI are used to design the circuits such as Wu folded compact (WFC) and CFR AI. Figure 22, [20], shown below is the circuit of LNA-PDAI (Low noise amplifier- Partially degenerated Active Inductor) in which all the inductors are replaced by on-chip inductors, and the one-stage cascode LNA with PDAI has better gain and better linearity with a moderate bandwidth at the cost of power consumption because of increase if intermediate stages.

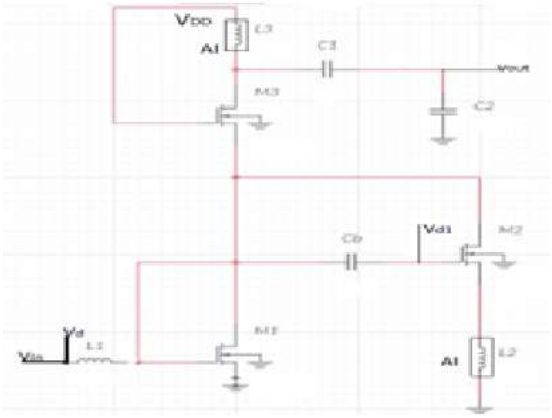


Fig. 22: LNA-PDAI

L3 in the above diagram is replaced by WFC-AI to improve the quality factor. L2 can be replaced by the Active Inductor using FGMOS circuit, [21].

4.3 Tuning Of Active Inductor in MMIC

The current reuse technique is the most popular choice for the designing of ultra-low power LNAs. Transistors M1 and M2, [22], are moderately biased to have low power consumption. Transistor M3 is used in common source configuration and acts as a shunt feedback, used to tune the characteristics of the design, [23]. The tuning has been done to analyze the characteristics like input impedance matching, gain, noise figure, and the linearity of the LNA.

Because of the need for filters in the communication system, the LC inductors can be designed using AI, for this gyrator-based AI is most commonly used. A method has been proposed in, [24], to synthesize the AI to have the transfer function for a two-port network which was successfully implemented to design the flexible low-power active LC filters and a single-ended tunable active inductor (TAI) employing two basic trans conductors. To enhance the quality factor, a feedback resistance is incorporated. Meanwhile, a network of capacitance is utilized to achieve the desired inductance value's tuning range. To generate the frequency of oscillations, the LC oscillators have been designed using the gyrator-C-based AI as described in, [25]. The tuning has been done by controlling the gate voltage of the MOS transistors. By varying this voltage from 0.8 volts to 1.6 volts, the frequency range from 86MHz to 1.137 GHz has been obtained. In any design, tuning of inductance can be done in many ways and the design that can be used as a resistance and capacitance is given by, [26], [27]. But the most common techniques are first by varying the value of control voltage or gate voltage so that the feedback resistance can be controlled, second by controlling the variation of the transconductance by regulating the current source, and third by using the floating gate transistors so that the inductance value can be stored and can be varied, [28]. A tunable floating active inductor using an improved grounded active inductor has been shown in, [29]. In the design multi regulated cascade stage has been used to design the active inductor to reduce the parasitic series resistance so that the Q factor can be increased. The main advantage of the design is free of substrate effect which is beneficial in sub-micron technology. The Q factor and the inductance value are tuned by varactor capacitance and bias current. The design has been implemented at 180nm CMOS technology having the Q factor from 10 to 567 with the inductance value of 6 to 284 nH. The method for finely tuning inductance takes advantage of the concept of altering the number of metal plates in an inductor's patterned ground shield (PGS) that are connected to the ground, thereby modifying its magnetic fields. This innovative technique is described in, [28]. The significant aspect of this approach is that it preserves the original geometry and physical shape of the inductor as specified in the process design kit (PDK), even during the inductance tuning process. The control over the number of metal shields connected to the ground is achieved through an electronic circuit, comprising analog-to-digital converters and active switches, as detailed in, [30].

The tuning range of a tunable active inductor is limited. While it can cover a broad frequency range, there are practical limits to how wide the tuning range can be, which may not meet the requirements of all applications. Inductance value tuning is not linear and noise sensitivity has not been analyzed. Non-ideal behavior can limit their usefulness in certain applications, especially those requiring high linearity or low noise. The quality factor (Q) of the proposed TAI is not as high as that of some passive inductors, limiting their use in certain applications requiring very low losses. In tightly integrated circuits, electromagnetic interference (EMI) and crosstalk between components can be a challenge, potentially affecting the performance of tunable active inductor circuits.

5 Conclusion

This paper introduces a novel on-chip tunable RF Active Inductor design based on a gyrator, capable of operating at high frequencies with a central frequency of 1.2GHz. The design demonstrates the ability of the compact single-port AI configuration to generate inductance values in the range of 3nH to 9nH. What sets this circuit apart is its capacity to fine-tune the inductance value through charge tunneling and injection into the floating gate of the FGPMOS feedback resistor, using on-chip external voltages.

The design was simulated using the Cadence Virtuoso tool, fabricated through ON Semiconductor, and characterized using a Vector Network Analyzer. It finds applications in navigation L-band and mobile communication. Additionally, the simulation model of the proposed tunable AI was used to create a Bandpass Filter, which was then simulated on a 0.35μm CMOS process using T-spice. This Bandpass Filter offers tunable bandwidth, ranging from 3.5GHz to 10GHz, utilizing the tunable active inductor, and its central frequency and quality factor can be programmed. Further optimization can be explored to predict the tuning range accurately. The paper also underscores the promising applications of the proposed AI design in RFIC and MMIC circuits, such as Low Noise Amplifiers.

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Contribution of Individual Authors to the Creation of a Scientific Article

- Ms. Rajni Prashar carried out the simulation of the design under the supervision of Dr. Garima.
- Dr. Garima Kapur carried out the fabrication process and the post-fabrication testing.

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Conflict of Interest

The authors have no conflicts of interest to declare.