Medium-Voltage Drives (MVD) - Performance Analysis of Seven-Level Cascaded H-Bridge Multilevel Driver

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Abstract: - The drawbacks of traditional inverters, particularly in high-power applications and medium voltage, have been highlighted in previous investigations. Due to the cascaded H-bridge multilevel driver (CHBMD) harmonic characteristics improved and power enhanced, inverters with multiple levels are increasingly popular for high-power applications. The scientific literature has documented works on multilevel inverter topologies, control strategies, and applications. Additionally, no conclusive results investigate or rate a three-phase multilevel inverter's effectiveness. The present investigation evaluates the performance of a multi-carrier sinusoidal pulse width modification (MCS-PWM) based, Seven-Level cascaded H-bridge multilevel driver (7LCHBMD). Performance assessments develop based on the outcomes of a modeling experiment on the CHBMD functionality utilizing MATLAB. The characteristics of the results chosen to perform the task were the harmonic range, waveform arrangement, and essential significance reducing the THD output of the 7LCHBMD. The MCS-PWM technique procedure from the perspective of the voltage line had been determined according to the findings of the simulation investigation and analysis carried out for the 7LCHBMD utilizing the PD-PWM as the control framework.

1 Introduction

Many Medium voltage drivers (MVD) applications need a unique control way to minimize the harmonic on the output side for the high-power motors. In reality, the big conditioning systems require more efficiency and high power characteristics from motor drivers. To understand the multilevel motor drivers, it is crucial to study the half-bridge cell`s most straightforward architecture to generate a level of square-wave output. In such an arrangement, a voltage source is required, [1]. On the other hand, multi-level output waveforms are synthesized using the full-bridge architecture. Traditional motor drivers can deal with high-power applications, but they have significant restrictions. The converter's power electronics are linked in serial with utilizing transformers, causing issues like high gloss and cost to the total arrangement, [2]. Additionally, the high-frequency operation of traditional inverters has several drawbacks, mainly brought on by switching losses and device rating restrictions. Due to the dynamic voltage balancing circuit, there are additional problems with the complicated construction, [3].

As a result, multilevel motor drivers are becoming an alternative for medium voltage and high-power implementation. These converters have unique circuit architecture, allowing them to generate high voltage and decrease harmonics, [4]. Numerous high-power and medium voltage (MV) industrial applications use multilevel motor drivers, including motor systems, static VAR compensators (SVC), and AC power supplies. The staircase output waveform is created by combining multiple levels of DC voltages to get the AC output terminal voltage. The switches' voltage decreases load while enabling greater output voltage, [5]. Reduced switching losses in high-power applications are now possible using multilevel inverters, which are also an efficient and workable option, [6].

Additionally, the synthesized output includes more processes as the DC side voltage levels increase, resulting in an output closest to the sinusoidal wave with minor distortion due to harmonics. As a result, the need for an output filter has been decreased, [7].

The proposed methodology of our work uses the latest literature review scanning and simulation

results. CHBMD systems have been around for more than 25 years, according to a patent search, [8]. A recent study introduced the neutral point clamped converter architecture, and the development of multilayer inverters officially began, [9]. This topology's three-level output voltage waveform exhibits much higher spectrum performance than a traditional inverter. In, [9], the authors used many levels to improve the spectral structure of the output waveforms. The multilayer motor drivers enhance waveform quality and significantly lessen the devices' voltage stress, [10]. The inverters refer to as diode-clamped multilevel motor drivers. The needed voltage capacity of the clamping diodes changes in a multilevel motor driver. Meynard's flying capacitor multilevel inverter is an alternative. In this inverter layout, clamping capacitors use to limit the voltage across an open switch rather than clamping diodes, [11]. The CHBMD is a more straightforward multilevel inverter architecture with fewer power device requirements than the abovementioned ones. This topology's fundamental flaw is that each step needs an independent DC power supply, making it usable in applications using renewable or alternative sources that provide DC voltage output. Much literature has reported using three-phase CHBMD in driving and static applications, [12]. CHB MLI is gaining popularity in renewable industries due to its straightforward control, sustainability for high-voltage handling MV, higher fault tolerance due to its modularity structure, and freedom from capacitor challenges, [13]. In, [14], switch all CHB power cells during the basic cycle, resulting in equal power distribution across all cells and increased switching loss. PSPWM harmonics develop at multiples of N × switching frequency (where N = the number of CHB power cells) due to multı level controlling carriers.

The present study addresses some of the characteristics of CHBMD that are recognized according to several performance standards. The CHBMD performance has been thoroughly investigated, based on the outcomes of the simulation. The CHBMD circuit architecture and the various MCS-PWM approaches were discussed. Before outlining the critical components of the CHBMD as the paper's conclusion, the simulation findings are provided with analyzing of minimalized the output THD by using different variants of the control system. This study will provide a guide for designers and user of MVD to select the correct controlling variants, which will make the system works with higher efficiency and fewer harmonics.

2 Configuration of 3-Phase CHBMD

The output of three identical power cells per phase for 7LCHBMD structures can be connected with a wye or a delta arrangement from the input grid using phase-shift multi-secondary transformers. The arrangement representation of 7LCHBMD with separate DC sources is shown in Figure 1. Every power cell uses four switches, so twelve switches per phase are required for the 7LCHBMD structure, [13]. For the 7LCHBMD circuit arrangement, nine H-bridge cells, including 36 power switches, will be needed. Implies that twelve pairs of gating signals per phase must be produced to feed the switches. High- and two low-frequencies controlling different switches are created for each H-bridge cell by designing the switching such that only two switches function simultaneously with the same frequency and the other two do not operate, [14]. According to Figure 1, V_{AN} is phase A's voltage, which is calculated by adding V_{AHB1}, V_{AHB2},... $V_{A(HBn-1)}$ and V_{ABn}. Phases B and C have the same concept.
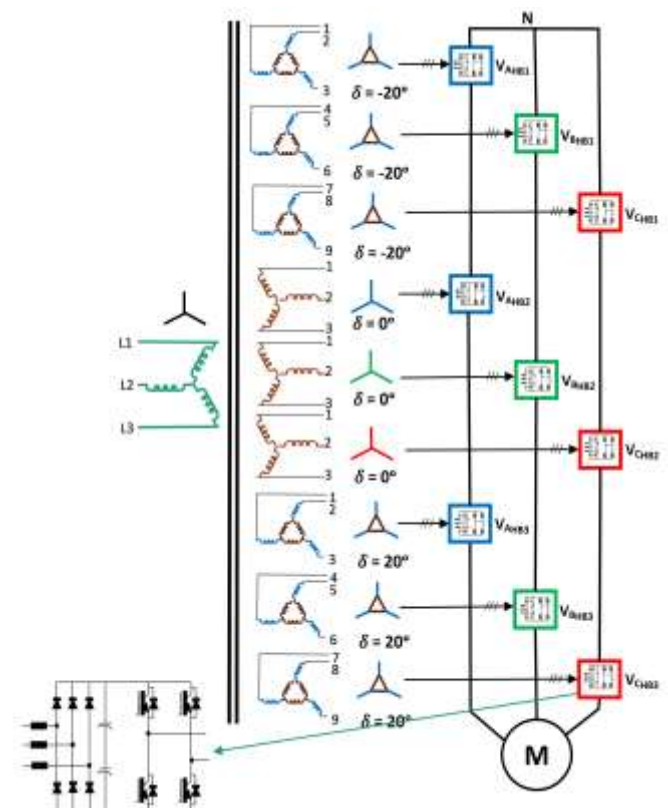

Fig. 1: A typical CHBMD arrangement.

The two-phase voltages are used to represent the line voltages. For instance, the potential V_{AB} between phases A and B may be calculated using equation (1).

$$V_{AB} = V_{AN} - V_{BN} \qquad (1)$$

As the V_{AB} refers to the voltage between A and B phases. V_{AN} is the voltage between line A and N neutral point. The V_{BN} refers to the voltage between line B and N neutral point, [15].

3 Multi Carrier Sinusoidal - PWM (MCS-PWM)

3.1 Fundamental Concept

The fundamental idea of MCS-PWM is to combine multiple triangular carrier signals with a single signal modulation for each phase controlling. (m – 1) A triangular wave with the fc frequency and sine wave are positioned for an m-level converter so that their frequency bands are adjacent. The carrier set's zero reference is placed in the center. The modulated signal has a sinusoidal waveform with amplitude Am and frequency fm. Each control signal is constantly compared to the modification signal. The electronic switch turns on if the control signal is stronger than the triangle wave allocated to that level for each comparison. If not, the electronic device turns off, [1]. Four carrier waveforms are required for a three-phase, 7LCHBMD, and each one must be matched to a set of requested waveforms that are separated by 1200 cycles, [5]. The MCS-PWM method for a 3-phase, 7LCHBMD is shown in Figure 2.
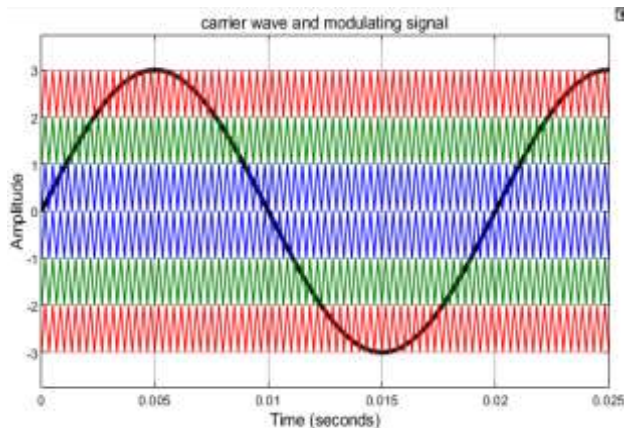

Fig. 2: MCS-PWM method of CHBMD

The MCS-PWM method requires three fundamental variables, including the ma modulation index specified in equation (2).

$$m_a = \frac{A_m}{N\,A_c} \qquad (2)$$

$$m_a = \frac{(m-1)}{2} \qquad (3)$$

As the multilevel inverter's (odd) level number is, m. A_m is the modulating signal's amplitude. A_c is the carrier (triangular) signal's peak-to-peak rate. The definition of the index frequency of modulation (m_f) is specified in equation (4).

$$m_f = \frac{f_c}{f_m} \qquad (4)$$

Where f_c is the carrier signal's frequency, and F_m is the modulated signal's frequency. The third variable is the variation in the angle between the signal of modulating and the positive side of triangle wave signals. A zero value of the angle is used in the current investigation.

3.2 The Implementation of Classifications and Disposition

The MCS-PWM approach may generally classify into three types of methods: Phase Shifted (PS), Carrier Disposition (CD), and Hybrid (H), [7], as shown in Figure A (Appendix). PSPWM modulation controls N CHB modules using "N" carrier signals. For multilayer operation, carrier signals are phase-shifted 180/N. Figure A(a) (Appendix) shows the 7LCHBMD configuration's phase-shifted signals. During each switching cycle, all operational components change the output voltage. The PS-PWM approach has the highest switching losses. Thus, the output voltage waveform contains the most pronounced switching frequency harmonic components at 2 × N × fs (where fs is the switching frequency and N is the number of operational HB modules). LSPWM modulation regulates "2N" carrier-signal CHB modules. Carrier signals are uniformly vertically displaced. Six carrier signals provide 7LCHBMD output voltage. Figure A(b) (Appendix) and Figure A(c) (Appendix) illustrates carrier signal magnitudes between 1 and 2/3, 2/3 and 1/3, 1/3 and 0, 0 and −1/3, −1/3 and −2/3 and −1. In each switching cycle, one CHB module flips, but the connected modules do not change the output voltage. Switching losses have lowered. Switching modules during fundamental cycle segments unevenly distributes power across operating modules. Depending on modulation index amplitude, the bottom module gives the greatest power to the output, while the top module (controlled by carrier signals between 1 and 2/3 and −2/3 and −1) contributes the least. When using the CD technique, the ref waveform is observed via a series of carrier waves that have been phase-shifted by successive increases in the source waveform's strength. H technique, on the other hand, combines

these two approaches. The gating signals for the CHBMD switches will be obtained in this study using the CD approach. Alternative wave disposal schemes, like Alternative Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD), and Phase Disposal (PD), are possible with the CD approach. For the PD scheme, every carrier signal is s seen in Figure 2. Carrier signals in the POD scheme are in phase when they are above the reference zero value. Although the waveforms carrier zero are 1800 cycles evacuated compared to those above zero, they are still in phase. Contrarily, the APOD method requires that each carrier signal be phase-shifted 1800 cycles back and forth from its neighboring carrier, [6]. Despite the alternative wave carrier disposition used for the three-phase CHBMD in this study, this article focuses primarily on the PD scheme's findings compared to those of other techniques and the traditional SPWM-based three-phase converter.

4 Findings and Evaluation

Utilizing MATLAB/Simulink, the three-phase 7LCHBMD is simulated. In the simulation research, each module's DC input voltage equals 400 volts, frequency output equals 50 Hz, and the CHBMD driver's load is an induction motor. The MCS-PWM method (PD scheme), findings, analysis, and comparison were completed.

4.1 Line Voltage Waveforms Affected by m_f

The line output voltage waveforms of CHBMD by the PD controlling, which uses values ma = 0.75, mf = 37, is shown in Figure 3.
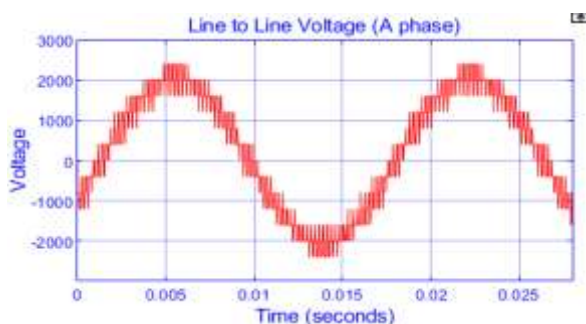

Fig. 3: The line output voltage of CHBMD with PD strategy (ma=0.75, mf=37)

The line output voltage waveforms of CHBMD by the PD controlling, which uses values ma = 0.75, mf = 60, is shown in Figure 4.
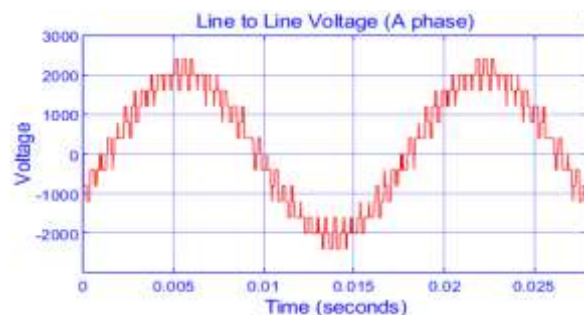

Fig. 4: The line output voltage of CHBMD with PD strategy (ma=0.75, mf=60)

It is noticeable from the results that, no matter if the mf value is even or odd, the output voltage using the PD controlling strategy is unsymmetrical. More switching will appear in the waveforms when mf is raised, but ma stays the same. Since f_c grows as mf increases, so does f_c since f_m is a constant frequency. Consequently, the modulating and carrier signals will often cross.

4.2 The Relation between Driver Level and m_a Value

The line output voltage waveforms of CHBMD using the PD arrangement, with m_f maintained at 37 and changing m_a,. The line voltage can produce a maximum of 9 levels. Predominately, it can determine the maximum level number that could be achieved in the line output voltage waveform is 4s + 1, taking into account the DC supply source for every phase where s = 2 for the 7-level CHBMD. The values list of CHBMD using the PD technique (mf= 37) attained is presented in Table 1.

Table 1. Values list of CHBMD using PD technique (mf= 37) attained.

m_a	Number of levels
≥ 0.95	11
0.8 – 0.9	9
0.6 – 0.8	7
0.3 – 0.5	5
< 0.3	3

4.3 Analysis of Harmonics in Line Voltage

The output voltages harmonic spectra CHBMD using the PD technique are shown in Figure 5 and Figure 6, which show that only an odd number of frequencies exist for an odd number of mf, but both odd and even frequencies are found for even mf. It is discovered that this property is comparable to a single-phase CHBMD. Figure 5 and Figure 6 do not show any critical frequencies [8]. Instead, only the recurrence of the first significant harmonic (29 for mf = 39 and 50 for mf = 60) is shown to be identical to that of a 3-phase 7-level CHBMD. However, with

m_f set at 37, it is discovered that as ma increases, the size of the harmonics decreases, with the highest harmonic accounting for just 5.1% of the fundamental component.
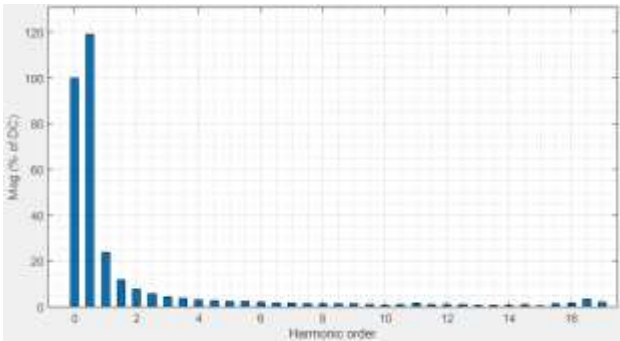

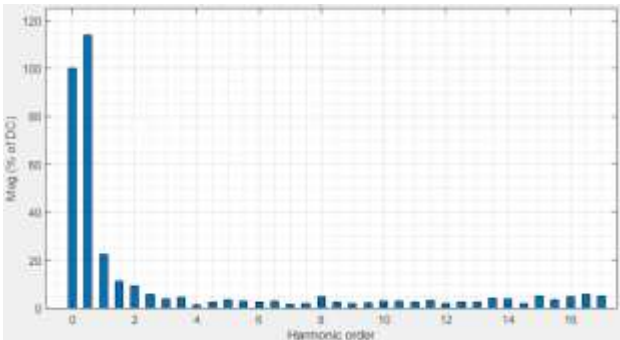Fig. 5: The line output voltage of CHBMD with PD strategy (ma=0.9, mf=37)

Fig. 56: The line output voltage of CHBMD with PD strategy (ma=0.2, mf=37)

The line output voltage harmonic spectra for the 7LCHBMD using the PD strategy and mf different values. The data show an equivalent harmonic arrangement, showing that preserving an odd number and triple mf match with adding mf has no discernible advantages. As a result, if mf is selected to be an odd number and triplen, the ordinary three-phase SPWM converter does not produce any triplen harmonics in the line's voltage, [9].

4.4 m_a and   Output Voltage   Crucial Interaction

The output voltage essential of 7LCHBMD using a PD carrier placement scheme inverter is shown in Figure 7. The CHBMD output voltage fundamental is much greater than the traditional inverter with a comparable DC voltage input, making the latter more appealing for applications requiring significant power. The output voltage does not rise proportionately with ma when ma surpasses 1 (over-modulation). The three-phase CHBMD line voltage THD for the PD, APOD, and POD carrier deployment schemes are shown in Figure 7. According to the findings, when contrasted with

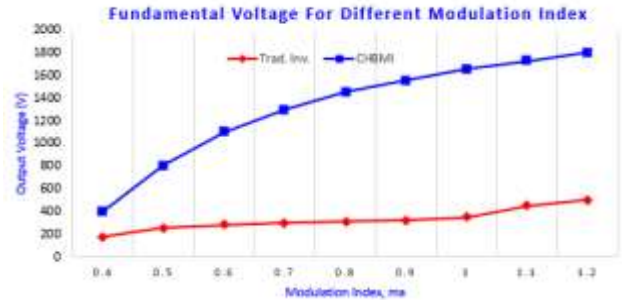APOD and POD, the PD technique delivers the lowest line voltage THD.

Fig. 7: Evaluation of the principal voltage output

4.5   The Line Voltage's THD

It entails the cancellation of harmonic in the line voltage that was previously discussed. The THD of output voltage for different control strategies is shown in Figure 8 for different amounts of ma. The graphic illustrates the inverse relationship between ma and the THD of the line and phase voltage for the CHBMD. Additionally, it is shown that, as predicted, the THD of line voltage is much smaller than the phase voltage THD for a given ma value.
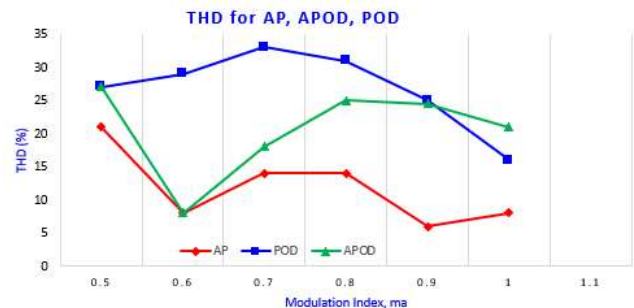

Fig. 8: THD of output voltage for different control strategies

The THD of output voltage performance for CHBMD using PD strategy for different ma values is shown in Figure 9, which compares the performance in CHBMD of the PD scheme. The output voltage of 1108 V is compared while ma is held constant at 0.8. The DC input used for the CHBMD and traditional inverters is 400V and 1600V to produce the same fundamental output voltage. The THD effectiveness in CHBMD's line output voltage may be inferred from Figure 9 to be almost mf-independent. Because mf changes, the amplitude of the most notable harmonics stays constant, changing only the harmonic interval. Therefore, mf only significantly affects how well the inverters operate regarding THD.

Fig. 9: THD of output voltage performance for CHBMD using PD strategy for different ma values

5 Conclusion

The simulation analysis that was carried out allowed for identifying several different characteristics of the CHBMD using the PD controlling strategy in terms of the line voltage. Compared to the phase voltage, the line output voltage is capable of synthesizing a more significant number of levels, and as a result, it more closely resembles a sinusoidal waveform. In addition, the line voltage produces superior spectrum performance, eliminating the need for an output filter in most cases. The CHBMD can create output voltages with a higher fundamental but much lower THD. Based on the findings of the research, it is also possible to conclude that, in contrast to the traditional inverter, there is not a significant improvement in the harmonic performance that can be achieved by setting an odd number and triplen mf to a CHBMD. The PDPWM suggested modulation for the 7LCHBMD approach is implemented, operated, and compared to established methods. In modulation approaches, switching loss is equal in all semiconductor modules and lower than in other techniques. When the line output voltages are created, the PD scheme benefits three-phase applications because it cancels out the major carrier component between phase legs. This makes the system advantageous in these applications. When the modulation index is high, the PD modulation technique produces the THD in the line output voltage. In conclusion, the findings revealed that CHBMD is appropriate for operation at a high ma that does not exceed one. The higher the m_a means higher output voltage, greater levels number, and less critical harmonics. A larger m_f means guarantees a greater space between the component and the harmonic, which simplifies the filtering process.

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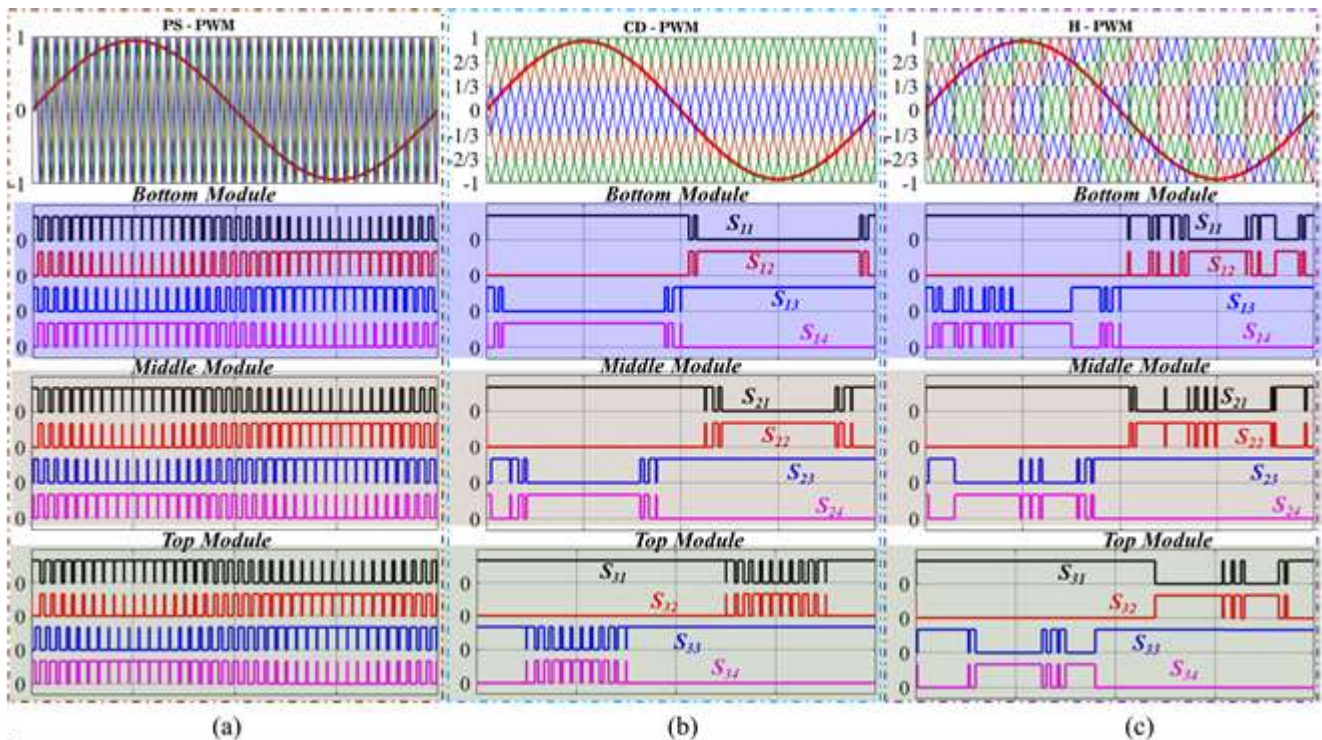
APPENDIX

Fig. A: MCS-PWM methods classify (a). Phase Shifted (PS), (b). Carrier Disposition (CD), (C). Hybrid (H)

Contribution of Individual Authors to which Creation of a Scientific Article (Ghostwriting Policy)
The authors equally contributed to the present research, at all stages from the formulation of the problem to the final findings and solution.

Conflict of Interest
The authors have no conflicts of interest to declare.