Phase Noise Reduction Technique for ISM Band LC Oscillator Using Tail Current

KRUTI THAKORE[1)], D. J. SHAH[2)], N. M. DEVASHRAYEE[3)]
Electronics and Communication Department[1, 2, 3)]
LDRP ITR, KSV University[1)], Sakalchand Patel University[2)], Nirma University[3)]
Gandhinagar[1)], Visnagar[2)], Ahmedabad[3)]
INDIA [1, 2, 3)]

Abstract: - This paper presents low phase noise, precise frequency tuning range LC Voltage controlled Oscillator (VCO) circuit of Phase lock loop, to support - IEEE 802.11a/b/g, Bluetooth, Zigbee and IEEE 802.15.4., operating on 2.4GHz ISM band (Industrial, Scientific, Medical). The presented circuit is implemented in Cadence virtuoso environment and using GPDK090 Library of 90nm CMOS Technology. The presented VCO is tuned at 2.4GHz frequency with tuning range of 80MHz. The measured Phase noise is -126.3dBc/Hz at 1MHz offset frequency. The total power consumption of the presented VCO is 4.7mw at 1V power supply.

Key-Words: - frequency tuning range, phase noise, Zigbee, IEEE802.15.4, ISM Band, FOM, VCO.

Received: April 1, 2021. Revised: September 2, 2021. Accepted: September 17, 2021. Published: September 29, 2021.

1 Introduction

The persistent work on unique wireless connectivity motivates the development of Voltage controlled oscillator for Phase lock loop. In today's era, very Intensive research work is done towards realizing efficient oscillators to improve the overall performance of the system.

Phase-locked loops (PLLs) are widely used in radio frequency and at RF front-end transceivers. Networks like transceivers with sensor-based network systems, home automation, automotive and medical solutions. The voltage Controlled oscillator is the key block of phase lock loop and must be very accurate to generate channel frequency in the range of 2400 – 2480 MHz for the wireless applications including ISM band to support - IEEE 802.11a/b/g, Bluetooth, Zigbee and IEEE 802.15.4., with minimum required bandwidth of 80MHz. Commonly, both ring oscillators and LC oscillators are used in GHz range applications. However, ring oscillators suffer from poor phase noise compared to that of LC oscillators and are less suitable for high-end wireless communication systems. LC oscillators are more attractive due to their better phase noise performance. They occupy larger area compared to that of ring oscillators, in case of on chip Tank circuit. LC VCO with off chip inductor and varactors occupies less area and consumes less power. The cross coupled MOSFET pair represents the one-port oscillator to provide a negative resistor to compensate for the energy loss in the LC tank in order to sustain the oscillation with the given frequency. As the on-chip inductor on CMOS process has very low-quality factor (Q), which increases the total power consumption of the circuit. Low quality factor (Q) also degrades phase-noise performance. As well On-chip inductor takes larger silicon area and LC-VCO provides narrower frequency tuning range. Phase noise is crucial parameter of LC oscillator. High phase noise of oscillator can degrade the performance of the system. As reduction in phase noise with power consumption at high frequency with required tuning range adds more challenges for the oscillator designers.

In the literature different techniques to reduce phase noise is proposed. Phase noise is generated in the oscillator due to thermal noise in the source transistor current, around the second harmonic of the oscillation and at second harmonic high impedance is required at the tail to stop switching FETs from loading the resonator [[13]]. Inductive and capacitive filtering techniques with top and tail biasing is proposed in [[13]] for phase noise reduction. Inductive degeneration technique is proposed in [[3]] with on chip and off chip LC filtering technique, which results in better phase noise. In paper [[4]], phase noise and figure of merit is improved with increasing Q of the inductor. The Quality factor is increased with multi-metal layer inductor, which reduces DC resistance and HRS reduces substrate effect at 5GHz tuned oscillator. In paper [[5]], LC tank is used with complementary

cross coupled negative resistance, which is tail biased with NMOS current mirror course. Symmetrical inductor and PMOS varactors in inversion mode are used for fine tuning and metal-metal capacitor array is used for additional coarse tuning for process variation changes, which is controlled by 3-bit signal. In [[6]] literature, the VCO modeling equations and Hajimiri's phase noise equations are modified to define Id current and MOS variable gm/Id is introduced for compromising working in different inversion regions. It is also shown that the working in weak and moderate inversion region results in low current and increases phase noise. In [[7]], LC-QVCO is presented with cascade switching biasing technique and source body resistor. The CSB technique reduces resonator loss generated by MOSFET resistance and source body resistors reduces noise contribution of substrate related to cross coupled MOSFETs. A new technique is introduced in [[8]], reduction of 1/f3 phase noise in LC oscillator by self – switched biasing. Reported phase noise is -122.8dBc/Hz at 1MHz, achieved by decoupling and coupling capacitors with switched biasing at tail current. In literature [[9]], a novel circuit of Lc oscillator with tail current noise of second harmonic filtering technique is proposed to reduce phase noise. The proposed filtering circuit works as low pass and band stop filter. But in this LC filtering technique area occupancy is high. The technique proposed in [[10]], phase noise reduction in LC oscillator using tail current shaping is achieved with two extra transistors with RC network. In [[11]], a 2.4GHz LC oscillator is proposed with tail current biasing and gate resistance matching techniques to reduce phase noise. A diode connected load with tail current source biasing is proposed to reduce phase noise in comparison with nMOS, pMOS and CMOS VCO. In [[12]], active inductor is used with phase noise reduction technique, which results in -117.2dBc/Hz at 1MHz offset. The two approaches reported in literature for modelling the phase noise are in frequency domain [[13]] known as Leeson's model and in time domain [[1]], [[2]] known as Hajimiri's model. According to Hajimiri's model, total phase noise generated in the oscillator is due to noise sources and tank losses, which is highly associated with oscillator topology [[14]]. Phase noise is reduced by reducing the value of Impulse sensitivity function (ISF), which is reduced by reducing the tail current value at the time when oscillator is more sensitive to noise. From the Hajimiri's model, phase noise is obtained by (1).

$$L(\Delta w)=10\log\left(\frac{\frac{in^2}{\Delta f}}{2qmax^2\Delta w^2}\Gamma rms^2\right) \quad (1)$$

It is reflected from the equation (1), that (Γrms) root means square-RMS value of the effective ISF is directly proportional to the value of phase noise. If the Γrms value is reduced by shaping the tail current, then phase noise can be reduced. If the tail current is made maximum at maxima and minima points of output, when sensitivity to noise is less and ISF is close to zero, as an effect phase noise can be reduced. Also considering the ISF effective, [[14]]

$$\Gamma eff(wot)=\Gamma(wot)\alpha(wot) \quad (2)$$

Where, $\alpha(wot)$ is noise modulation function (NMF) and it is approximately sinusoidal function. If the value of Γeff is reduced by making the tail current minimum at zero crossing points of output then phase noise is reduced because at these points' oscillator is more sensitive to injected noise onto tank circuit. Also, the thermal noise of switching transistors is modulated by α(wot), which depends on the total contribution of switching transistor and tail current waveforms [[10]]. In this paper the reduction in phase noise is made reduced by tail current shaping and tail biasing technique. Using Hajimiri's oscillator concept [[1]], [[15]], the conventional Oscillator is proposed and simulated in this paper, as shown in Figure 1. In this conventional LC oscillator tail current is applied through a single nMOS transistor, which is fixed biased at the gate terminal and drain is connected at the switching transistors of oscillator. In this conventional oscillator tail transistor designed to operate in saturation region and it behaves as current source to determine oscillation amplitude. Here, conventional oscillator is compared with the proposed LC oscillator with tail current technique to reduce phase noise. The LC oscillator topology selected here is nMOS oscillator, due to higher switching speed and a symmetrical output signal. Compared to complementary LC oscillator, nMOS LC oscillator is more stable to Vdd variations and interference noise [[9]].

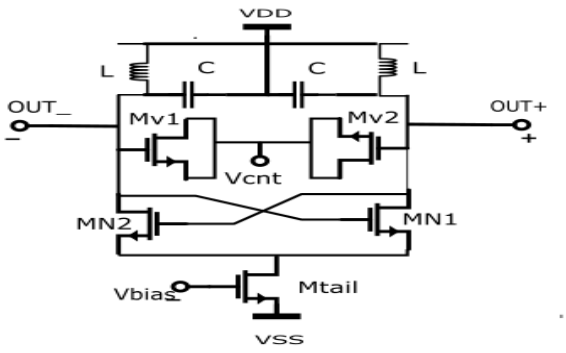


Fig. 1 Conventional nMOS LC oscillator

The tail transistor source in the conventional oscillator introduces thermal noise in the current source at the second harmonic of the oscillation, which can be removed by introducing high impedance and narrow band mechanism at the tail transistor. Moreover, it is possible by preventing the switching transistors in triode region from loading the resonator circuit at the second harmonic.

The techniques proposed in [[10], [15], [16]] are used to reduce phase noise by tail current shaping. In this technique, outputs of oscillator are connected to the gate of tail transistor through capacitor, which will make the tail current maximum at zero crossings and make small at maxima of oscillation output. This concept will reduce the sensitivity of phase noise into the oscillator and results in better phase noise. To reduce phase noise in the proposed oscillator circuit, the combination of these two techniques is used.

The rest of this paper is organized as follows. Section II describes the Proposed LC Voltage controlled oscillator. Section III describes simulation results of proposed LC voltage-controlled oscillator with analysis of operation and gives the comparison with conventional VCO and previous published papers. Section VI concludes the paper.

2 Voltage Controlled Oscillator

In the phase lock loop voltage Controlled oscillators are the essential component that has been used widely in transmitters and receivers, need to design with accuracy.

The schematic of proposed nMOS LC VCO is shown in below Figure 2. In this proposed technique an effort is made to improve the phase noise performance of the LC-VCO. In this circuit, compare to conventional nMOS LC oscillator four extra nMOS transistors are connected in between source node of switching transistors and ground node. Here, Mc1 and Mc2 transistors are used to improve the tail current in order to reduce phase noise. The gate terminals of both the transistors receive gate voltages from DC source as well from output node of oscillator, which include AC and DC part. As, Ac part of voltage comes from the output node of the oscillator through Cdc capacitor and DC part from the Vdc external DC source through Rdc resistor. The concept to apply DC source at the gate of the transistors, to achieve required loop gain to start the oscillation. As per oscillation theory, very small amount of DC current is required at the switching pair of oscillators, to generate continuous sine wave with positive feedback gain of the oscillator. The AC part of the gate voltage, coming from output node, is used to turn on and off the Mc transistors for tail current shaping. This will make the tail current minimum at the zero crossing points of the output voltage and at the peak points the tail current is made maximum. Now, Mb1 and Mb2 transistors are used to determine the oscillation amplitude as well behave as a current source. Both the gate terminals of the Mb transistors are connected with Vbias external DC source. These transistors are designed to operate in saturation region to provide tail current at the source node of switching transistors. The selected value of Vbias maintains the Mb transistors in saturation region and the selected value of Vdc is quit above the threshold value of the nMOS to turn on the transistor.

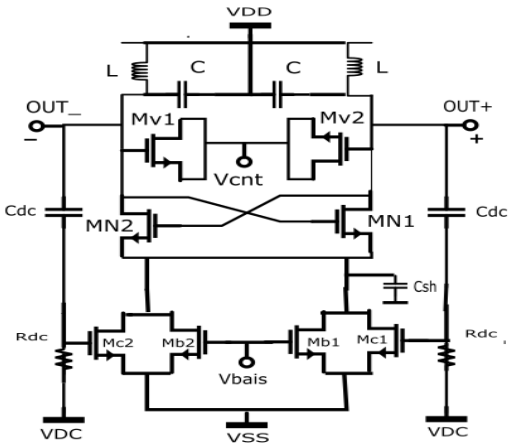


Fig. 2 Proposed LC oscillator

In this circuit, Both Mc and Mb transistors are connected through their drain and source terminals. At the zero-crossing point of the output, Mc transistor has very low gate voltage, which is from the Vdc source. This will make drain node voltage low and transistor will enter into triode region at this point. However, drain of the Mb transistor is connected with the drain of Mc transistor, the tail

current coming from Mb transistor will become low at this point. This will make tail current minimum at the zero crossing of output oscillation voltage. According to the output voltage, as increase in output voltage, gate voltage of Mc transistor is increased. This will increase the drain voltage and finally tail current from Mb transistor will increase. This results in maximum tail current at peak points of output oscillator voltage. So, shape of the tail current is made by Mc transistors according to output of oscillator voltage and tail current is applied by the Mb transistors. However, tail current is also one of the noise contributors in the LC oscillator, tail current is made small during zero crossing when the sensitivity of the output phase to injected noise is large. This will play role to reduce the phase noise of the LC oscillator.

The high value of Rc resistor is selected to stop noise and loss of the tank circuit. Here, Csh capacitor is used as capacitive filter to reduce phase noise of the oscillator at the second harmonic. In the second harmonic frequency, the sources of switching transistors are grounded by capacitor Csh. When transistors enter in triode region, tank loss is increased by low resistance drain – source path of transistors and it results in increased phase noise. The capacitive filtering offers large impedance at the source of switching transistors and offers better phase noise.

The size of the Mc transistor is selected such that to response the applied small gate voltage and drawing proper current from Mb transistor. As well, size of the Mb transistor is selected proper for tail current applied at the source node of switching transistors according to output voltage. The selection of the Vdc source value offers small current at the starting of oscillation and also controls Mb transistor drain current for proper tail current shaping.

The output of LC oscillator may be expressed as [1]

$$V_{out(t)} = A \cos (w_0 t + Ø) \quad (3)$$

Where, A is amplitude, w_0 is frequency and Ø is arbitrary. In the practical LC oscillator, output voltage is generally given by [1]

$$V_{out(t)} = A(t)\, f\, (w_0 t + Ø) \quad (4)$$

As, A(t) and Ø(t) are functions of time and f is periodic function. While designing the LC oscillator it is required to know effect of amplitude and phase noise separately. Amplitude noise can be eliminated by amplitude limiting circuit, which controls the output oscillation amplitude. Phase noise of the oscillator is reduced over here with techniques proposed.

3 Simulation Results

In this section, simulation results of proposed oscillator are shown. The simulation has been performed in Cadence virtuoso environment and using GPDK090 Library of 90nm CMOS Technology. In Figure 3, oscillation output voltage of proposed oscillator with tail current is shown and Figure 4 shows the exact amplitude of oscillation output voltage and tail current.

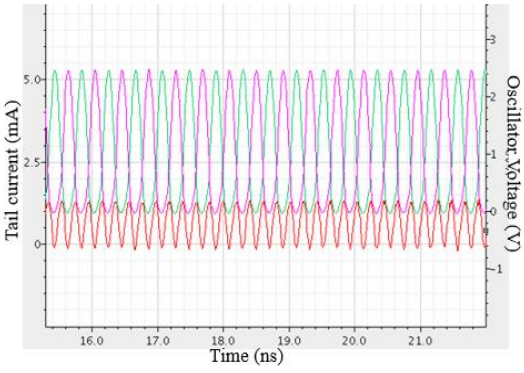


Fig. 3 Proposed VCO simulation

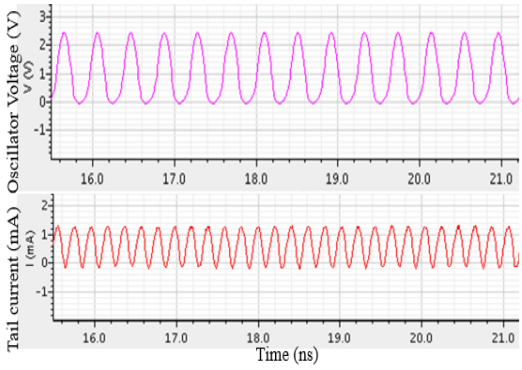


Fig. 4 Proposed oscillator output voltage and tail current

From the simulation results in Figure 3 and Figure 4, it is observed that, with the use of tail current shaping technique, the amplitude of oscillation output peak to peak voltage is achieved 2.5V and tail current is 1.2mA. As, the proposed oscillator is tuned at 2.4GHz and frequency tuning range from 2.4 to 2.48GHz is achieved by varying control voltage from 0 to 1V. The achieved bandwidth is of 80MHz, which is shown in Figure 5. The sensitivity of the proposed oscillator can be measured per 0.1V, which is observed 8MHz. This is simulated by periodic steady state analysis and the requirement is same for ISM band applications.

The PSS analysis is performed to determine the phase noise of the oscillator. As, Conventional and Proposed oscillators are simulated and results are shown in Figure 6 and Figure 7. Proposed LC oscillator has -126.3dBc/Hz phase noise at 1MHz offset frequency, as observed from Figure 6, 2.4GHz oscillation frequency and power consumption is 4.7mw at 1V supply voltage. The proposed oscillator phase noise does not vary more with the control voltage variation, which reflects from Fig 6(b). The conventional oscillator has phase noise of -119.8dBc/Hz at 1MHz offset, which is observed from Figure 7. The figure of merit is calculated by equation (5) [[10]].

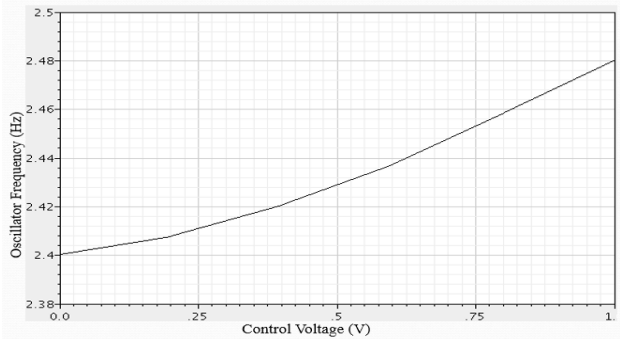


Fig. 5 Frequency tuning range of proposed oscillator

$$FOM=L\{\Delta f\}+10\log(\frac{Pdc}{1mW})-20\log(\frac{f0}{Foffset}) \quad (5)$$

Where, f0 is the oscillation frequency.
L{Δf} is the phase noise measured at a frequency offset Δf.
Pdc is the power consumption.

Here, Table 1. reflects the performance summary and comparison of conventional and proposed LCVCO. From the equation of figure of merit - FOM, it is observed that at fixed offset frequency, FOM of the LC oscillator fully depends on the phase noise and the power consumption value of the LC oscillator. As, there is trade-off between phase noise and power consumption, but phase noise is lower at low offset frequency compare to higher offset frequency due to flicker noise is reduced. So, Figure of merit (FOM) value as a reference parameter of LC oscillator is considered for performance optimization of VCO. Low value of phase noise with lower power consumption results in better value of FOM.

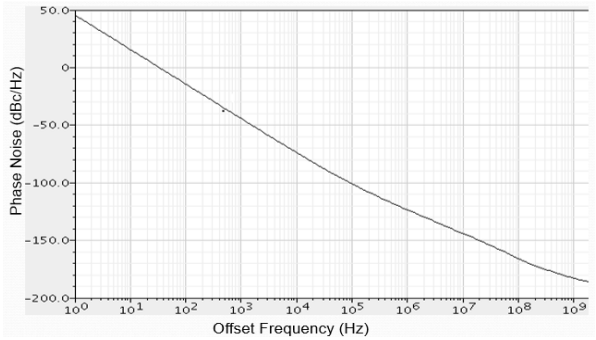


Fig. 6(a) Phase Noise of Proposed Oscillator

As, one of the most required parameter of LC oscillator for ISM frequency band, Frequency tuning range is simulated for bandwidth – channel frequency. So, value of FOMt has been calculated for performance parameter of LC oscillator.

$$FOMt=FOM-20\log[FTR/10] \quad (6)$$

Where, FTR – Frequency tuning range is in %.
FOMt is highly depends on the value of phase noise, FOM and Frequency tuning range in percentage.
This value reflects the efficiency of tuning range of oscillator. As, there is trade-off between power consumption and FTR, FOMt value gives overall performance of the LC oscillator including phase noise, power consumption and FTR.

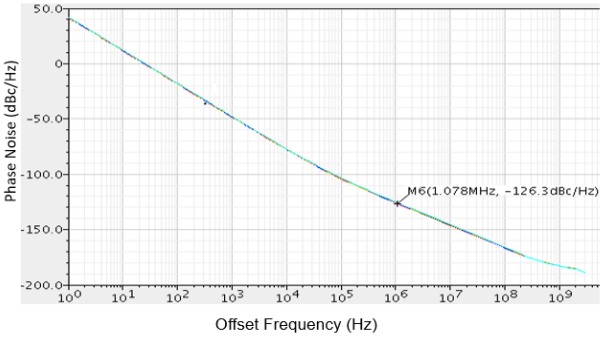


Fig. 6(b) Phase Noise of Propose LC Oscillator with tuning voltage

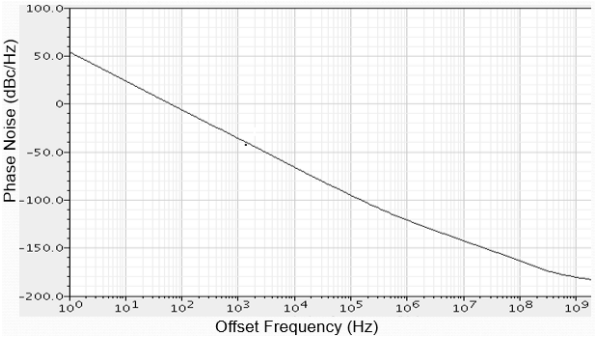


Fig. 7 Phase Noise of Conventional Oscillator

Table 1 shows the simulation result values of phase noise, Figure of Merit (FOM) and FOMt for the conventional and proposed oscillator circuits, at 10KHz, 100kHz, 1MHz and 10MHz offsets, as well as the amount of phase noise improvement for the proposed LC oscillator circuit. At 1MHz offset, the proposed oscillator results around 6.3dB lower phase noise, compared to the conventional oscillators. The FOM value of proposed oscillator at 100kHz and 1MHz is -183.58dBc/Hz and -187.18dBc/Hz. Compared to conventional oscillator improved FOM is 8.91dB and 7.44dB at 100kHz and 1MHZ offset frequency and FOMt improvement is 7.76dB at 1MHz, which shows the better performance of proposed oscillator in terms of phase noise, FTR and power consumption.

Table 1. Comparison of Phase noise, FOM and FOMt

	Conventional Oscillator				***Proposed Oscillator***			
Offset Frequency	*@10kHz*	*@100kHz*	*@1MHz*	*@10MHz*	*@10kHz*	*@100kHz*	*@1MHz*	*@10MHz*
Phase Noise (dBc/Hz)	*-65.08*	*-94.93*	*-119.8*	*-142.1*	*-76.6*	*-102.7*	*-126.3*	*-144*
FoM (dBc/Hz)	*-164.82*	*-174.67*	*-179.74*	*-181.84*	*-177.48*	*-183.58*	*-187.18*	*-185.88*
FoMt (dBc/Hz)	*-155.22*	*-165.17*	*-170.14*	*-172.2*	*-167.98*	*-174*	*-177.9*	*-176.7*
Improved P.N. (dB)	-	-	-	-	*11.52*	*7.77*	*6.3*	*1.9*

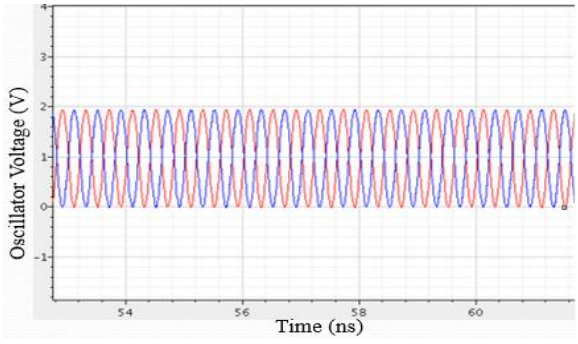


Fig. 8 Conventional Oscillator Simulation

In this proposed circuit, second harmonic thermal noise is reduced by Csh capacitor. The Mb and Mc transistors are used to reduce the effect of flicker and thermal noise. So, overall phase noise is reduced by selecting 2pF capacitor at the tail biasing. Here, the very low value of Vdc and high resistance of 20kΩ offers high impedance at the tail gate node. Capacitors connected with the gate and output node of the oscillator with the 20pF value, offers sinusoidal voltage to self-bias the tail current and blocks DC components.

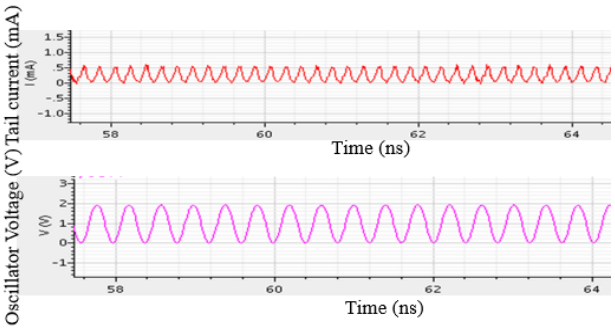


Fig. 9 Conventional oscillator output voltage and tail Current

The simulation result of conventional oscillator is shown in Figure 8 and Figure 9. The output oscillation voltage is 2V and tail current amplitude is 0.6mA

for the conventional oscillator. The proposed oscillator tail current swings up to 1.2mA and oscillation output voltage is 2.5V, which is observed from Figure 4. The tail current amplitude is and output oscillation is better compared to conventional oscillator (Figure 10). The proposed oscillation start up is at 13ns, shown in Figure 11.

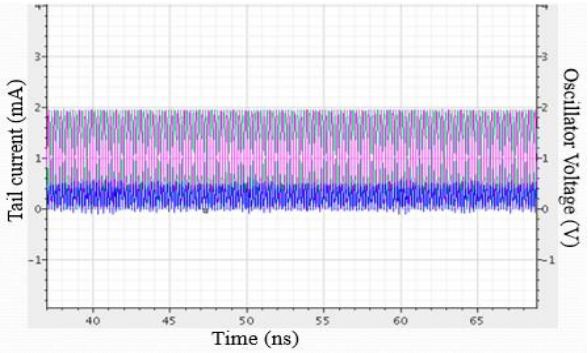


Fig. 10 Conventional oscillation with tail current

The periodic steady state analysis is performed to get the frequency tuning range of the VCO, as shown in Figure 5.

$$Fosc=\frac{1}{2\pi\sqrt{L(Cvar+Cp)}} \quad (7)$$

Here, LC oscillator is required to tune at 2.4GHz frequency for ISM band application and tuning range of 80MHz. From the equ. 7, the relation between oscillator frequency and LC tank is observed. Selected Inductor value is 3nH and the total capacitance is Ctotal = 1.4pf. Frequency tuning is achieved by capacitors as varactors. Here, nMOS transistors are used in AMOS configuration as variable capacitors. However, these all simulations are performed at 27ºC temperature and under typical process corner, where mosfet are under normal operation, with Vdd of 1v fix supply voltage. Effect of process variations are simulated here.

Table 2. Simulation results of LC VCO with different Process Corners

Temperature - 27ºC	*FF Vdd+10%*	*FF*	*TT*	*SS*	*SS Vdd-10%*
Supply Voltage	*1.1V*	*1V*	*1V*	*1V*	*.9V*
Tuning Voltage Vcnt	*0 – 1V*	*0 - 1V*	*0 – 1V*	*0 – 1V*	*0 -1V*
FTR (GHz)	*2.35 – 2.42*	*2.35– 2.44*	*2.40 – 2.48*	*2.45 – 2.54*	*2.46 – 2.57*
Phase Noise @ 10kHz	*-81.9dBc/Hz*	*-79.7dBc/Hz*	*-76.6dBc/Hz*	*-68.4dBc/Hz*	*-64.4dBc/Hz*
Phase Noise @100kHz	*-104.9dBc/Hz*	*-104.1dBc/Hz*	*-102.7dBc/Hz*	*-96.9dBc/Hz*	*-93dBc/Hz*
Phase Noise @1MHz	*-128.1dBc/Hz*	*-127.3dBc/Hz*	*-126.3dBc/Hz*	*-122.3dBc/Hz*	*-119.18dBc/Hz*
Power dissipation	*~6.5mw*	*~5mw*	*~4.7mw*	*~4.4mw*	*~3.1mw*

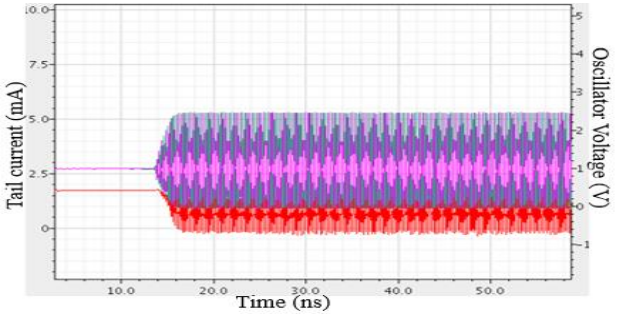


Fig. 11 Proposed VCO oscillation with tail current

To observe the effect of process corners with variation in temperature and supply voltage, in the simulations of proposed Oscillator, the total tail current and the output voltage swing of oscillation under effect of the process corner cases of {VDD+10%, FF, 0ºC} and {VDD–10%, SS, +50ºC} are compared with those in the typical case of {VDD, TT, 27ºC}. The variation in the tail current is 18% and output oscillation voltage is 12%, Figure 12 shows the effect of process corner SS at +50ºC with variation in Vdd supply voltage of 10% and typical corner at 27ºC with fix supply voltage of 1V on oscillation voltage and tail current. In this case, Vdd is 1V for typical case and is varying between .9V to 1.1V for SS and FF process corners, as a part of 10% of supply variation effect. The effect of process corners is also observed on phase noise, power consumption and frequency tuning range. Figure 13 shows the simulation results of Phase noise and frequency tuning range under FF and SS process corners. The sensitivity of the oscillator can be found with PPV simulations. The effect of supply voltage changes on tail current, output voltage as well as on phase noise can be found. The phase error generated in oscillators are due to mismatches in LC tanks and which can be derived and compensated with additional circuits or techniques. The stability of the LC oscillator is to produce stable oscillation and to maintain a consistent and fixed frequency over a given period. In this paper these parameters are not more focused, but simulations and derivations are possible to be performed. Table 2. shows the result of this comparison with process corner effects.

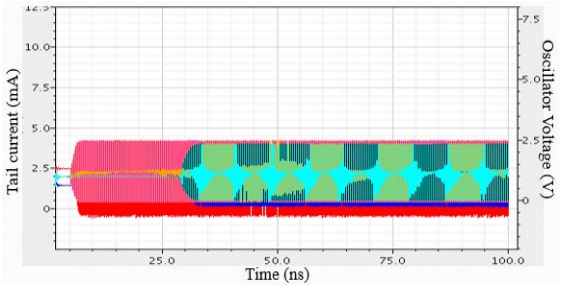


Fig. 12 Simulation with {VDD–10%, SS, +50ºC} and {VDD, TT, 27ºC} of proposed Oscillator

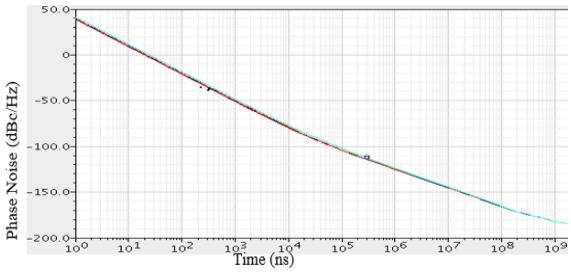


Fig. 13(a) Simulation of Phase noise with Process corner {VDD+10%, FF, 27ºC}

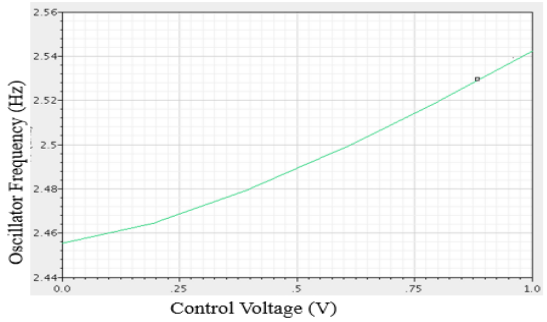
Table 3. Comparison with previously published papers

Fig. 13(b)Simulation of frequency tuning range with Process corner {VDD, SS, 27ºC}

Compare to typical process corner in FF corner, phase noise is improved but the power consumption is increased. Figure 13 shows the phase noise of -128.1dBc/Hz at 1MHz offset frequency with process corner FF and Vdd + 10% variation. The generated all simulation results are observed form Table 2 under the effect of all process corners. It is also observed form the Table 2, Frequency tuning range shifts lower under FF process corner and shifts to upper frequency under effect of SS process corner. The power consumption increases with FF process corner and reduce under the effect of SS process corner.

The oscillator circuits are implemented with the Cadence 90nm Technology. In both the oscillator circuits, all the capacitors are assumed as MIM capacitors for implementation of such capacitors, and so, less unwanted effects are generated associated with those capacitors. Fortunately, the effect of those parasitic including resistors and inductor are taken into account the circuit simulator. Figure 14 shows layout of proposed LC

Ref.	Power supply	Tech.	FTR	Frequency	Phase Noise	Δf	Power	FOM dBc/Hz
[4]	*1V*	*120nm*	*22%*	*5GHz*	*-119dBc/Hz*	*1MHz*	*10mw*	*182.9*
[5]	*2.2V*	*90nm*	*20%*	*2.4GHz*	*-105.9dBc/Hz*	*1MHz*	*5.14mw*	-
[6]	*1.2V*	*90nm*	-	*2.16GHz*	*-106.2dBc/Hz*	*1MHz*	*.53mw*	*183.6*
[7]	*1.2V*	*180nm*	*4.2-5GHz*	*4.56GHz*	*-120.3dBc/Hz*	*.4MHz*	*4.9mw*	*186.5*
[8]	*1V*	*180nm*	-	*2.55GHz*	*-122.8dBc/Hz*	*1MHz*	*3.2mw*	*186*
[9]	*1.2V*	*130nm*	-	*2GHz*	*-130dBc/Hz*	*1MHz*	*2.4mw*	*192.3*
[10]	*1.8V*	*180nm*	-	*10GHz*	*-107.8dBc/Hz*	*1MHz*	*1.45mw*	*186.2*
[11]	*1.8V*	*180nm*	*2.4-2.48GHz*	*2.46GHz*	*-124dBc/Hz*	*1MHz*	*2.86mw*	*187.2*
[12]	*1.8V*	*180nm*	*1.12-2.71GHz*	-	*-117.2dBc/Hz*	*1MHz*	*13.6mw*	*188.7*
This Work	*1V*	*90nm*	*2.4-2.48GHz*	*2.4GHz*	*-126.3dBc/Hz*	*1MHz*	*4.7mw*	*187.2*



Voltage controlled oscillator with 27.68*26.66 um area. Figure 15 shows layout of conventional LC voltage controlled oscillator with area of 23.86*17.69um.

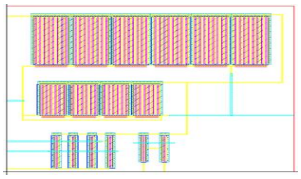


Fig. 14 Layout of proposed oscillator

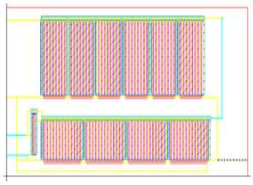


Fig. 15 Layout of Conventional Oscillator

Table 3. Shows the comparison of all the process parameters like, power supply, technology, FTR, Phase noise with offset, power consumption, FOM and area with the previously published literature. As a result, the proposed LC oscillator has better phase noise, power consumption and FOM at 2.4GHz frequency with 1V of supply.

4 Conclusion

In this paper, the phase noise is reduced to -126.3dBc/Hz at 1MHz offset frequency using tail current improvement. The oscillator is designed and simulated in cadence virtuoso using 90nm technology with 1V of supply voltage. The oscillator is tuned at 2.4GHz frequency and frequency tuning range is 2.4 to 2.48GHz achieved. This frequency bandwidth of 80MHz is achieved by control voltage tuning of 0 – 1V. The proposed VCO circuit also results better with PVT variations. The proposed oscillator demonstrates FOM and FOMt of -187.18dBc/Hz and -177.9dBc/Hz at 1MHz offset frequency with better tail current and output oscillator amplitude.

References:

[1] Ali Hajimiri, Thomas H. Lee, Design Issues in CMOS Differential LC Oscillators, IEEE journal of solid-state circuits, Vol. 34, no. 5, May 1999

[2] Emad Hegazi, Henrik S., Asad A. Abidi, A filtering Technique to Lower LC Oscillator Phase Noise, IEEE journal of solid-state circuits, Vol 36, December 2001.

[3] Pietro Andreani, Henrik S, Tail Current Noise Suppression in RF CMOS VCOs,IEEE Journal of solid-state Circuits, Vol. 37, NO. 3, March 2002

[4] J. kim, J-O. Plouchart, N. Zamdmer, M. Sherony, Yue Tan, Meeyoung Yoon, R. Trzcinski, M. Talbi, J. Safran, A Power-Optimized Widely-Tunable 5-GHz Monolithic VCO in a Digital SOI CMOS Technology on High Resistivity Substrate, IEEE 2003 International Symposium on Low Power Electronics and Design, August 2003.

[5] A. J. Ginés, R. Doldán, A. Villegas, A. J. Acosta, M. A. Jalón, D. Vázquez, A. Rueda and E. Peralías, A 1.2V 5.14mW Quadrature Frequency Synthesizer in 90nm CMOS Technology for 2.4GHz ZigBee Applications. Asia Pacific Conference on Circuit and Systems, China IEEE 2008.

[6] Rafaella Fiorelli, Eduardo J. Peralías, Fernando Silveira, LC-VCO Design Optimization Methodology Based on the gm/ID Ratio for Nanometer CMOS Technologies, IEEE transactions on microwave theory and techniques, vol. 59, no. 7, July 2011

[7] Han Wang, Liguo Sun, Lu Huang, A 4.6 GHz cascade switched biasing LC–QVCO using source-body resistor, Analog Integrated Circuit and Signal Processing, pp 539-547, 2013.

[8] Nan Chen, Shengxi Diao, Lu Huang, Fujiang Lin, Reduction of 1/f3 phase noise in LC oscillator with improved self-switched biasing, Analog Integrated Circuit and Signal Processing, pp 19 - 27, 2015.

[9] Bahram Jafari, Samad Sheikhaei, Phase noise reduction in a CMOS LC cross coupled oscillator using a novel tail current noise second harmonic filtering technique, Microelectronics Journal, pp 21–30, 2017.

[10] Bahram Jafari, Samad Sheikhaei, Phase noise reduction in LC cross coupled oscillators using sinusoidal tail current shaping technique, Analog Integrated Circuit and Signal Processing, April 2018.

[11] Divyesh Sachan, Harshbardhan Kumar, Manish Goswami, Prasanna Kumar Misra, A 2.4 GHz Low Power Low Phase-Noise Enhanced FOM VCO for RF Applications Using 180 nm CMOS Technology, Wireless Personal Communication, April 2018.

[12] Yin Zhang, Wanrong Zhang, Pei Shen, Hongyun Xie, Dongyue Jin, Shu Xu, Xin Yang, Zhao Zhang, A Novel LC VCO with High Output Power and Low Phase Noise Using Differential Active Inductor, IEEE, 3rd International Conference on Integrated Circuits and Microsystems, 2018.

[13] Lesson, D. B, A simple model of feedback oscillator noise spectrum, Proceedings of the IEEE, 54(2), 329–330, 1966.

[14] Hajimiri, A., & Lee, T. H, A general theory of phase noise in electrical oscillators. IEEE Journal of Solid-State Circuits, 33(2), 179–194

[15] A. Jannesari and M. Kamarei, Sinusoidal shaping of the ISF in LC oscillators, International Journal of Circuit Theory and Applications, vol. 36, no. 7, pp. 757–768, 2008.

[16] I.-S. Shen, T.-C. Huang, and C. F. Jou, A low phase noise quadrature VCO using symmetrical tail current-shaping technique, IEEE Microwave Wireless Component Letter, vol. 20, no. 7, pp. 399–401, 2010.

Conflicts of Interest

The author(s) declare no potential conflicts of interest concerning the research, authorship, or publication of this article.

Contribution of individual authors to the creation of a scientific article (ghostwriting policy)

The author(s) contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of funding for research presented in a scientific article or scientific article itself

No funding was received for conducting this study.