A High Gain, High BW OP AMP withFrequency Compensation Techniques at 65 nm Technology

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Abstract— OP-AMPs finds applications in different domains of electronics engineering including communications. There has been several OP-AMP configurations realized in the last decades for different target applications. But with the evolution of communication standards, to meet the demand for high data rate over the years, requirement for a high frequency and high BW OP-AMP is gaining attention. This makes the design challenge much higher. This paper presents a two-stage CMOS amplifier which uses frequency compensation method to facilitate higher BW. Different parameters like Gain, Gain band width product (GBWP), Phase Margin and Total Power dissipation are considered in this design. A step-by-step procedure for an efficient amplifier design is followed using frequency compensation. We have achieved a gain-bandwidth product (GBWP) of 110 MHz that is capable of driving large capacitive loads. It also achieves 77.7 dB gain with a phase margin of 60^{o}.

Keywords—compensation, Gain Bandwidth product

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1. Introduction

OP AMPs are the basic building blocks of many electronic applications. Communication is a domain where it plays a very vital role in signal conditioning. Though different OP-AMPs are being designed over the years but with the advancement of communication standard, design challenges are also going up. OP AMPs needs to be optimised to be used in analog systems to facilitate of higher accurate gain, input and output impedance matching, line development and bandwidth expansion, [1], [2]. Apart from the other challenges, the biggest challenge is to improve op amp stability in the wide bandwidth. The solution is therefore to compensate the magnifier according to the frequency response process.

The purpose of this paper is to design a simplified frequency compensation scheme along with the OPAMP to make it stable with high gain in high frequency range. Secondly the proposed circuit must have the less power consumption and generate less noise so the second problem is to make the design power aware and noise aware. For this we will use a two stage Miller compensation circuit.

This paper presents a two-stage CMOS amplifier which uses frequency compensation method to facilitate higher BW. Different parameters like Gain, Gain band width product (GBWP), Phase Margin and Total Power dissipation are considered in this design. A step-by-step procedure for an efficient amplifier is followed using frequency compensation. We have achieved a gain-bandwidth product (GBWP) of 110 MHz that is capable of driving large capacitive loads. It also achieves 77.7 dB gain with a phase margin of 60^{o}. The remaining part of the paper is organised as follows:

Section II describes the circuit fundamentals, section III deals with mathematical calculations. Section IV presents the simulation results and section V includes concluding remarks.

2. Fundamentals of the Proposed Circuit

2.1 Two stage Miller,s Compensation

The block diagram is shown in Figure 1 below.

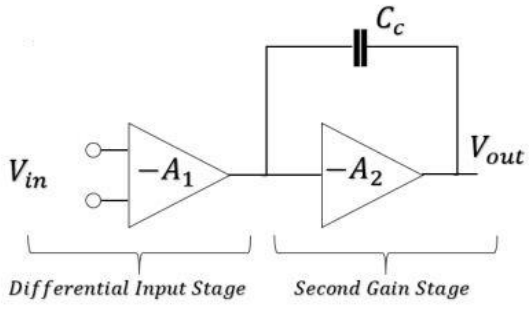

Fig. 1 Block diagram of a Miller compensated operational amplifier

It is basically a two stage frequency compensation circuit where the two stage can be modeled as the cascade of two amplifier. Here the first stage is differential amplifier which act as an input differential pair and also it forming a current mirror circuit acting as a load. The second stage is the common source stage which acting as a gain stage. The need of this common source arises for the gain obtain from the differential amplifier is not high enough. The compensation capacitor is connected to the second stage to shift the associated transmission zero to higher frequency. The Miller-effect of a bug and more of the dominant, the second part of the pole down in frequency, while the other, less dominant, and the sign of the pile-up in the frequency of post-

distribution). This action is intended to ensure a good phase margin, the force of the transfer function of the system is to act as a single-pole system. The Miller compensation method is that there is a compensation capacitor is to be installed between the initial level of output (differential amplifier), and the op-amp output gain: the output of the amplifier).

A two-stage amplifier can be modelled as a cascade of two amplifiers as shown in Figure 2. The first stage is a differential amplifier, which generates an amplified version of the difference input signal. In this stage, the CMRR, slew rate, and other characteristics are to be determined.

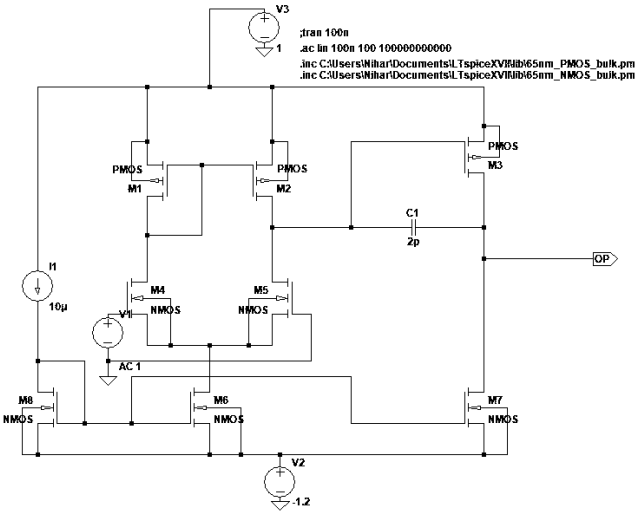

Fig. 2: Miller compensated two stage operational amplifier

The second stage is an inverting amplifier. The purpose of this step is to ensure that a large current gain. The gain stage and the input stage forms two poles which have impact on the stability of the feedback system. Compensation techniques needs to be used in order to ensure the stability of the amplifier in a specific gain.

The design consists of a NMOS differential amplifier with an active load for the first stage, and a PMOS common-source amplifier as the second stage. A compensation capacitor is connected between the second levels of the output of the first stage from the output to obtain a post-distribution, which means that, in the case of an op-amp. Here the simulation is done in LTspice at 65nm CMOS technology. For a simple two-stage op-amp, as shown in Figure 2. A standard power supply, it will also be used to generate the power for the reference only. The parts of each of these blocks will be discussed in the following sections of this document. The required operational amplifier specifications are descried below.

3.Mathematical Calculation

A design step for two stage Op Amp can be constructed as

Basic op amp Equations are

$$I_D = \frac{\mu_{n,p} C_{ox}}{2}\left(\frac{W}{L}\right) V_{ov}{}^2 \text{ or } \frac{W}{L} = \frac{2I_D}{\mu_{n,p} C_{ox} V_{ov}{}^2}$$

$$\text{Trance – conductance, } g_m = \sqrt{2\mu_{n,p} C_{ox}\left(\frac{W}{L}\right) I_D}$$

$$= \frac{2I_D}{V_{ov}}$$

$V_{ov} = V_{GS} - V_T$, here V_{ov} is called voltage overdrive.

Step 1: we have to design the compensation capacitor C_c

$$C_c = \frac{g_{m1}}{2\pi f_{uf}}$$

It should be noted that the compensation capacitor needs to be optimized again after the design procedure is complete. During simulation tweaking the compensation capacitor is required to obtain the appropriate stability.

Step 2: we have to calculate g_m

$$gm_{1,2} = GB \cdot C_c$$

Step 3: then we calculate $I_{D1,2}$

$$I_{D1,2} = SRC_c$$

Step 4: thus we can calculate the aspect ratio $\left(\frac{W}{L}\right)_{1,2}$

$$\left(\frac{W}{L}\right)_{1,2} = \frac{\left(g_m\right)^2}{K_n \cdot I_{D1,2}}$$

Similarly, this way we can calculate the aspect ratio for the other MOS as well.

4.Simulation result

The circuit shown in Figure 2 has been designed in a 0.65-µm CMOS technology. A supply voltage of ±1.6 V has been employed. The following transistor dimensions are calculated by using the equations presented in the previous section. It is expressed as W(µm)/L(µm) per transstor. M_1 ➔ 7/1, M_2 ➔ 7/1, M_3 ➔ 60/1, M_4 ➔ 3/1, M_5 ➔ 3/1, M_6 ➔ 15/1, M_7 ➔ 70/1, and M_8 ➔ 10/1. The input voltage of ±0.400 mV have been applied and the bias current of I_1 = 10µA. A conservative compensation capacitance Cc = 20 pF has been chosen for the proposed circuits.

4.1 Result Analysis

This section presents various simulation results of electrical characteristics of two stage op amp such as transient analysis, gain, frequency analysis, and noise, power and output voltage.

1) Transient analysis

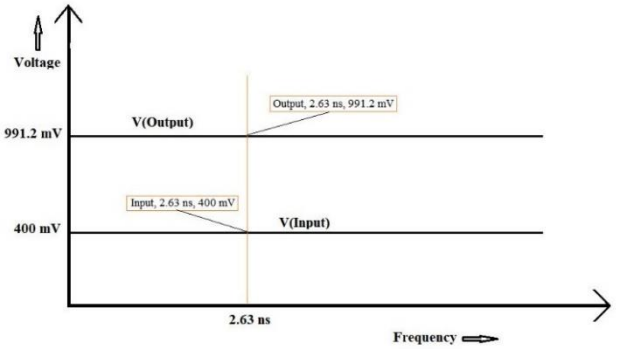

Fig. 3: Transient analysis

The Transient analysis (Figure 3) in the time domain, it is a study of one parameter, such as voltage or current builds up in the course of time. If we look at the raw data, we can see that the behavior for a certain period of time. From this result we can see the increase in the output voltage as compared to the input. For the input voltage of 400mV we get the amplified output of 991.2 mV.

2) AC analysis

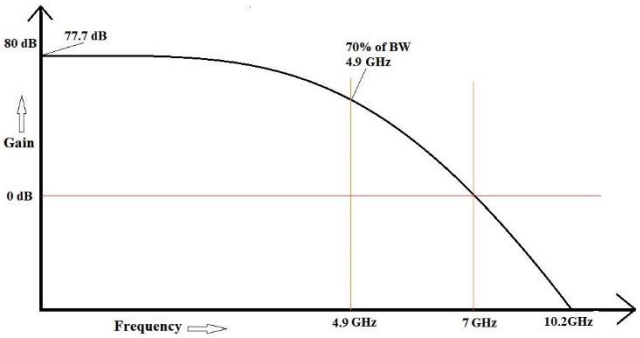

Fig. 4: AC analysis

The AC analysis presented in Figure 4 shows that the design works well in higher frequency band up to around 4.9GHz. We can think of the noise in the graph in a Cartesian coordinate system with a real and an imaginary axis, we can think of it as a Nyquist diagram. From the AC analysis we can check the frequency, BW, GBP. Here the gain we get is 77.7 dB, and the bandwidth is 4.9 GHz.

3) Phase Margin

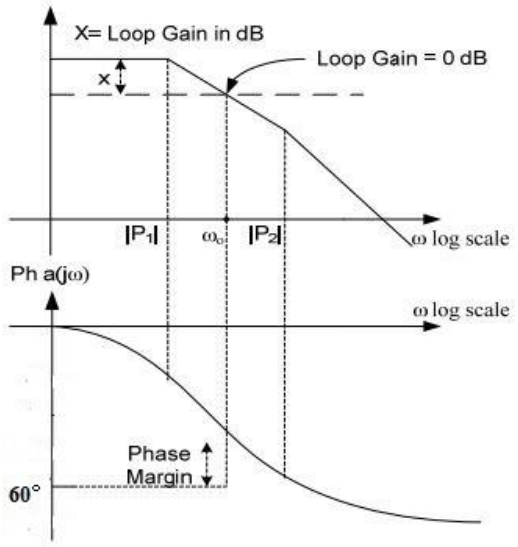

Fig. 5: Phase and gain relation

Additional phase lag that makes the system on the verge of instability is called the phase margin. Here we get the phase margin of $60°$ as shown below. The phase and gain margins are presented in Figure 5 and Figure 6.

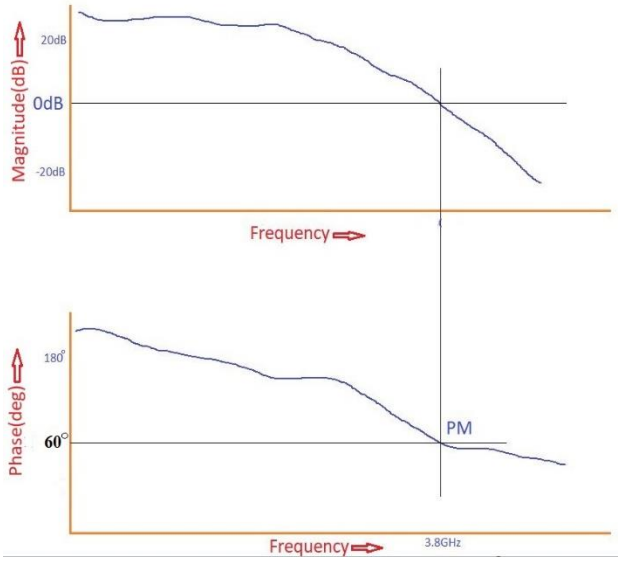

Fig. 6: Phase Margin

4) Noise analysis

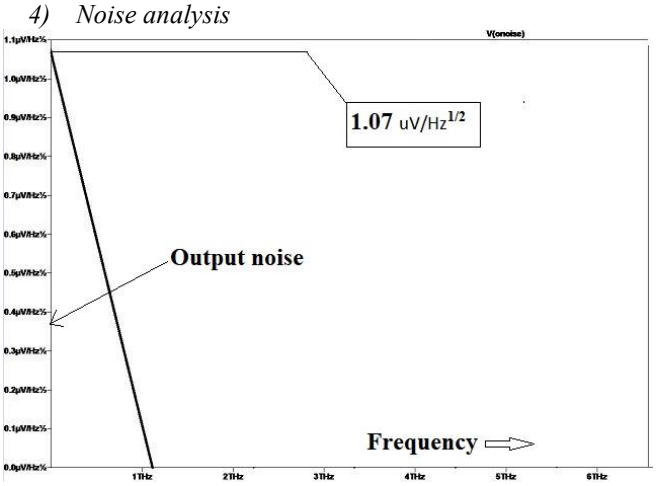

Fig. 7: Noise analysis

The noise analysis shown in Figure 7 depicts that the noise level is equivalent to the system, as well as the injection of noise from an external source, in the right environment. Noise analysis in an op-amp circuit is very critical where accuracy is the prime concern. In this result we get the noise of 1.1 $\mu V/\sqrt{Hz}$.

4.2 Results Chart

Below shows the results of the proposed circuit (Table 1).

Parameter	Value
Open Loop Gain	77.7 dB
Bandwidth	7 dB
Phase Margin	60°
Noise	1.1 $\mu V/\sqrt{Hz}$
Output Voltage for the input voltage of 400 mV	991.2 mV

Table 1: simulation results

4.3 Comparative Tables

In this section we compare this results with some previously reported works (Table 2).

Paper	Technology	Gain	PM	Noise
2017, [1]	180 nm	61	68°	14 $\mu V/\sqrt{Hz}$
2018, [2]	180 nm	63	78°	8 $\mu V/\sqrt{Hz}$
2019, [3]	180 nm	73	56°	13.6 $\mu V/\sqrt{Hz}$
2020, [4]	180 nm	70	72°	14 $\mu V/\sqrt{Hz}$
This paper	65 nm	77.7	60°	1.1 $\mu V/\sqrt{Hz}$

Table 2: Comparison table

5. Conclusion

Lastly, interesting studies in the field can also be found in [5], [6], [7], [8], [9], [10], [11], [12]. Specifically, this work implements a two-stage OP-AMP for high BW applications. Frequency compensation technique is successfully used to attain high BW while maintaining a sufficiently higher gain and GBWP. Different other parameters like Phase Margin and Total Power dissipation are considered in this design to make it stable and to have low power dissipation. A step-by-step procedure for an efficient amplifier design is followed. We have achieved a gain-bandwidth product (GBWP) of 110 MHz that is capable of driving large capacitive loads. It also achieves 77.7 dB gain with a phase margin of 60°. Hence this design can be claimed to be suitable for high frequency applications.

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Conflicts of Interest

The author(s) declare no potential conflicts of interest concerning the research, authorship, or publication of this article.

Contribution of individual authors to the creation of a scientific article (ghostwriting policy)

The author(s) contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

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