Design and Analysis of a Modified TG Rectifier with Substrate Voltage Compensation Techniques at 45 nm Technology for High Frequency Low Power RF Energy Harvesting

[1]MANASH PRATIM SARMA, [2]KANDARPA KUMAR SARMA

[1,2]Department of Electronics and Communication Engineering

[1,2]Gauahati University, Assam, INDIA

[1]mpsarma@gauhati.ac.in, [2]kandarpaks@gauhati.ac.in

Abstract: - The development of latest generation of wireless communication standards in the recent years has created enormous possibility to deploy high speed wireless network throughout the globe. There is always demand for high speed, seamless data connectivity. But it is a well-known fact that the increase in speed always makes the power consumption higher. Also while attempting to cater to the need of connectivity to a remote location, the major bottleneck is the availability of power. Hence incorporating self-sustainability to a wireless network is becoming the need of the hour. Radio frequency (RF) energy harvesting (EH) is gaining much attention in contemporary communications in this context. In the design of an EH system, the high frequency rectifier plays a significant role. Apart from several design hurdles that exist in a high frequency rectifier, to attain a high percentage conversion efficiency (PCE) at lower input power is the primary design challenge. This paper presents a design of a modified transmission gate (TG) based high frequency rectifier with two substrate voltage compensation techniques, viz. capacitor and MOS based compensation for RF EH system.The proposed capacitor and MOS based techniques enable the rectifier to achieve a PCE upto 86% and 92% at -5dBm respectively in its single stage implementation. This can be claimed to be the highest in-class efficiency as compared to recently published works. The frequency responses with both the techniques depict a wide band performance covering all popular wireless bands. The dynamic power dissipations (DPD) observed are 12nW and 16nW at -5dB, whereas the leakage power (LP) is $20x10^{-51}$W and zero respectively. Further such an performance are obtained using minimal number of transistors, viz. 4 and 5 respectively.

Key-Words: -Energy Harvesting, PCE, Transmission Gate

Received: July 14, 2019. Revised: November 12, 2019. Accepted: December 4, 2019. Published: January 2, 2020.

1 Introduction

With the improvement of wireless communication technology and increasing demand for high data rate network, lots of efforts have been made to deploy connectivity all across the globe. Along with the data rate, the network life-time and power management is becoming another important aspect. In line with the idea of green communication, making the networks self-sustainable in terms of power is becoming a very significant issue in all modern day wireless networks. Hence the network must have the capabilityto harvest energy from different sources so as to maintain the self-sustainability as well as virtual operation [1]. Network life-time can be enhanced with energy harvesting (EH) capability. It makes installing a network a less complicated issue at any hard reach location. Hence energy harvesting has become an crucial part in medical as well as surveillance applications [1] [2]. There are several natural and artificial sources available that can be utilized for harvesting energy. As the nature of the sources available for harvesting are diversified and there needs the transfer of the harvested energy from node to node, the related design has to be of different capabilities and efficiencies [3]. Also since there happens to be several RF sources available in present time, in outdoor as well as indoor environments, RF EH is becoming a major EH candidate to be explored by the designer.

An EH design is formed by a rectifier or a charge pump. Several design challenges are faced while designing such a rectifier. Such challenges are identified as high frequency compatibility, low power dissipation, lesser silicon area etc. But the enhancement of the power conversion efficiency (PCE) at lower input power is the most important criteria which the designer must address while formulating an efficient circuit design. A Cross coupled bridge rectifier with differential RF input is reported that provides low on state current and negligible leakage current and thus offers a better PCE [4]. An Ultra High Frequency (UHF) rectification unit based on voltage doubler is also designed with the technique of internal voltage cancellation to facilitate a zero-threshold transistor. They have claimed to achieve a good with reduced area [5]. A very widely used structure in EH is the Dickson charge pump. Several modifications to the basic structure have been proposed by several designers for specific applications achieving different efficiencies. The Dickson charge pump has been modified to reduce the leakage current with linear regulator and thereby total power consumption can be reduced [6]. Another Dickson charge pump based rectifier with improved performance in two configurations are presented which works in GSM band with a satisfactory PCE [7]. Also dynamic threshold reduction technique based CMOS rectifier has been designed with the use of a clamper to reduce the effective threshold voltage and increase the sensitivity and hence achieving a high PCE [8]. A coplanar waveguide based compact RF rectifier has been proposed in [9], which claims to achieve a peak PCE of 74.8% at 10dBm in the frequency range of 0.1 to 2.5GHz. The structure is cascaded to get a higher output voltage. A low temperature coefficient bandgap voltage reference along with a high efficiency rectifier is reported in [10]. A curvature compensation technique is also proposed and the final PCE of 87.2% is achieved.A low power CMOS full bridge rectifier with four transistors at 130 nm technology is presented in [11]. An AC-DC rectifier, an impedance matching network and a DC-DC converter with maximum power point tracking system is designed which is observed to attain a peak efficiency of 5%.

This paper presents a design of a modified transmission gate (TG) based high frequency rectifier with two substrate voltage compensation techniques, viz. capacitor and MOS based compensation for RF EH system.The proposed techniques enable the rectifier to achieve a PCE upto 86% and 92% at -5dBm respectively in its single stage implementation. This can be claimed to be the highest in-class efficiency as compared to recently published works. The frequency responses with both the techniques depict a wide band performance covering all popular wireless bands. The dynamic power dissipations (DPD) observed are 12nW and 16nW at -5dB, whereas the leakage power (LP) is 20x10-51W and zero respectively. Also this is achieved with minimal number of transistors, viz. 4 and 5 respectively.

The remaining of the paper is organized as follows. Section II deals with the proposed rectifier design with compensation techniques along with explanation of the functionality, Section III deals with derived results and discussion and Section IV includes the concluding remarks.

2 Design of the Rectifier with Capacitor and MOS based Compensation Techniques

The generic structure of an EH system consists of three significant units; viz. the matching unit, the rectifier and the power management unit. This is shown in Fig.1.Among all our design emphasis is on a topology for an efficient rectifier suitable for high frequency and low signal power scenario. There are different hurdles faced while designing a rectifier in such a constrained situation. As the PCE is the foremost criteria, emphasis has to be given to enhance this parameter with the use of minimal number of devices. It has been observed that in a EH rectifier, the connection of the device substrate, particularly the pMOS is a bit complicated. This is because it should always be connected to a high voltage which happens to be the DC supply voltage in general case. But as there can't be a DC supply voltage in an EH rectifier, the substrate has to be connected to the signal voltage. As the signal voltage in many a times falls to a low value, the circuit performance suffers in these time durations. Hence some substrate compensation technique is essential. This paper explores this dimension of an EH rectifier.

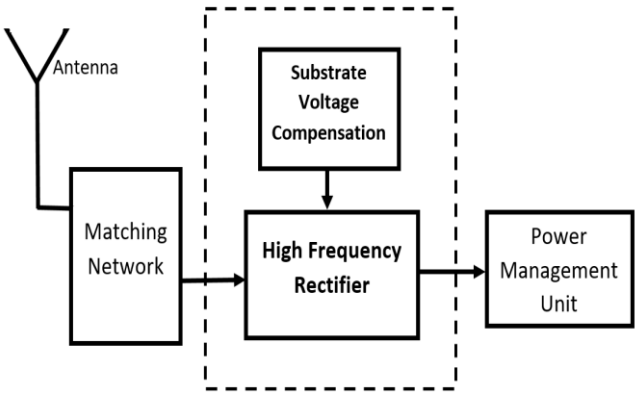

Figure 1: The Block Diagram of the proposed EH system.

The basic unit of the rectifier is designed using the concepts of the transmission gate (TG). The concept of TG is well established and has been used in many CMOS based digital circuits. The nMOS pass transistor can pass the negative voltage efficiently with less propagation time while the pMOS pass transistor allows the positive voltage efficiently with less propagation time; hence the TG can be a solution to such situations where the circuit is subjected to both the voltage levels. Also the TG generates a sufficiently higher on state current for a wide range of input voltages.

The circuit presented here is a modification to the TG based rectifier designed by us which was reported in [12]. As stated ealier, the substrates of the nMOS and the pMOS of the TG needs to be connected to the ground and the DC supply voltage respectively to create a proper biasing condition to the devices. This is essential to ensure the desired performance of the circuit. In a normal digital circuit there is nothing to be bothered by the designer. But complexity arises in this kind of EH rectifiers where a DC voltage source can't be used as this will make the entire idea of EH pointless. This is due to the fact that point of self-sustainability of the system will be completely lost. The pMOS substrate can be directly connected to the RF input but this also has the limitations for the purpose as this voltage may either be sufficiently low or even negative throughout a significant time in the entire signal time period. This compels the designer to explore some alternate circuit arrangements to keep the pMOS substrate at a constant high voltage. This paper proposes two substrate voltage compensation techniques to deal with the aforementioned issue. Both the techniques are simple and are realized with minimal number of components and/or devices. The functionality of both the techniques are explained in the sub-sections below.

2.1 Capacitor Based Compensation

A capacitor based compensation technique is implemented as a modified and extended version of the previously designed TG based rectifier [12]. One capacitor is used to connect each of the pMOS substrate and the RF input. The capacitor gets charged by drawing the current from the RF input. The voltage developed across the capacitor can maintain a positive potential at the substrate even when the RF input goes low. Though the capacitor gets discharged completely if the RF input remains at lower level for a sufficiently longer time duration. But this technique definitely increases the time of proper functioning of the circuit. This is shown in Fig.2. Lastly, we have studied, [13], [14], [15], [16], [17], [18], [19] and [20] regarding this research subject.

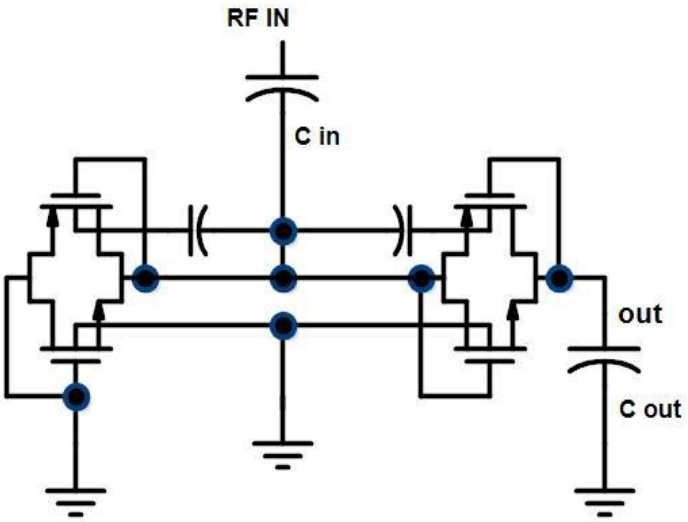

Figure 2: Proposed TG based rectifier with capacitor based substrate compensation

Let us consider the input RF voltage be $V_{in}(t)$, the capacitance connected to the substrate be C_s and total resistance at the charging path be R_c. When the input voltage is high the capacitor will be charged and the voltage developed across the capacitor shall be

$$V_c=V_{in}(t)[1-e^{-t/R_cC_s}] \quad \ldots\ldots\ldots(1)$$

When the input voltage $V_{in}(t)$ falls to a low value, the voltage V_c appeared at the substrate and thereby maintains a sufficiently higher value at least for one R_cC_s time when the voltage will get dropped by 68% due to discharging. Hence this can be a simple yet effective technique to be applied.

2.2 MOS Based Compensation

Another substrate compensation technique is proposed to be used as an improved and extended part of the previous TG based rectifier design [12]. This configuration is based on a diode connected pMOS. The gate and the drain terminal is connected to the RF input and the source is getting connection to the output. The substrate of this pMOS is connected to the substrates of the pMOSes in the rectifier. This is done to maintain a high positive voltage at both the pMOS substrates so as to maintain a proper functioning of the circuit even when the input voltage falls to a low or even negative value. This modified circuit is shown in Fig. 3.

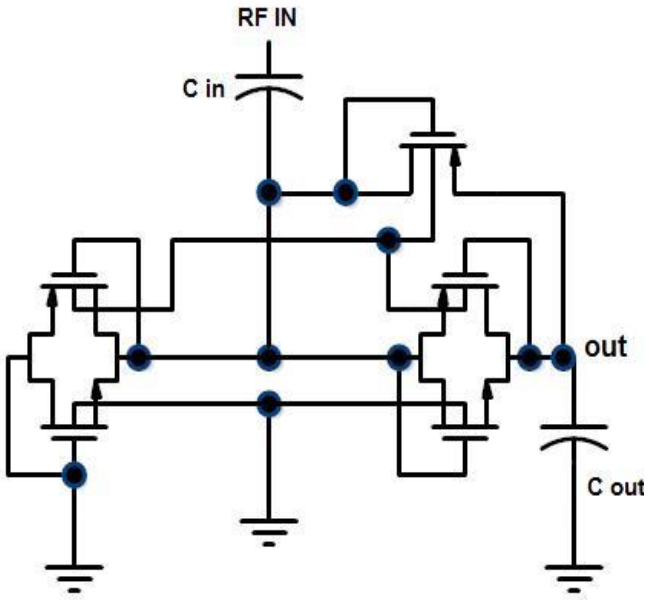

Figure 3: Proposed TG based rectifier with MOS based substrate compensation

In both the cases a high voltage at the pMOS substrates can be maintained over a longer duration than the uncompensated counterpart. Hence the successful rectification will happen over a larger time duration during the negative cycle of the input. This will contribute to the increase of effective on state current through the pMOSes. So the output voltage and current increases which finally yields a higher PCE.

In a TG structure when input is positive, the pMOS will be initially saturated and then shall switch to non-saturation state while the nMOS will be in saturation state.

If we consider the $I_{Dn}$and I_{Dp} be the current through the nMOS and the pMOS respectively and V(t) be the RF signal voltage, then the total output current is

$I_{out}= I_{Dn}+ I_{Dp}$……(2)

With the rest of the description as in [12], the PCE can be calculated as

$PCE = (P_{out} / P_{in})*100\%$……(3)

Here the I_{Dp} will increase which will enforce more charging current at the C_{out} and which makes the V_{out} to rise. Thus the PCE will also increase. This is why the compensation techniques are significant.

3 Analysis of Circuit Performance and Discussion

This section presents the experimental results derived and the analysis of the results as well as the comparison of the performance parameters

Before designing the circuit under consideration, optimization of the transistor sizing has to be done. With the use ofsimulation based optimization techniques as reported in [12] the aspect ratio of both the nMOS and the pMOS are tailored as shown in Table 1. The basic consideration of optimization to ensure anminimum power dissipation which is another essential parameter to be achieved by the design.

Table 1: Aspect Ratios of both nMOS and pMOS devices

L_n	W_n	L_p	W_p
45nm	150nm	65nm	150nm

The transient response of the circuits are important to know the time domain rectified output. It directly gives the idea whether a steady output is available over a period of time. The transient response of both the circuits is obtained at 2dB and -5dB respectively and is shown in Fig. 4. The output voltage observed are 816 mV and 820 mV at 2dB input power for capacitor compensation and MOS compensation respectively. Again the output voltages at -5dB input power are 320mV and 300mV for capacitor compensation and MOS compensation respectively.

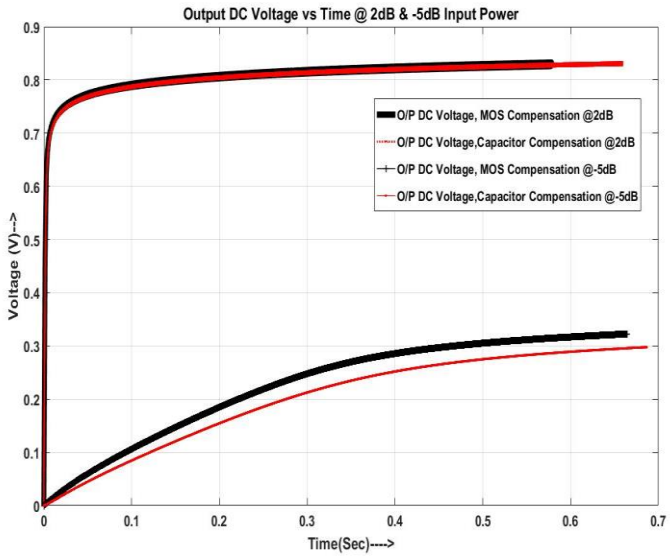

Figure 4: Output DC Voltage of both the circuits

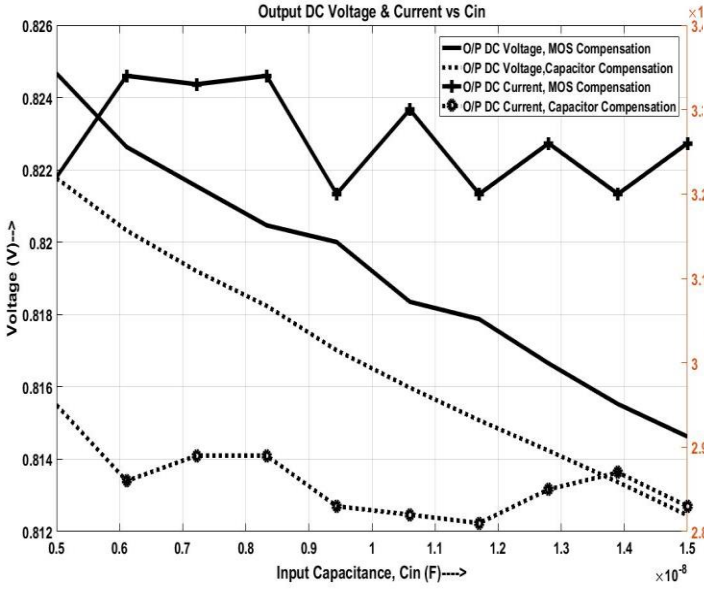

Figure 5: Output DC voltage and current vs C_{in} for both the circuits

The dependence of the input capacitance on the output voltage and current needs to be observed. The DC output voltages and currents are plotted with input capacitance. It is seen that both the output voltage and output current are better in case of the MOS based compensation technique. This is shown in Fig. 5. There is a decrease in the voltage and current values as the input capacitance increases. This is due to the fact that with the increase in capacitance the capacitor becomes slower hence will respond poorly to a high frequency signal.

Similarly the output behaviour with respect to output capacitor value needs to be studied for both the cases. The DC output voltage and current shows better result in the MOS based compensation than that of capacitance based compensation when plotted with different value of the output capacitance which is shown in Fig. 6. The voltage and current in both the circuits show a decline with increase in output capacitance.

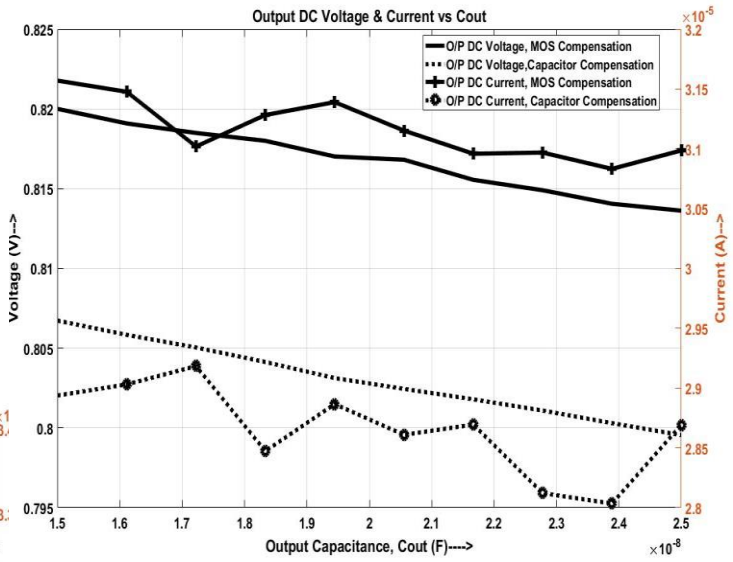

Figure 6: Output DC voltage and current vs C_{out} for both the circuits

The length and width of both the devices will have an impact on the output voltage and current. Hence this impact needs to be studied. In Fig. 7 the output voltage and current with respect to the length of the nMOS (L_n) is presented for both the circuits. Here also the MOS based compensation is seen to perform better. The output voltage and current increases with the length of the nMOS channel.

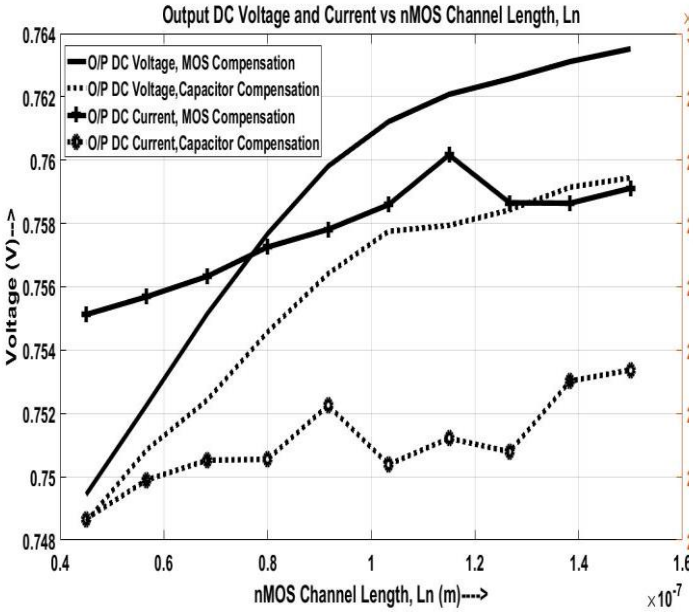

Figure 7: Output DC voltage and current vs L_n for both the circuits

Similarly the output voltage and current is plotted with nMOS channel width (W_n), pMOS channel length (L_p) and pMOS channel width (W_p) and are presented in Fig. 8, Fig. 9 and Fig. 10.

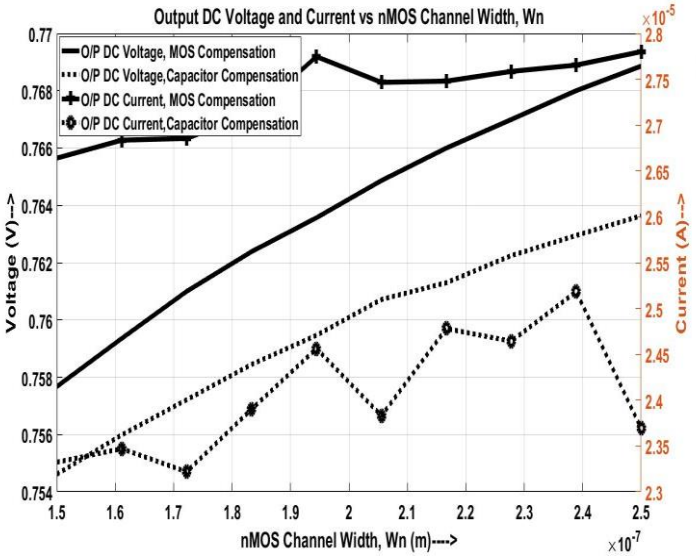

Figure 8: Output DC voltage and current vs W_n for both the circuits

The better performance of the MOS based compensation is reflected in all the Fig. 8, Fig. 9 and Fig. 10. In Fig. 8 it is seen that the voltage and current in both the circuit increases with the W_n value. Again the declining of the output voltage and current with the L_p value is depicted in Fig. 9. The output voltage and current is seen to increase with the increase in W_p in the Fig. 10.

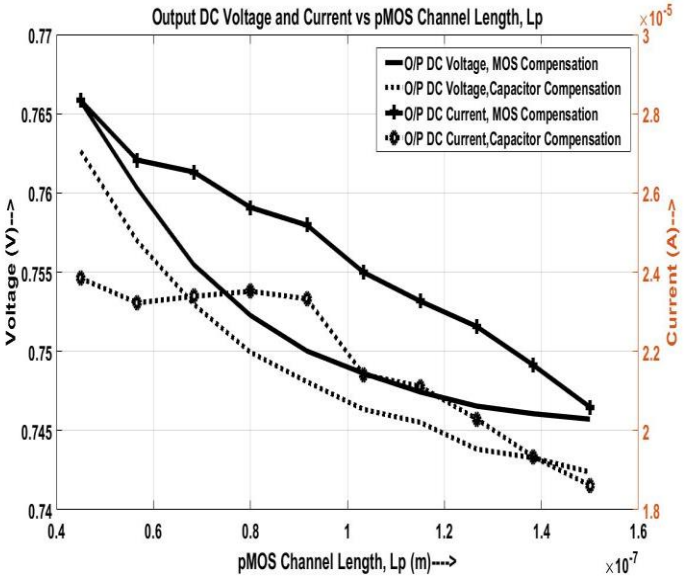

Figure 9: Output DC voltage and current vs L_p for both the circuits

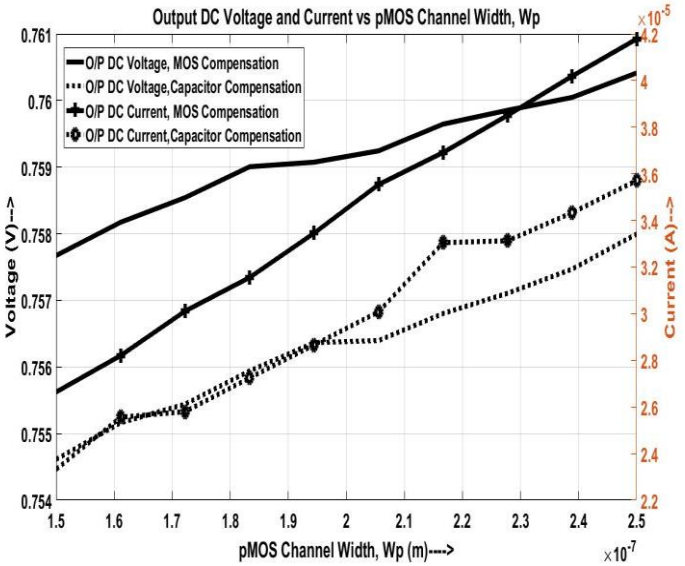

Figure 10: Output DC voltage and current vs W_p for both the circuits

The frequency response of both the circuit is simulated which shows that both the circuits are capable of being operated at a wideband covering almost all popularly available commercial bands. The output AC component of voltage and current of both the design across the frequency range is shown in Fig. 11.The AC components present throughout the frequency range is negligible which clearly shows efficient rectification in the whole band.

The temperature profile of both the circuits are analyzed. The change of voltage and current with the increase in temperature over a wide temperature

range is seen to be almost zero in case of capacitor compensation and is negligible in MOS based compensation. It clearly indicates the temperature stability in terms of both voltage and this is presented in Fig. 12.

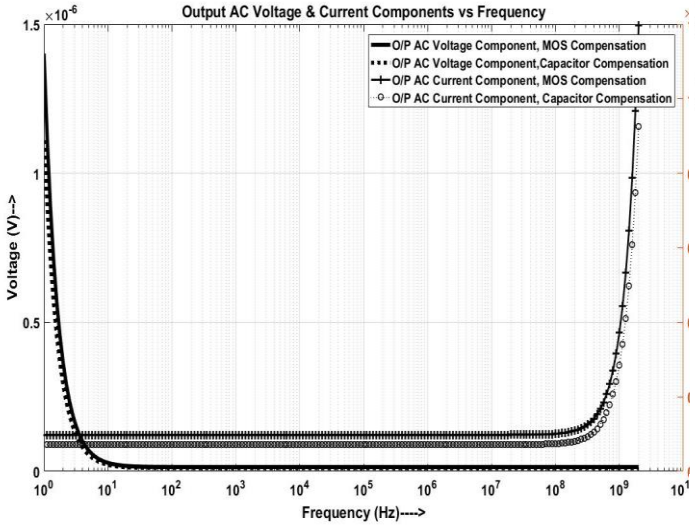

Figure 11: Output AC components of voltage and current vs frequency for both the circuits

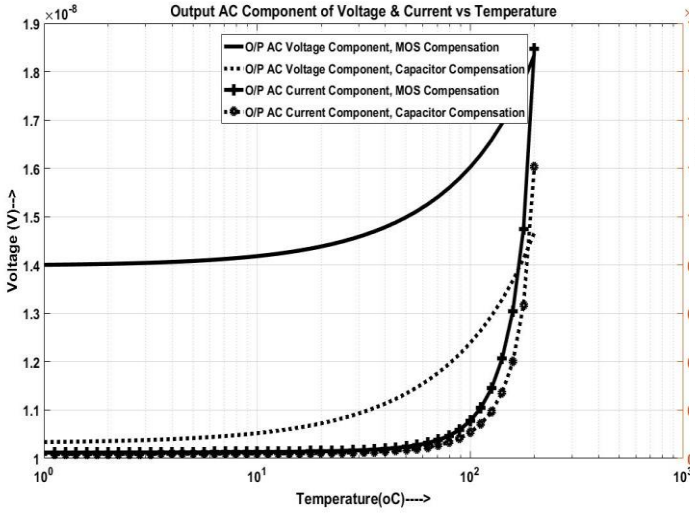

Figure 12: Output AC components of voltage and current vs temperature for both the circuits

The circuit performance should be analyzed over a range of input power in EH based designs. The output DC voltage and current are evaluated with the input power and is presented in Fig. 13. The DC current and voltage increases with the increase in the input power level (P_{in}) which is expected. It is also seen that the MOS based compensation performs better that the capacitor based compensation in terms of both the voltage and current.

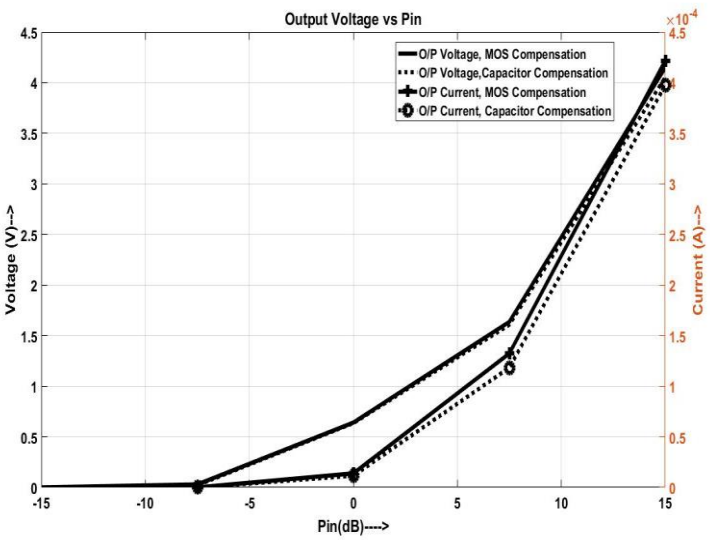

Figure 13: Output DC voltage and current vs P_{in} for both the circuits

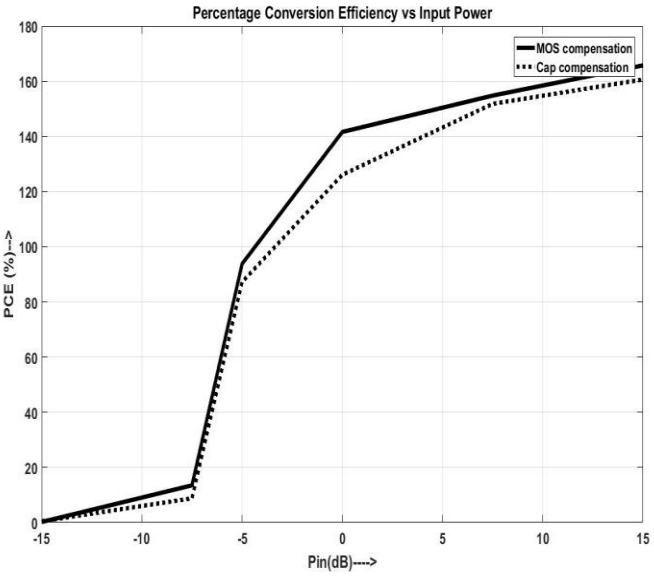

Figure 14: PCE vs P_{in} for both the circuits

It is already stated that the PCE is the most significant performance parameter in an EH rectifier. The PCE of both the circuits presented here are evaluated. At -5dB the PCE obtained are 86% and 92% for the capacitor based compensation and MOS based compensation respectively. The PCE is plotted across P_{in} and is shown in Fig. 14. For higher input power, power gain is also observed. This clearly shows that the design is efficient to be applicable at input low power scenarios. The dynamic power dissipation (DPD) of the circuit with MOS based compensation is plotted across the output voltage at 2dB and -5dB respectively and is

shown in Fig. 15. The instantaneous DPD changes with output voltage.

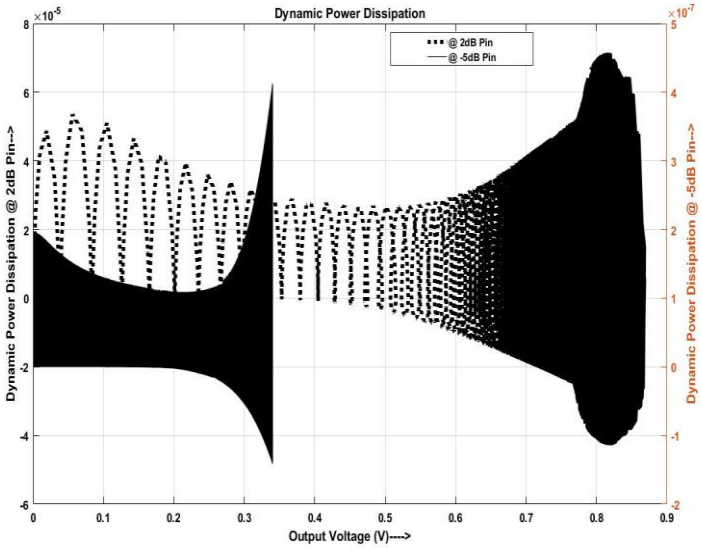

Figure 15: DPD vs Output voltage

The key parameters of both the circuits are presented in Table 2. This shows that the MOS based compensation outperforms the capacitor based compensation except the dynamic power dissipation.

Table 2: Comparative Analysis of both the circuits

Parameters	Capacitor based Compensation		MOS based Compensation	
	@2dB	@-5dB	@2dB	@-5dB
O/P Voltage	816 mV	300mV	820mV	320mV
PCE	100%	86%	120%	92%
DPD	14.97nW	12nW	19.59nW	16.5nW
LP	$20x10^{-51}$W	$20x10^{-51}$W	$6.8x10^{-51}$W	0

A comparative analysis of the presented work is done with few recently reported works. This shows that the designs presented here provides the best in-class efficiency. This is shown in Table 3. In [21], [22] and [23] you will find some other studies about CMOS.

Table 3: Comparative Analysis with recent works

Work	Comparison with the reported works					
	Technology	*Stage*	*Frequency (MHz)*	*Input Power (dbm)*	*Output Voltage (V)*	*Max PCE (%)*
[13]	Schottky Diode	1	868	10	-	48
[14]	Schottky Diode	1	900	-10	0.66	40
[15]	Schottky Diode	2	868	-10	0.649	44
[16]	Schottky Diode in 0.35 µm CMOS	5	900	-14.8	1.5	36
[17]	TSMC 0.18 µm	8	925	-21.2	0.78	43
[4]	0.18 µm CMOS	1, Diff	953	-12.5	0.62	67
[18]	TSMC 90 nm CMOS	5, Diff	868	-17	1.62	40
[19]	65 nm CMOS	5	900	18	6	31
[7]	65 nm CMOS	2	953	-15	0.402	56
[12]	45 nm CMOS	1	953	-2	0.485	80
This work	45 nm CMOS	1	953, 1800	-5	0.3	86
This work	45 nm CMOS	1	953, 1800	-5	0.32	92

4 Conclusion

This paper proposes modification to a TG Dickson based rectifier with two substrate compensation techniques viz. capacitor based compensation and MOS based compensation. The results indicated that both the configurations are capable to function over a wide band of frequencies that covers several commercially available bands. The PCE of 86% and 92% at -5dBm are achieved with capacitor and MOS based techniques respectively, which is significantly high in comparison to the recently reported works. This proves the suitability of both the designs in low power RF energy harvesting to facilitate self-sustainability to a system as part of green communication set-ups. Another achievement of both the designs are that it uses minimum number of transistors as 4 and 5 respectively, hence the designs can be said to be area efficient too. Since the area is directly linked to the cost of production, hence the designs can be stated to be a cost effective one. The DPD and LP are also presented in the Table 2, which shows that the circuits provides a very low DPD and almost negligible LP. A significantly low DPD makes the circuit feasible for power aware implementation. Again a low LP is desired as it indicates lower power loss. The MOS based compensation technique works better in all aspects except the DPD, where the capacitor based

technique performs better. Both the designs can be said to be promising candidate in EH as higher PCE at a low input power is achieved over a wide range of frequencies with optimal number of transistor and low power dissipation. Further medications are to be explored to obtain high PCE at a very low input power. Adaptive frequency operation can be another dimension to make the circuit more versatile.

References:

[1] S. Ulukus, A. Yener, E. Erkip, O. Simeone, M. Zorzi, P. Grover, and K. Huang, '*Energy Harvesting Wireless Communications: A Review of Recent Advances*', IEEE Journal of Selected Areas in Comm., vol.33, no.3, pp-360-381, 2015

[2] S. Sudevalayam and P. Kulkarni., "*Energy harvesting sensor nodes: Survey and implications*", IEEE Comm. Surveys Tutorials, vol.13, no. 3, pp-443–461,2011.

[3] J. Rabaey, M. J. Ammer, J. L. Silva, D. Patel, and S. Roundy. "*PicoRadio Supports Ad Hoc Ultra-Low Power Wireless Networking*", IEEE Computer, vol.33, pp-42–48, 2000.

[4] K. Kotani, A. Sasaki and T. Ito, "*High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs*", IEEE Jornal of Solid-State Circuits, vol. 44, no.11, 2009.

[5] M. L Matia et al, "*A comparision of High-Efficiency UHF RFID Rectifier Using Internal Voltage Compensation and Zero-Threshold-Voltage MOSFETs*", 2014 IEEE 5th Latin American Symposium on Circuits and Systems, 2014.

[6] H. Lin, H. Cao, Z. Chen, W. C. Chan, W. K. Lee and M. Zhang, "*Leakage Current Elimination for Dickson Charge Pump with a Linear Regulator*", ELSEVIER Microelectronics Journal, vol. 64, pp. 29-34, 2017.

[7] M. Taghdosi, L. Albasha, N. A. Quadir, Y. A. Rahama and N. Qaddoumi, "*High Efficiency Energy Harvesters in 65nm Process for Autonomous IoT Sensor Applications*", IEEE Access, vol. 6, pp-2397-2408, 2018.

[8] M. M. Mohamed et al., "*High-Efficiency CMOS RF-to-DC Rectifier Based on Dynamic Threshold Reduction Technique for Wireless Charging Applications*", IEEE Access, vol. 6, Pp-46826-46831, 2018.

[9] M. M. Mansour and H. Kanaya, "*High-Efficient Broadband CPW RF Rectifier for Wireless Energy Harvesting*", IEEE Microwave and Wireless Components Letters, vol: 29 , no: 4 , pp-288-290, 2019.

[10] S. Yuh Lee, Z. Xian Liao and C. Hung Lee, "*Energy-Harvesting Circuits With a High-EfficiencyRectifier and a Low Temperature Coefficient Bandgap Voltage Reference*", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, vol. 27, no. 8, pp-1760-1767, 2019.

[11] T. Oh, O. Hassan, S. Shamsir and S. K. Islam, "*Low-Power RF Energy Harvester Circuit Design for Wearable Medical Applications*", United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), USA, 2019.

[12] M. P. Sarma, K. K. Sarma, N. E Mastorakis, "*Design of a TG Based High Frequency Rectifier at 45 nm for RF Energy Harvesting Application*", 2nd IEEE European Conference on Electrical Engineering and Computer Science (EECS), pp-52-523, Athens, Greece, 20-22 Dec. 2018.

[13] D. Allane, G. A. Vera, Y. Duroc, R. Touhami, and S. Tedjini, ''*Harmonic Power Harvesting System for Passive RFID Sensor Tags*'', IEEE Transaction on Microwave Theory Technology, vol. 64, no. 7, pp. 2347–2356, Jul. 2016.

[14] D. Masotti, A. Costanzo, P. Francia, M. Filippi, and A. Romani, ''*A Load modulated rectifier for RF Micro-power Harvesting with Start-up Strategies*'', IEEE Transaction on Microwave Theory Technology, vol. 62, no. 4, pp. 994–1004, Apr. 2014.

[15] D. Assimonis, S.-N. Daskalakis, and A. Bletsas, ''*Sensitive and Efficient RF Harvesting Supply for Batteryless Backscatter Sensor Networks*'' IEEE Transaction on Microwave Theory Technology, vol. 64, no. 4, pp. 1327–1338, Apr. 2016

[16] J. W. Lee and B. Lee, "*A Long-range UHF-band Passive RFID Tag IC Based on High-Q Design Approach*" IEEE Transactions on Industrial Electronics, vol. 56, no. 7, pp. 2308–2316, Jul. 2009.

[17] C.-Y. Yao and W.-C. Hsia, "*A–21.2 -dBm Dual-channel UHF Passive CMOS RFID Tag Design*", IEEE Transaction on Circuits and Systems I, Reg. Papers, vol. 61, no. 4, pp. 1269–1279, Apr. 2014

[18] M. Stoopman, S. Keyrouz, H. J. Visser, K. Philips, and W. A. Serdijn, "*Co-design of a CMOS Rectifier and Small Loop Antenna for Highly Sensitive RF Energy Harvesters*," IEEE Journal on Solid-State Circuits, vol. 49, no. 3,pp. 622–634, Mar. 2014

[19] C.-H. Tsai, I.-N. Liao, C. Pakasiri, H.-C. Pan, and Y.-J. Wang, "*A Wideband 20 mW UHF Rectifier in CMOS*", IEEE Microwave and Wireless

Component Letters.,vol. 25, no. 6, pp. 388–390, Jun. 2015.
[20] H. Kim and I. Kwon, "*Design of High-Efficiency CMOS Rectifier with Low Reverse Leakage for RF Energy Harvesting*", Electronics Letters, vol. 55 No. 8 pp. 446–448, 2019.
[21] Evandro Bolzan, Eduardo V. V. Cambero, Alfeu J. S. Filho, Ivan R. S. Casella, Carlos E. Capovilla, RF PAD De-Embedding in CMOS Active Cascode Inductor Design, *WSEAS Transactions on Circuits and Systems,* pp.12-18, Vol.17, 2018
[22] Bruno C. Dias, Evandro Bolzan, Jose A. Torrico Altuna, Alfeu J. Sguarezi Filho, Carlos E. Capovilla, Proposal of an ASIC CMOS for Sliding Mode Control of Switched Reluctance Aerogenerators, *WSEAS Transactions on Circuits and Systems,* pp.445-453, Vol.13, 2014
[23] Design of Synchronous Section-Carry Based Carry Lookahead Adders with Improved Figure of Merit, *WSEAS Transactions on Circuits and Systems,* pp.155-164, Volume 15, 2016

Conflicts of Interest

The author(s) declare no potential conflicts of interest concerning the research, authorship, or publication of this article.

Contribution of individual authors to the creation of a scientific article (ghostwriting policy)

The author(s) contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of funding for research presented in a scientific article or scientific article itself

No funding was received for conducting this study.

Creative Commons Attribution License 4.0 (Attribution 4.0 International , CC BY 4.0)