Active Matching Technique with Common-Gate Configuration to Improve Performance of PHEMT Frequency Multipliers

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Abstract: - In this paper, we verify the potentiality of common-gate configuration as an active impedance matching to improve performance of PHEMT frequency multiplier by 4. A 8.87% relative bandwidth at millimeter wave frequencies for frequency multiplier by 4 is achieved by this technique. In this contribution, simulation results show the good impact of this technique on the performance of PHEMT frequency multiplier by 4 especially on the conversion gain and output power.

Key-Words: - Active impedance matching stage, PHEMT technology, frequency multiplier, RF circuits, common-gate configuration, passive elements.

1 Introduction

A primary concern of RF circuits is to insure an impedance matching for the full band of operating frequency. Among the main requirements on the performance of RF circuits are the increasing gain and decreasing of device parasitics. Such requirements are satisfied by impedance matching of the whole device to 50 Ω external impedance with at least 0 dB losses.

Impedance Matching techniques based on passive elements are the most popular in RF circuits. Among the most used are LC-based circuits which are easier to realize for wideband impedance matching at microwave frequencies [1]. However, the big size of the inductor in LC networks stills the major disadvantage in terms of integration on chip because it occupies large circuit areas [2]. The matching circuits based on passive elements are typically limited to applications, i.e. impedance matching requirements change according to the application attended, which require a re-designing of the matching circuit. Thus, the apparition of transistor-based matching circuits has been an excellent solution [3] for obtaining a high integration and flexibility of performance control.

The most well known transistor-based input matching structure is the common-gate configuration. Previously published works have demonstrated that the common-gate configuration is widely used by RF amplifiers and especially low noise amplifiers[4] as it offers the possibility of wide bandwidth, small size and low cost.

As mentioned that this technique is much used by low noise amplifiers (LNA), in this present work, we will verify the potentiality of this matching technique for other circuits such as active frequency multipliers.

Common-gate configuration is chosen for obtaining input matching of the frequency multiplier using 0.15µm GaAs PHEMT process from UMS foundry in order to improve its output power and conversion gain.

This paper is organized as follows: in Section II, we will demonstrate in analysis and simulation the PHEMT common-gate configuration. In Section III, we will present the frequency multiplier by 4 with common-gate input stage in order to verify the potentiality of this technique on multiplier

performance. Finally, we will finish by a conclusion in Section VI.

2 PHEMT Common-Gate Configuration

The operation principle of MESFETs common-gate configuration as an active matching stage has been detailed by a number of researchers [5]. In this work, the common-gate configuration based on PHEMT device will be employed to verify the potentiality of this configuration as an input matching stage on frequency multiplier input return-loss performance without the use of passive matching components. Besides, we verify the technique impact on multiplier performance, namely output power, conversion gain and chip size.
Figure 1 shows the PHEMT common-gate configuration and its small signal equivalent circuit. The PHEMT common-gate provides an electronically tunable active impedance matching for optimum return-loss. At frequencies reasonably lower than the transition frequency of the PHEMT device, F_T, the input impedance can be expressed by the formula (1) [6]:

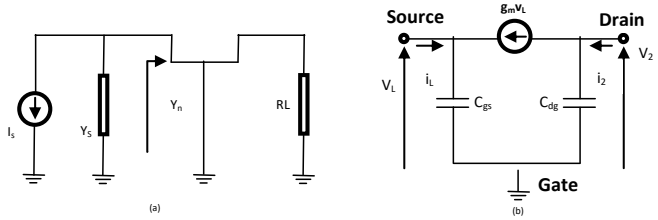

Fig.1. (a) Common-gate - (b) Small signal equivalent circuit

$$Zin \approx rs + \frac{1}{g_m(PHEMT)} \qquad (1)$$

Where rs is the PHEMT source resistance and gm is the transconductance. From the above formula, we can deduce that the input impedance of the common-gate stage is inversely proportional to the transconductance of the PHEMT device.
Despite the simplicity of the common-gate structure, it can offer a good impedance matching. Besides this major advantage, it is considered as an excellent choice for a wide-bandwidth system because the device transconductance is not much affected by the frequency. This configuration also allows a broadband impedance matching from DC to microwave frequencies and gain performance due to the absence of miller capacitance multiplication at the input [6].

Thus, the input impedance can be electronically tuned for optimum return-loss by adjusting the PHEMT bias.
A near ideal match to make Zin ≈ 50 Ω would require a PHEMT transconductance ≈ 20 mS
PHEMT size is 1*45µm^2 for the input common-gate configuration. An inductor about of 1.46 nH is used to insure the device bias at Vds=3 V and rs ≈ 0.5 Ω. The simulation results are obtained for a frequency of 15 GHz.
Figure 2 shows the input impedance for the common-gate stage for a frequency range from 10 GHz to 20 GHz.

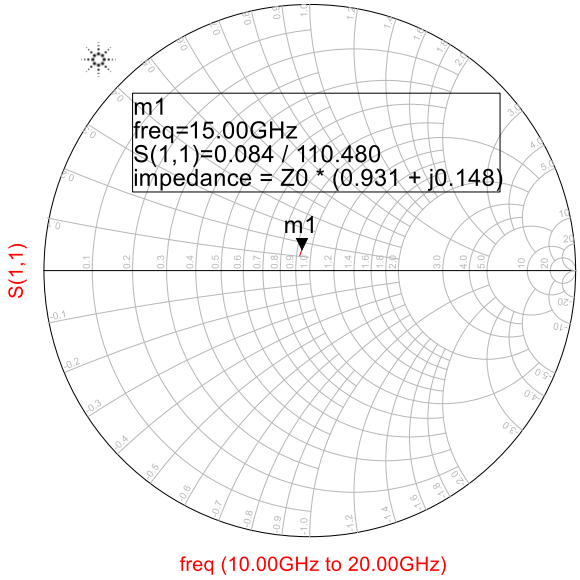

Fig.2. Input impedance for common-gate structure

By adjusting the device bias at Vds= 3 V and its size to1*45µm^2, which implies a transconductance value of 20 mS, we can deduce from the figure above that the input impedance is almost equal to 50 Ω. Therefore, it is the value sought by this configuration.

3 Frequency multiplier by 4 with common gate configuration

In order to generate a signal in the millimeter bands around 60 GHz, a multiplication chain by 4 has been designed. This chain consists of three blocks: a harmonic generator to which has been added a two pole high-pass filter [7] to push through the harmonic of interest (4th harmonic) and reject the other unwanted signals, followed by a buffer amplifier at the output to improve the power level of the desired harmonic [8]. From simulation results, we found that the multiplication chain has a

conversion loss, which is insufficient to have better performances. In this regard, several techniques for improving the conversion gain exist, among which the common-gate configuration is providing an active impedance matching.

We recall that the input frequency is 15 GHz to generate a signal around 60 GHz at the output.

Figure 3 shows the power levels of different harmonics of the unmatched frequency multiplier by 4.

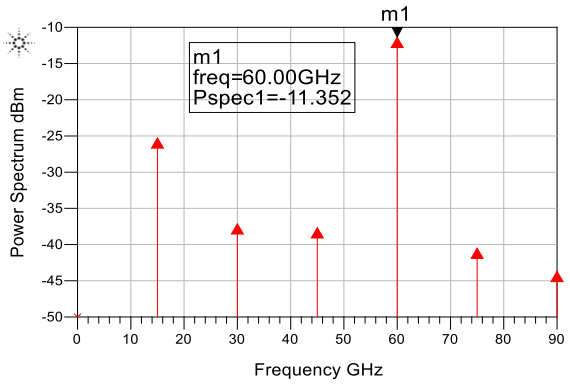

Fig.3. Power levels of different harmonics of unmached frequency multiplier by 4

From figure 3, it can be seen that the power level of the fourth harmonic (60 GHz) reaches a value of -11.35 dBm. Since the power level applied to the chain input is about 0 dBm, the multiplication chain by 4 has a conversion gain of about -11 dB. Therefore, this value indicates that the multiplication chain has a conversion loss that will not give better performance of the chain. Therefore the insertion of the common-gate configuration to the input of the chain is mandatory.

Figure 4 shows the input return-loss for the multiplication chain.

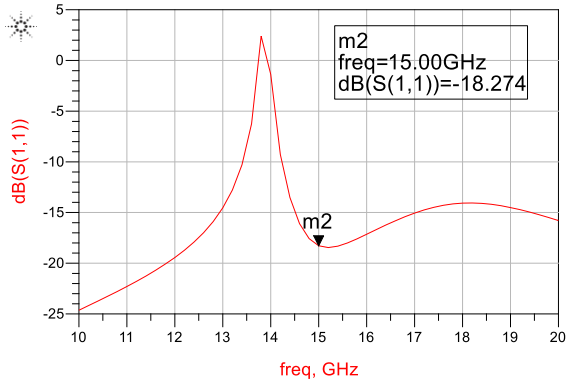

Fig.4. Input return-loss for the chain of multiplication

From figure 4, we can see that the reflection coefficient around 15 GHz has a value of -20 dB. This value verifies the input impedance matching of the multiplication chain. The new performance of matched frequency multiplier by 4 is presented below.

Figure 5 illustates the power evolution of the fourth harmonic of as a function of the input/output frequency of matched multiplier by 4.

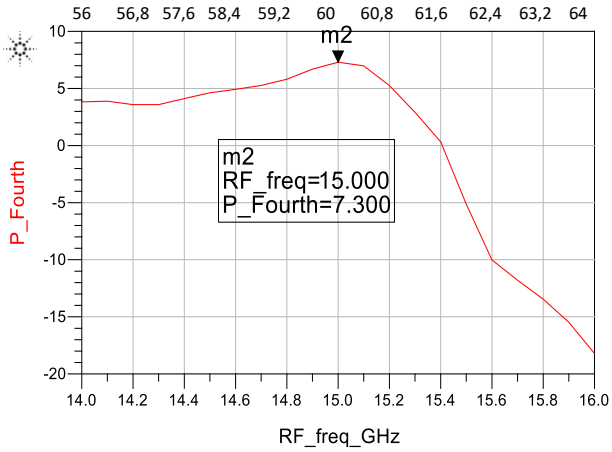

Fig.5. Power evolution of the fourth harmonic as a function of the input/output frequency of mached frequency multiplier

We can see clearly after the insertion of the common-gate configuration that the power of the fourth harmonic around 60 GHz of about 7.3 dBm, which proves the good impact of the configuration used as an input impedance matching on the frequency multiplier performance.
Conversion gain evolution as a function of the input/output frequency after the insertion of common-gate circuit is shown in figure 6.

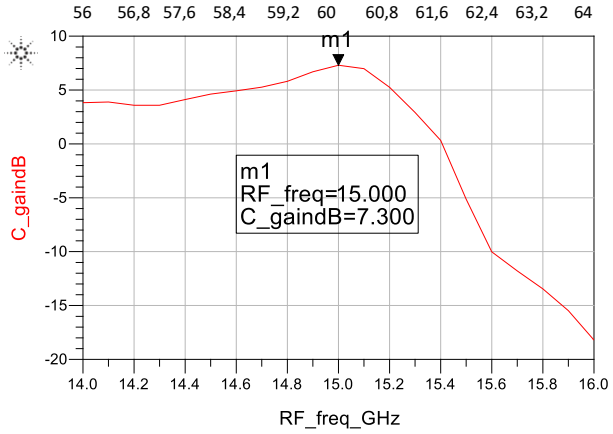

Fig.6. Power evolution of conversion gain a function of frequency of mached frequency multiplier

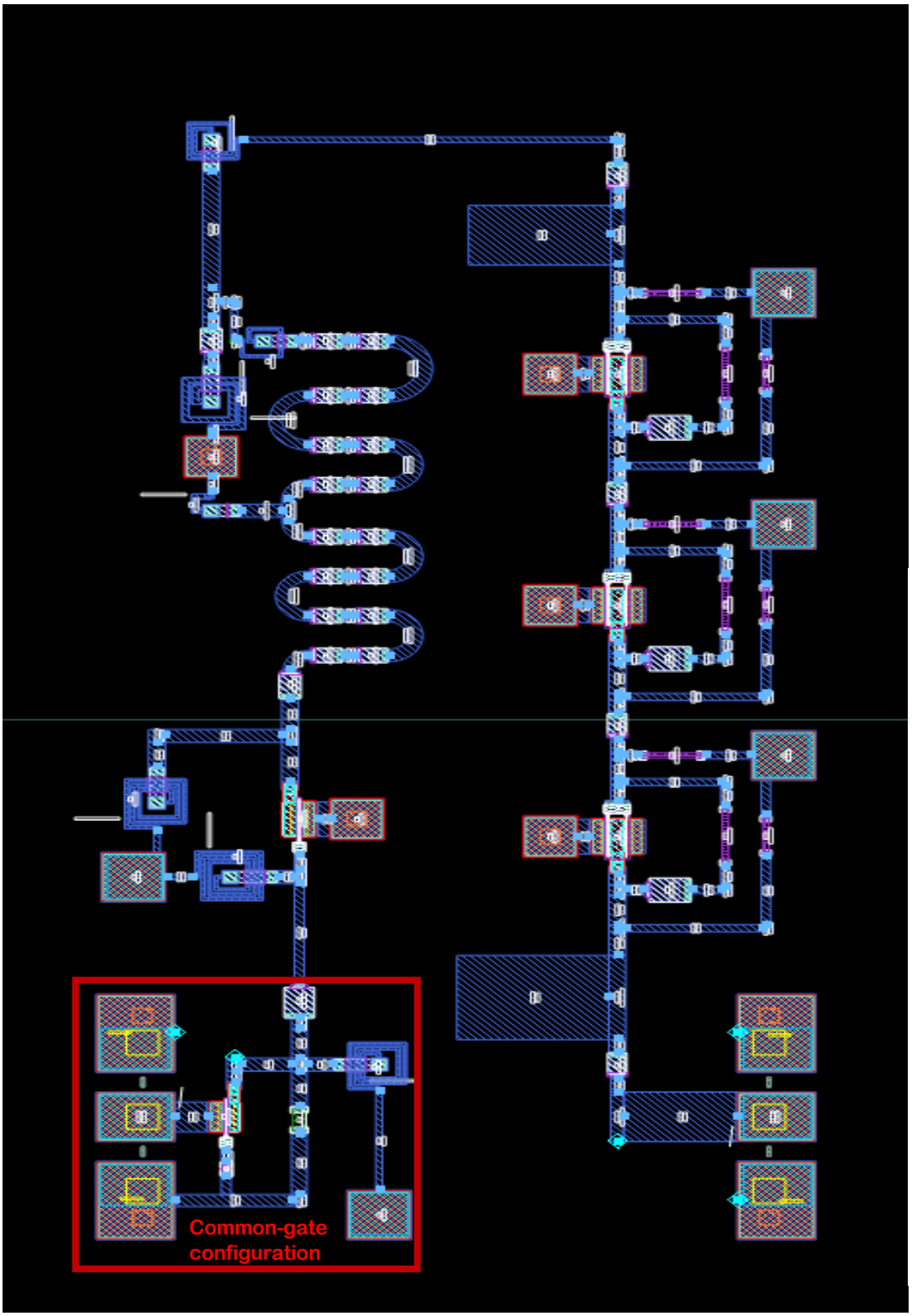

Fig.7. Layout of frequency multiplier by 4 with common-gate configuration

The evolution of conversion gain versus the input / output frequency is shown in figure 6. We observe from the gain curve that around 15 GHz (60 GHz), conversion gain has a value of 7.3 dB. We can also see that the bandwidth at 3dB of this multiplier is between 56 GHz and 61.2 GHz.

According to the obtained results, the potentiality of the common-gate configuration is verified on the multiplier performance in terms of the conversion gain and output power. Furthermore, a relative bandwidth of 8.87% at millimeter frequencies has been achieved through this technique.

The frequency multiplier by 4 is implemented on a 100 μm-thick GaAs substrate. This is a multilayer technology. The total number of layers used in PH15 from UMS foundry and used in this circuit is 16 layers. Figure 7 shows the layout of the frequency multiplier by 4 with the active impedance matching circuit. The whole circuit measures 2.88 mm^2 whose 0.27 mm^2 is the size of common-gate configuration.

4 Conclusion

The potentiality of common-gate configuration as an active input impedance matching to improve performance of PHEMT frequency multiplier by 4 has been verified in this paper. Simulation results demonstrate a minimum input return-loss of frequency multiplier thanks to electronic tunability of the used configuration. Besides, this technique has a good impact on the conversion gain, output power, and bandwidth.

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