Simulation and design of an integrated planar inductor using fabrication technology

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Abstract: - This paper presents the conceptions and characterization of integrated planar inductor containing magnetic layers. A novel approach has been used to perform planar magnetic devices by using physical model for integrated planar inductor for 35 μm fabrication technology. According to CMP, C35B3C0 fabrication technology provides three metallic layers; therefore, there is no need to use poly-silicon or diffused underpasses. The metallic -1 layer is used for underpasses. Operation voltage of IC's (Integrated Circuits) fabricated with this technology is 2.5 to 3.6 *V*. The physical model of the integrated planar inductor is designed using "The Electric VLSI Design". The purpose of this paper is to present and compare the results of total inductivity of inductors with different number of turns. Grover's expressions are used for calculations. Simulated results for parasitic and resistance capacities for our model are presented in this paper, too.

Key-Words: CMOS proces, Planar inductor, Self-inductance, Mutual-inductance

1 Introduction

Passive components comprise the majority of chip area occupied by monolithic converters, even when the components are optimized for minimum area [1]. System-In-Package applications are facing miniaturization issues due to passive components size. The push towards higher and higher frequencies has generated much interest in novel structures for planar inductors. Therefore by increasing the switching frequency of DC-DC converters in the 10 MHz and 100 MHz frequency range, the size of filter passive components is dramatically reduced. Thus, the passive area of integration drops below the 10 mm^2 range [2]. Planar devices offer several advantages. Some of these are better thermal management, low profile, and higher power densities. Although research on planar inductors is concentrated on integrating air core inductors on silicon wafers [3,4,5], the application of substrates to planar inductors enables to increase the inductance without increasing the stray capacitance between the coils and the ground plane. In our application, surface area is the key point of designing the inductor since the aim is to integrate the inductor on the top of a SMPS die in a surface area of $3mm^2$. We proposed a figure of merit ($MHz/m\Omega.mm^2$) to evaluate our inductor performance targeting the DC/DC converter application. First, we describe the design issue based on Flux2D simulator. In the second part, fabrication process using electroplating technique will be detailed. And then, simulation results and process fabricated inductors are shown in the last section.

Inductors have a substantial importance on cell circuits such as: oscillators, filters, signal amplifiers, power amplifiers, low-noise amplifiers, etc. As those cells constitute highly integrated and analog circuits, then need to design very-large-scale integrated inductors is increased. Designing very-large-scaled integrated inductors is more challenging than other passive components.

There are several different integrated inductors layouts. The rectangular spiral, hexagonal spiral and circular spiral respectively are mostly used layouts. The spiral planar inductor can be fabricated only by using two or more metallic layers fabrication processes, because one of layers is used for underpass. In this paper, rectangular spiral layout is used to design four winding planar inductor.

2 Fabrication process

Fabrication process is based on 1P3m standard – one polysilic layer (1P) and three metallic layers (3M). According to X-FAB fabrication process datasheet, thickness of metallic layer number 2 and number 3 i s 1 µm, whereas thickness of metallic layer number 1 is 0,58 µm. Sheet resistance of first metallic layer is 0,090 Ω, and the sheet resistance of second and third metallic layers is 0,045 Ω. Capacitance for micrometer square of isolated layer between metal-2 and metal-3 is 1,25 fF/µm^2, whereas perimeter capacitance is 0,111 fF/µm.

According to design roles [4], minimal width of metallic layer Metal-1, Via-1 and Via-2 is 0,5 µm, and distance between conductive traces is 0,45 µm. Width of the conductive traces on layers Metal-2 and Metal-3 is 0,6 µm, and distance between these traces is 0,5/0,6 µm. XU035 [4], offers extra power conductive connections, where width of these conductive connections is 3,0 µm and distance between them is 2,5 µm. Figure 1 shows cross-section view of layers of 0,35 µm fabrication process with a polysilic layer and three metallic layers – 1P3M.

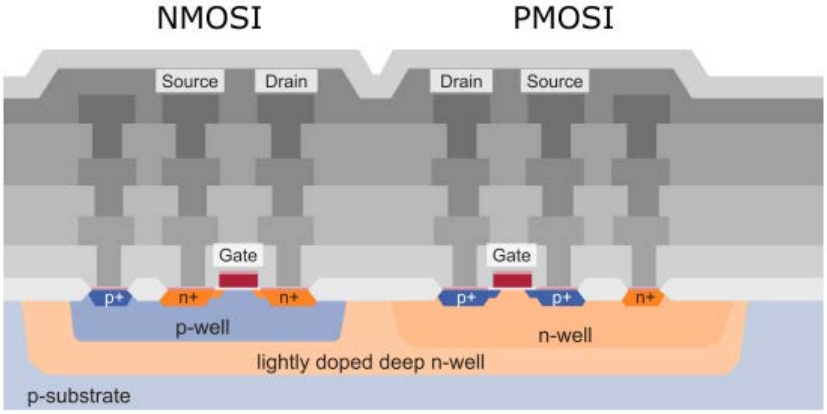


Fig. 1. Layers alignment of 0,35 µm 1P3M fabrication process [4].

3 Design of planar inductor

The inductance value of the spiral inductors at the HF range can be determined using the quasi-static method proposed by Greenhouse [14] with a good level of accuracy. In contrast to the helical windings of conventional magnetic devices, the windings of planar transformers and inductors are located on flat surfaces extending outward from the core center leg. Magnetic cores used with planar devices have a different shape than conventional cores used with helical windings. Compared to a conventional magnetic core of equal core volume, devices built with optimized planar magnetic cores usually exhibit: Significantly reduced height (low profile); Greater surface area, resulting in improved heat dissipation capability; Greater magnetic cross-section area; enabling fewer turns; Smaller winding area; Winding structure facilitates interleaving; Lower leakage inductance resulting from fewer turns and interleaved windings; Less AC winding resistance; Excellent reproducibility, enabled by winding structure. A magnetic field is actually stored energy. The physical distribution of the magnetic field represents the distribution of this energy. Understanding the properties of the magnetic field not only reveals the amount of stored energy and its locations, it also reveals how and where this energy is coupled to various electrical circuit elements. Inductance is simply an electrical circuit concept which enables the circuit designer to predict and quantify the effects of magnetically stored energy in the electrical circuit. Applying the basic principles of magnetic field behavior (discussed in earlier seminars) to planar magnetic structures enables us to optimize the design and predict the magnitude of parasitic circuit elements such as leakage inductance. The magnetic field also is the dominant influence on the distribution of high frequency AC current in the windings, thereby determining AC winding losses.

Figure 2 shows top view of planar inductor. Four windings rectangular spiral layout is used for this design. As shown, distance between turns is 1µm, and width of conductive traces is 1 µm. These sizing parameters are consistent with design rules listed on datasheet [4]. Turns are layout on third (upper) metallic layer. Middle (second) metallic layer is used for underpass – connecting the end of inner turn with node number 2. As shown in figure 2, metallic traces layout on second metallic layer is of 9 µm length. Dimensions with few decimals shown in figure 2, are because of grid stepping size of design software. Total size of this inductive coil is 23 µm x 18 µm. Figure 3 shows three-dimension view of the planar inductive coil.

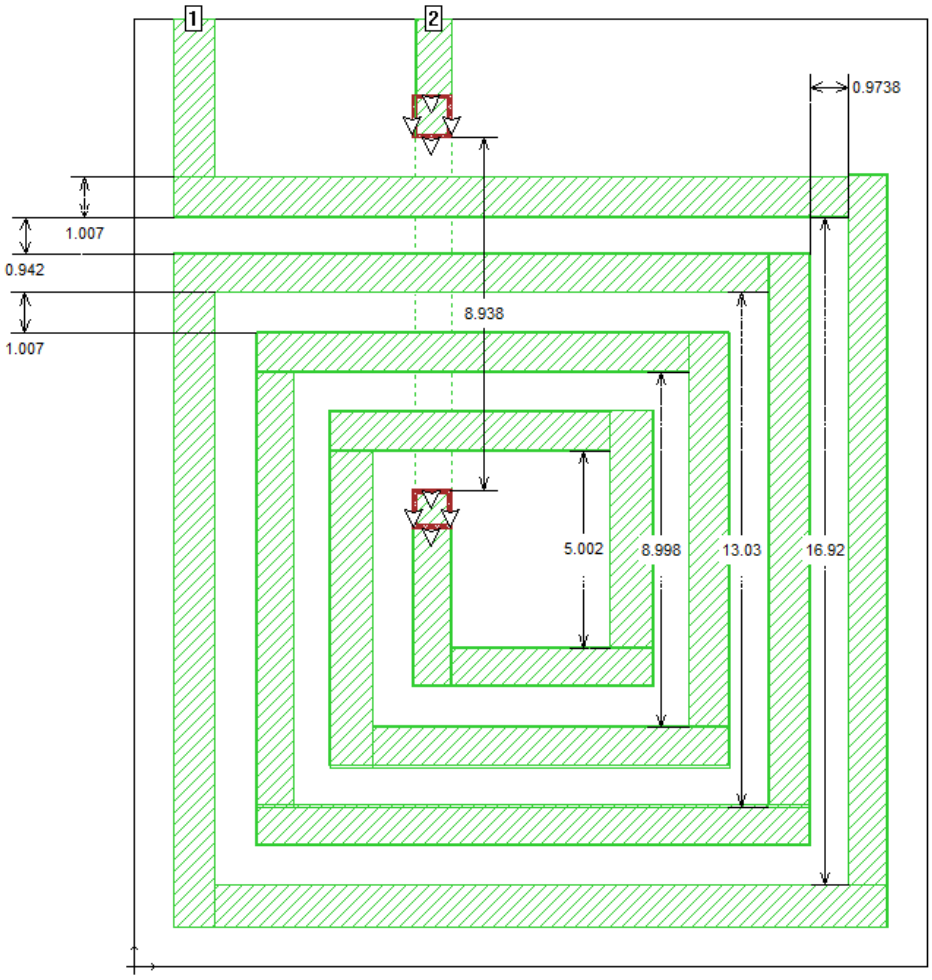


Fig. 2. Top view (with dimensions) of planar inductor – third metallic layer.

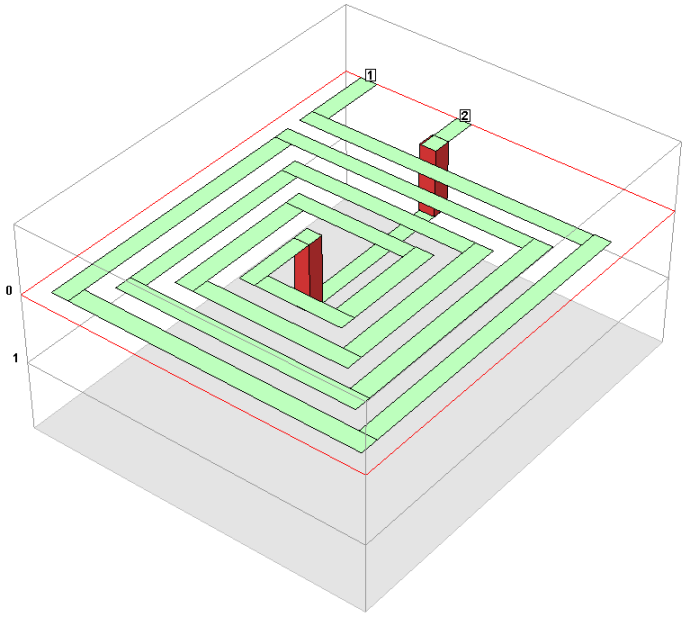


Fig. 3. 3D view of rectangular planar inductor.

4 Results

a) Calculation of series resistance

For uniformly distributed direct current on rectangular cross-section view conductor, with length L, resistivity ρ, resistance is given [2] by:

$$R_{DC} = \rho \frac{L}{Wt} \quad (1)$$

As resistance of metallic layers are expressed in terms of sheet resistance on da tasheet [4], then resistance calculation is given by:

$$R_{DC} = R_S \frac{L}{W} \quad (2)$$

According to datasheet [4], sheet resistance of second and third (metal-2 and metal-3) layers is 0.045. Length of each segment of coil on third metallic layer are as following: 18, 17, 17, 1 6, 15, 14, 14, 11, 11, 10, 9, 8, 7, 6, 5, 5, 4 [μm], and length of segments on second metallic layer are: 9, 3 [μm]. Series resistance of coil is:

$$R_{DC} = 0.045 \cdot (18+17+17+16+15+14+14+11+11+10+9+8+7+6+5+5+4+9+3) = 0.045 \cdot 199 = 8.955\Omega$$

Calculated resistance is valid for direct currents and low frequency currents. At increasing frequencies, the current density becomes more and more nonuniform due to high frequency effekt in metalls [3]. Resistance of rectangular cross-section conductors on hi gh frequencies, based on di rect-current resistance is given by [3]:

$$R_{AC} = R_{DC}\left[1 + \left(\frac{f}{f_l}\right)^2 + \left(\frac{f}{f_u}\right)^5\right]^{\frac{1}{10}} \quad (3)$$

$$f_l = \frac{\pi\rho}{2\mu_r\mu_0 Wt} = \frac{\pi R_S}{2\mu_r\mu_0 W} \quad (4)$$

$$f_u = \frac{\pi^2 R_S}{\mu_r\mu_0}\left[K\sqrt{1-\frac{t^2}{W^2}}\right]^{-2} \quad (5)$$

where W and t are dimensions of rectangular conductur cross-section, μ is magnetic permeability (μ_r is taken 1), f_l and f_u are low and high cut-off frequencies, and K is first order elliptic integral and is given by

$$K(x) = \int_0^{\frac{\pi}{2}} \frac{1}{\sqrt{1-x^2\sin^2\varphi}} d\varphi \text{ , or}$$

$$K(x) = \int_0^1 \frac{1}{\sqrt{(1-t^2)(1-xt^2)}} dt \quad (6)$$

Taking $W = 1\ [\mu m]$, $t = 1[\mu m]$, $R_S = 0.045$, $\mu_r = 1.00$ and $x = [0,\ 0.2,\ 0.4,\ 0.6,\ 0.8]$, low cut-off frequency is $f_l = 5.62\ GHz$, and high cut-off frequency for different values of K parameter are listed on table 1. Resistance of coil on high frequencies – from 0.5 G Hz to 10 G Hz – for different values of K parameter are listed on table 2 and shown in figure 4.

Table 1. Calculated high cut-off frequencies depending on the first order elliptic integral.

x=0	K=1.57	$f_u = 49.8\ GHz$
x=0.2	K=1.66	$f_u = 44.56\ GHz$
x=0.4	K=1.77	$f_u = 39.2\ GHz$
x=0.6	K=1.95	$f_u = 32.3\ GHz$
x=0.8	K=2.26	$f_u = 24\ GHz$

Table 2: Calculated resistance of inductor on high frequencies for different values of K parameter.

		0.5 [GHz]	1 [GHz]	1.5 [GHz]	2 [GHz]	2.5 [GHz]	3 [GHz]	4 [GHz]	5 [GHz]	6 [GHz]	7 [GHz]	8 [GHz]	9 [GHz]	10 [GHz]
x=0.0	K=1.57	8.9571	8.9783	9.0126	9.0587	9.1150	9.1798	9.3284	9.4927	9.6639	9.8364	10.0065	10.1723	10.3327
x=0.2	K=1.66	8.9572	8.9784	9.0128	9.0590	9.1155	9.1805	9.3294	9.4940	9.6656	9.8383	10.0086	10.1746	10.3352
x=0.4	K=1.77	8.9572	8.9785	9.0130	9.0595	9.1162	9.1814	9.3309	9.4959	9.6679	9.8410	10.0117	10.1780	10.3388
x=0.6	K=1.95	8.9573	8.9788	9.0136	9.0604	9.1176	9.1834	9.3339	9.5000	9.6729	9.8468	10.0181	10.1850	10.3463

x=0.8	K=2.26	8.9574	8.9795	9.0151	9.0629	9.1213	9.1883	9.3415	9.5101	9.6852	9.8611	10.0341	10.2024	10.3650

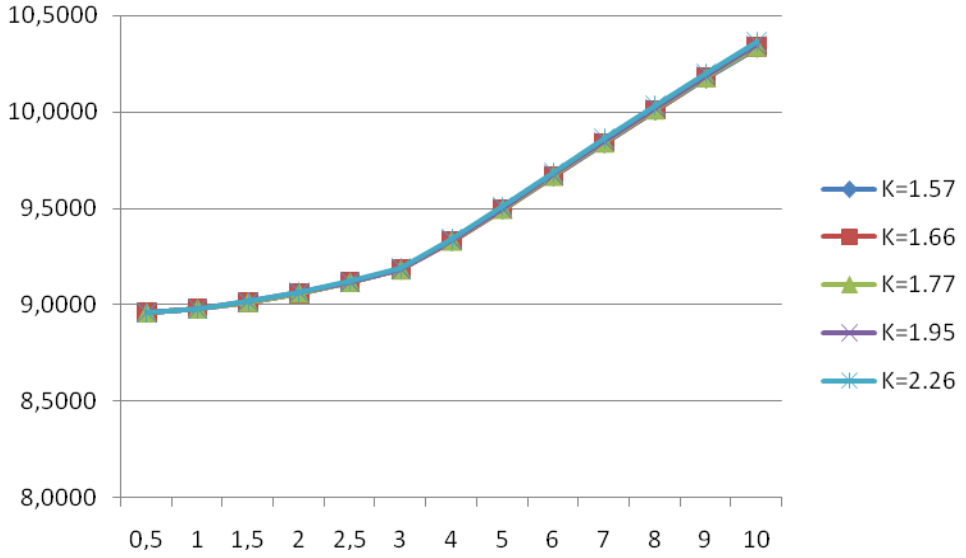


Fig. 4. Calculated resistance depending on the frequency for different values of *K* parameter.

b) Self-inductance calculations

The calculation of inductance, historically important in power engineering applications, has recently grown new interest due to the development of contactless power transfer systems [1]. In particular, planar inductors are used as intermediate resonators between the transmitting and receiving coils to improve the efficiency of the wireless power transfer, channeling the magnetic field in resonance condition. Self-inductance for a straight conductor according to Grover's equations extracted from [5], who further developed the concepts in [7] under a new comprehensive theory of inductance known as the theory of partial inductance [2] is

$$L = 0.002l\left\{ln\left[\frac{2l}{GMD}\right] - 1.25 + \frac{AMD}{l} + \frac{\mu T}{4}\right\} \quad (7)$$

where L is self-inductance [μH], l is length of conductor [cm], and GMD and AMD are geometric and arithmetic mean distance of cross-sections, respectively, μ is magnetic permeability of conductor, and T is frequency-correction parameter.
The total inductance of a loop is then equal to the sum of the partial self-inductances of each straight element plus all the partial mutual inductances between the elements. There is no unique choice of the elements into which a circuit is divided.
For thin-film inductors, according to (5) GMD is 0.2232(a+b) and AMD is $\frac{a+b}{3}$. So,

$$L = 0.002l\left\{ln\left[\frac{2l}{0.2232(W+t)}\right] - 1.25 + \frac{W+t}{3l} + \frac{\mu T}{4}\right\}$$

$$L = 0.002l\left\{\ln\left(\frac{2l}{W+t}\right) - \ln(0.2232) - 1.25 + \frac{W+t}{3l} + \frac{\mu T}{4}\right\} \quad (8)$$

$$L = 0.002l\left\{\ln\left(\frac{2l}{W+t}\right) - 0.25049 + \frac{W+t}{3l} + \frac{\mu T}{4}\right\}$$

where W and t are dimensions of cross-section for rectangular conductor. For near-direct-currents, in which magnetic permeability is 1, according to [5], expression for self-inductivity takes form

$$L = 0.002l\left\{ln\left(\frac{2l}{W+t}\right) + 0.50049 + \frac{W+t}{3l}\right\} \quad (9)$$

Calculated self-inductance of each segment of inductor is listed on table 3, and the total self-inductivity of inductor is 12.0154 *nH*.

Table 3: Calculated self-inductance of each segment of inductor.

	Length (μm)	Self-inductance (nH)
L1	18	1.2340
L2	17	1.1468
L3	17	1.1468
L4	16	1.0607
L5	15	0.9759
L6	14	0.8924
L7	14	0.8924
L8	11	0.6510
L9	11	0.6510
L10	10	0.5739
L11	9	0.4989
L12	8	0.4261
L13	7	0.3558
L14	6	0.2884
L15	5	0.2243
L16	5	0.2243
L17	4	0.1643
L18	9	0.4989
L19	3	0.1093

c) Mutual-inductance calculations

The mutual-inductance between two parallel conductors is a function of the length of the conductors and of the geometric mean distance. In general,

$$M = 0.2lQ \tag{10}$$

where M is the mutual-inductance in nH, l is the length of conductor in mm, and Q is the mutual-inductance parameter, calculated from the equation

$$Q = ln\left\{\frac{l}{GMD} + \sqrt{1+\frac{l^2}{GMD^2}}\right\} - \sqrt{1+\frac{GMD^2}{l^2}} + \frac{GMD}{l} \tag{11}$$

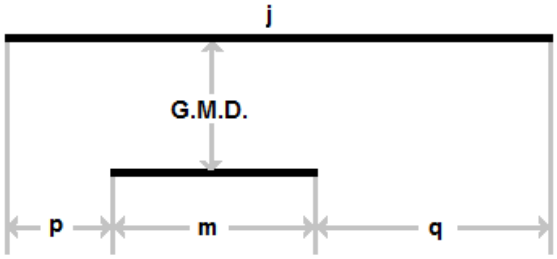
$$GMD = d \cdot \exp\left[-\left(\frac{w^2}{12d^2} + \frac{w^4}{60d^4} + \frac{w^6}{168d^6} + \frac{w^8}{360d^8} + \frac{w^{10}}{660d^{10}}\right)\right] \tag{12}$$

where w is the track width and d is distance between track centers [5]. Whereas, according to [5], mutual-inductance of two different length traces, in case of $p = q$ is

$$M_{j,m} = M_{m+p} - M_p \tag{13}$$

and in case of $p = 0$ is

$$2M_{j,m} = (M_j + M_m) - M_q \tag{14}$$



General expression of total inductance of inductor is given by $L_T = L_0 + \sum M$, where L_T is the total inductance, L_0 is the total self-inductance, and $\sum M$ is total mutual-inductance. In case of parallel conductors where current flows in positive direction and the others where current flows in negative direction, the total inductance is expressed by $L_T = L_0 + M_+ - M_-$, where M_+ is the total positive mutual-inductance, and M_- is total negative mutual-inductance.

Calculated positive and negative mutual-inductance of each segment is listed on table 4. Calculated total inductance value of designed inductor is 12,0745 nH. As noticed, total mutual-inductance has no any large effect on calculated total self-inductance. Resulting S-parameters of 0.1 GHz up to 10 GHz frequency range are shown in figure 6.

Table 4: Calculated positive and negative mutual-self inductance of each segment of inductor.

	pH		
	M+	M-	M+ - M-
M1	11.8972	4.6084	7.2888
M5	12.5453	4.6441	7.9012
M9	9.8593	4.2785	5.5808
M13	6.6882	3.0302	3.6580
M15	1.5937	2.7990	-1.2053
M11	3.3712	3.5537	-0.1825
M7	10.4877	4.9319	5.5558
M3	7.6161	5.2763	2.3398
M2	10.3822	5.5288	4.8534
M6	11.3050	3.6674	7.6376
M10	8.7683	3.1602	5.6081
M14	4.9345	3.6212	1.3133
M16	2.9726	2.6138	0.3588
M12	6.2448	3.7179	2.5269
M8	8.0937	3.6813	4.4124
M4	7.4563	5.9646	1.4917
ΣM	124.2161	65.0773	59.1388

Fig. 5. Two different length parallel conductors.

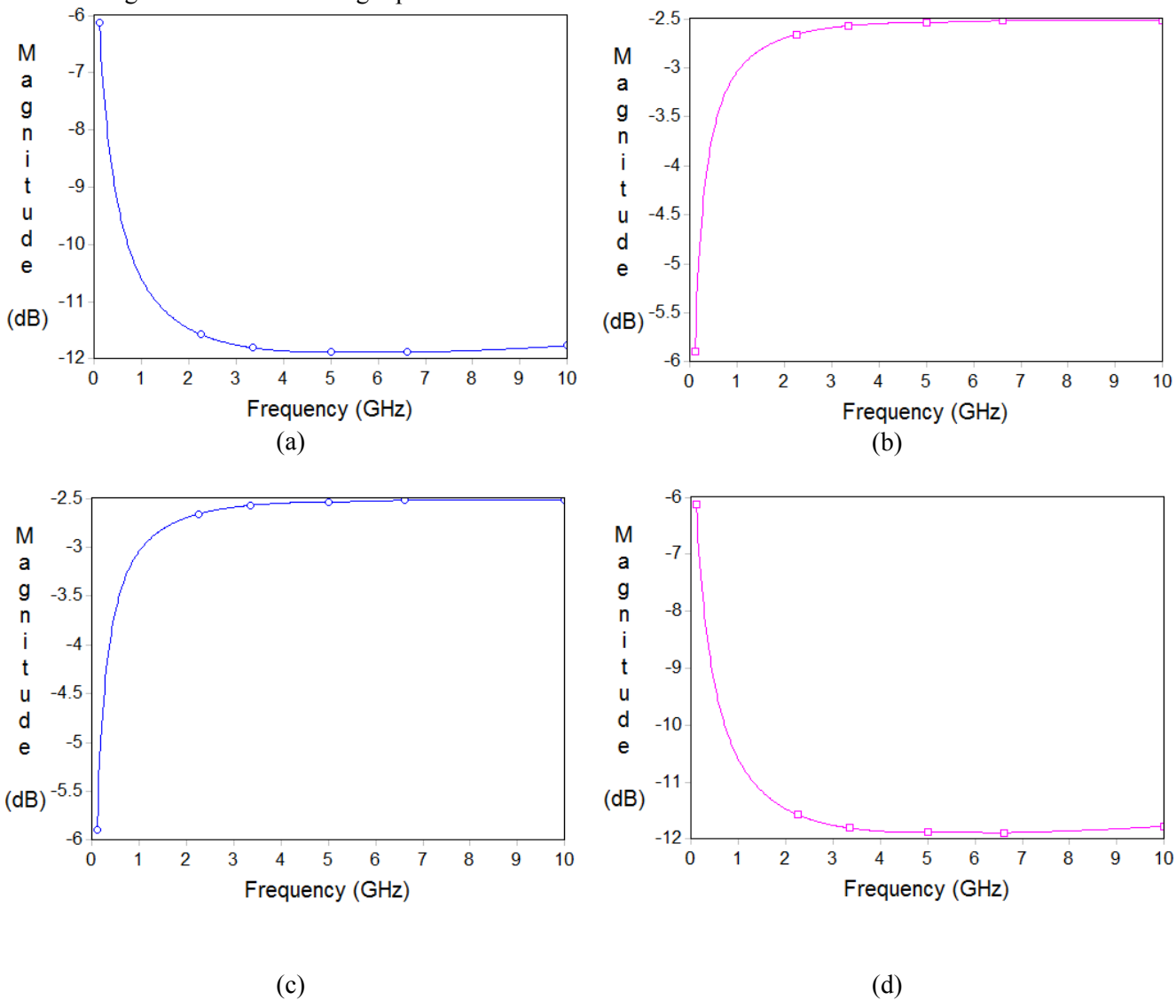


Fig. 6. S-parameters of inductor on frequency range 0.1 GHz – 10 GHz.
(a) the port - 1 voltage reflection coefficient, S_{11}; (b) the reverse voltage gain, S_{12}; (c) the forward voltage gain, S_{21}; (d) the output port voltage reflection coefficient, S_{22}.

5 Conclusions

An analytical and simulation procedure and design for the determination of the inductance of planar integrated inductors is presented in this paper. The inductor is partitioned into a number of parts, each with the shape of a parallelogram. The procedure is based on the partial inductance concept and consists in determining the partial self-inductance of each part and the partial mutual inductance between any two parts of the inductor. The partial self-inductance expression of a thin parallelogram is obtained in closed-form; as regards the partial mutual inductance calculations, the thin parallelograms are represented by segments, and the partial mutual inductances between filaments in any relative position are calculated. The comparison between analytical predictions and graphical form shows a very good agreement.

After that, design, size and calculations results are represented for rectangular planar inductor. Size of the four windings planar inductor is 23 μmx18 μm. This inductor is characterized by 8,59 Ω direct-current resistance and it's increased by increasing the frequency. This is caused by skin-effect. Total calculated inductance of the designed planar inductor is 12,0745 *nH*, which is not very high value, but as this is a very-large-scale integrated inductor, wiring a series of such inductors is possible to gain higher total inductance value.

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