Design and Performance Evaluation of a Buck–Boost Converter for DC Voltage Regulation

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Abstract: - This paper presents the design, modeling, and simulation of a non-inverting buck–boost DC–DC converter based on specified operating conditions, including an input voltage of 12 V, an output voltage of 42 V, a load power of 21 W, and a switching frequency of 200 kHz. Theoretical analysis is performed to determine the duty cycle, inductor value, capacitor size, and expected steady-state waveforms under continuous conduction mode. The converter is then implemented and simulated in MATLAB/Simulink using ideal switching and passive components. The simulated inductor voltage, inductor current, switch current, diode current, capacitor current, and output voltage waveforms are compared with analytically derived theoretical waveforms to validate the model. Results show strong agreement between theory and simulation, demonstrating the accuracy of the derived component values and confirming proper buck–boost operation. This work provides a complete workflow—from analytical design to simulation validation—serving as a foundational study for further development of controlled DC-DC converter systems.

Key-words: - Buck–Boost Converter, MATLAB/Simulink, DC–DC Conversion, PWM Control, Power Electronics, Voltage Regulation.

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1 Introduction

DC–DC converters play a critical role in modern power electronic systems by enabling efficient voltage regulation and power processing across a wide range of applications. These include renewable energy interfaces, electric vehicles, portable electronics, embedded systems, and industrial power supplies. Among various converter topologies, the buck–boost converter offers a unique advantage by providing both step-up and step-down voltage capability using a single switching device and passive components. This makes it highly suitable for systems where the input voltage varies widely or must be regulated to a fixed level despite fluctuations.

The buck–boost converter operates by alternately storing energy in an inductor during the switch ON interval and releasing this energy to the load during the OFF interval. Its dynamic behavior, efficiency, and output quality depend strongly on properly selected design parameters such as duty cycle, inductance, capacitance, switching frequency, and load resistance. Therefore, accurate theoretical analysis and simulation are essential to ensure correct operation prior to hardware implementation.

In this work, a buck–boost converter is designed according to a given specification: an input voltage of 12 V, a desired output voltage of 42 V, a load power of 21 W, an inductor ripple of 1.8 A, and a switching frequency of 200 kHz. Theoretical calculations are carried out to determine the required duty ratio, inductor value, capacitor value, and expected steady-state waveforms under continuous conduction mode (CCM). The converter is then implemented in MATLAB/Simulink using ideal switching devices and passive components. The simulated waveforms—including inductor voltage, inductor current, switch and diode currents, capacitor current, and output voltage—are compared with analytically derived theoretical waveforms to validate the design.

This study provides a complete design-to-simulation workflow for a buck–boost DC–DC converter, offering insights into its operation, steady-state characteristics, and waveform behavior. The results demonstrate close agreement between theoretical predictions and Simulink outputs, confirming the correctness of the model. The work also forms the basis for future developments such as closed-loop control, non-ideal component modeling, and hardware realization.

2 Theoretical Background

2.1 Buck–Boost Converter Operation

When the switch is ON, the diode is reverse-biased. The inductor is connected to the 12 V input and stores energy. The inductor current increases linearly. The load is supplied only by the output capacitor. When the switch is OFF, the diode conducts. The inductor releases its stored energy to the output capacitor and the load. The inductor voltage becomes negative because the output voltage (42 V) is greater than the input. The inductor current decreases linearly.

For the given design, the inductor current does not fall to zero. It varies between approximately 0.85 A and 2.65 A (1.8 A peak-to-peak ripple), confirming CCM operation.

2.2 Voltage Conversion Ratio

The output voltage of an inverting buck–boost converter is given by:

$$V_o = -\frac{D}{1-D}V_{in}$$

Using the given values $V_{in} = 12\ \text{V}$ and $V_o = 42\ \text{V}$, the required duty cycle is:

$$D = \frac{42}{42+12} \approx 0.78$$

This duty cycle ensures the converter boosts 12 V up to 42 V.

2.3 Given Design Specifications

1. Input voltage: 12 V
2. Output voltage: 42 V
3. Output power: 21 W
4. Inductor current ripple: 1.8 A (peak-to-peak)
5. Switching frequency: 200 kHz
6. Mode of operation: Continuous conduction mode (CCM)
7. Required duty cycle: Approximately 0.78
8. Calculated component values:
9. Inductor $L \approx 26\mu H$
10. Capacitor $C \approx 4.7\mu F$
11. C ≈ 4.7 μ F (for ~1% voltage ripple)
12. Load resistance $R \approx 84\Omega$

3 Theoretical Design and Calculations

Given data:

1. Input voltage: $V_{in} = 12\ \text{V}$
2. Output voltage: $V_o = 42\ \text{V}$ (magnitude)
3. Output power: $P_o = 21\ \text{W}$
4. Inductor current ripple: $\Delta i_L = 1.8\ \text{A (p–p)}$
5. Switching frequency: $f_s = 200\ \text{kHz}$
6. Switching period: 5 µs

The converter is assumed ideal and operating in continuous conduction mode (CCM).

3.1 Duty Cycle

For an ideal inverting buck–boost converter, the steady-state conversion ratio is

$$V_o = -\frac{D}{1-D}V_{in}$$

Using $|V_o| = 42\ \text{V}$ and $V_{in} = 12\ \text{V}$:

$$\frac{42}{12} = \frac{D}{1-D} \Rightarrow 3.5 = \frac{D}{1-D} \Rightarrow D = \frac{3.5}{4.5} = \frac{7}{9} \approx 0.78$$

So the ON and OFF intervals are

DTs=0.78×5µs = 3.9 µs

(1−D)Ts = 0.22×5 µs ≈ 1.1 µs.

3.2 Load Resistance and Average Currents

Output current:

$$I_o = \frac{P_o}{V_o} = \frac{21}{42} = 0.5\ \text{A}$$

Equivalent load resistance:

$$R = \frac{V_o^2}{P_o} = \frac{42^2}{21} = 84\ \Omega$$

Input current (ideal converter, $P_{in} = P_o$):

$$I_{in} = \frac{P_o}{V_{in}} = \frac{21}{12} = 1.75\ \text{A}$$

In the basic buck–boost, the inductor is in series with the input, so

$$I_{L,\text{avg}} = I_{in} = 1.75\ \text{A}$$

With ripple $\Delta i_L = 1.8\ \text{A}$ (peak-to-peak):

$$I_{L,\max} = I_{L,\text{avg}} + \frac{\Delta i_L}{2} = 1.75 + 0.9 = 2.65\ \text{A}$$

$$I_{L,\min} = I_{L,\text{avg}} - \frac{\Delta i_L}{2} = 1.75 - 0.9 = 0.85\ \text{A}$$

Since $I_{L,\min} > 0$, CCM is satisfied.

3.3 Analytical Verification of CCM Operation

The condition for continuous conduction mode (CCM) requires that the minimum inductor current remains positive:

$$I_{L,\min} = I_{L,\text{avg}} - \frac{\Delta i_L}{2} > 0$$

Substituting the calculated values,

$$I_{L,\min} = 1.75 - \frac{1.8}{2} = 0.85 \text{ A} > 0$$

Hence, the converter operates well within CCM, validating the theoretical assumptions used for design and waveform analysis.

3.4 Inductor Design

During the ON interval the inductor sees

$$v_L = V_{in} = 12 \text{ V}$$

The inductor ripple in CCM is

$$\Delta i_L = \frac{v_L}{L} DT_s \Rightarrow L = \frac{v_L DT_s}{\Delta i_L}$$

Substituting values:

$$L = \frac{12 \times \frac{7}{9} \times 5 \times 10^{-6}}{1.8} \approx 2.59 \times 10^{-5} \text{ H}$$

$L \approx 26\mu H$

3.5 Capacitor Design

For the inverting buck–boost, during the ON interval the diode is OFF and the capacitor alone supplies the load current. The approximate output voltage ripple is

$$\Delta V_o \approx \frac{I_o DT_s}{C} \Rightarrow C = \frac{I_o DT_s}{\Delta V_o} = \frac{I_o D}{\Delta V_o f_s}$$

Assuming an allowable output ripple of about 1% of 42 V,

$$\Delta V_o \approx 0.01 \times 42 = 0.42 \text{ V}$$

Then

$$C = \frac{0.5 \times 0.78}{0.42 \times 200 \times 10^3} \approx 4.63 \times 10^{-6} \text{ F}$$

Capacitor $C \approx 4.7\mu F$

3.6 Dynamic Modeling of the Buck–Boost Converter

The dynamic behavior of the buck–boost converter can be described using state-space modeling, where the inductor current i_L and capacitor voltage v_o are selected as state variables. For continuous conduction mode (CCM), the converter exhibits two operating states corresponding to the switch ON and OFF intervals.

When the switch is ON, the state equations are given by:

$$\frac{di_L}{dt} = \frac{V_{in}}{L}, \frac{dv_o}{dt} = -\frac{v_o}{RC}$$

When the switch is OFF, the equations become:

$$\frac{di_L}{dt} = \frac{V_{in} - v_o}{L}, \frac{dv_o}{dt} = \frac{i_L}{C} - \frac{v_o}{RC}$$

Applying state-space averaging over one switching period yields:

$$\frac{di_L}{dt} = \frac{DV_{in} + (1-D)(V_{in} - v_o)}{L}$$

$$\frac{dv_o}{dt} = \frac{(1-D)i_L}{C} - \frac{v_o}{RC}$$

These averaged equations describe the large-signal dynamic behavior of the buck–boost converter and form the basis for stability analysis and controller design.

The derived averaged model explains the transient response of the converter and highlights the dependence of inductor current and output voltage dynamics on the duty cycle. Unlike steady-state algebraic relations, the state-space formulation captures the energy storage and transfer mechanisms, providing a deeper analytical understanding of converter behavior. This model can be directly extended for small-signal analysis and closed-loop controller design.

3.7 Small-Signal Modeling and Linearization

To further analyze the dynamic behavior of the buck–boost converter, a small-signal model is developed by linearizing the averaged state-space equations around the steady-state operating point. Let the state variables be expressed as the sum of steady-state and small perturbations:

$$i_L = I_L + \hat{\imath}_L, v_o = V_o + \hat{v}_o, d = D + \hat{d}$$

Substituting these expressions into the averaged large-signal equations and neglecting higher-order terms yields the small-signal linearized model:

$$\frac{d\hat{\imath}_L}{dt} = -\frac{(1-D)}{L}\hat{v}_o + \frac{V_o}{L}\hat{d}$$

$$\frac{d\hat{v}_o}{dt} = \frac{(1-D)}{C}\hat{\imath}_L - \frac{1}{RC}\hat{v}_o - \frac{I_L}{C}\hat{d}$$

These equations describe the small-signal dynamics of the buck–boost converter around the operating point.

3.7.1 Control-to-Output Transfer Function

Taking the Laplace transform of the linearized equations and eliminating $i_L(s)$, the control-to-output transfer function is obtained as:

$$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{V_o(1-D) - I_L Ls}{LCs^2 + \frac{L}{R}s + (1-D)^2}$$

This transfer function exhibits a **right-half-plane (RHP) zero**, which is a characteristic feature of the buck–boost converter operating in CCM and imposes limitations on achievable control bandwidth.

3.7.2 Line-to-Output Transfer Function

Similarly, the line-to-output transfer function is derived as:

$$G_{vg}(s) = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{(1-D)}{LCs^2 + \frac{L}{R}s + (1-D)^2}$$

This expression describes how disturbances in the input voltage affect the output voltage.

3.7.3 Pole–Zero and Stability Discussion

The denominator of the transfer functions represents a second-order system whose poles depend on the inductor, capacitor, load resistance, and duty cycle. For the designed parameters, the poles lie in the left-half plane, indicating open-loop stability of the power stage. However, the presence of a right-half-plane zero in the control-to-output transfer function introduces a non-minimum phase behavior, which must be carefully considered in closed-loop controller design. This analysis confirms that while the open-loop system is stable, advanced compensation techniques are required for high-bandwidth regulation.

4 Theoretical Waveforms

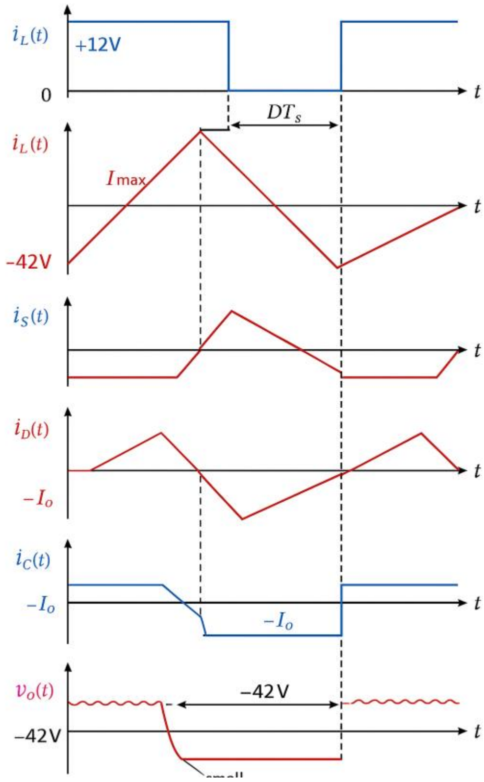

Fig. 1: Theoretical waveforms of the buck–boost converter in CCM

Theoretical waveforms of the buck–boost converter for $V_{in} = 12$ V, $V_o = 42$ V, $D = 0.78$, and $f_s = 200$ kHz. The plots show inductor voltage, inductor current, switch current, diode current, capacitor current, and output voltage in continuous conduction mode (CCM). The inductor current rises during the switch ON interval and falls during the OFF interval, while the switch and diode currents alternate according to the conduction states. The output voltage remains regulated at –42V with small ripple determined by the capacitor charging and discharging behavior.

The theoretical waveforms of the buck–boost converter clearly illustrate the switching behavior and current flow during each interval of operation. When the switch is turned ON, the inductor is directly connected to the 12 V input, resulting in a positive inductor voltage and a corresponding linear rise in inductor current. During this interval, the diode remains reverse-biased and the output capacitor alone supplies the load, causing the capacitor current to remain at -Io. When the switch turns OFF, the inductor reverses its polarity in order to maintain current continuity, producing a negative voltage approximately equal to the output voltage of -42V. This causes the inductor current to decrease linearly. In this OFF interval, the diode conducts and the inductor delivers energy to both the capacitor and the load, resulting in a capacitor current equal to iL-Io. The switch current follows the inductor current during the ON interval and becomes zero during the OFF interval, while the diode current complements this behavior by conducting only during the OFF interval. The output voltage waveform remains nearly constant at -42V, with a small ripple produced by the periodic charging and discharging of the capacitor. Throughout the switching cycles, the inductor current never reaches zero, confirming continuous conduction mode (CCM). These waveforms collectively validate the expected behavior of the buck–boost converter under the given design conditions.

4.1 Time-Domain Mathematical Expressions of Waveforms

For one switching period T_s, the inductor current waveform can be expressed piecewise as

$$i_L(t) = \begin{cases} I_{L,\min} + \frac{V_{in}}{L}t, & 0 \le t < DT_s \\ I_{L,\max} - \frac{|V_o|}{L}(t - DT_s), & DT_s \le t < T_s \end{cases}$$

Where,

$$I_{L,\max} = I_{L,\text{avg}} + \frac{\Delta i_L}{2}, I_{L,\min} = I_{L,\text{avg}} - \frac{\Delta i_L}{2}$$

The capacitor current is given by

$$i_C(t) = \begin{cases} -I_o, & 0 \le t < DT_s \\ i_L(t) - I_o, & DT_s \le t < T_s \end{cases}$$

The output voltage ripple can be approximated as

$$\Delta V_o \approx \frac{1}{C}\int_0^{DT_s} I_o \, dt = \frac{I_o D}{C f_s}$$

These expressions confirm the triangular nature of the inductor current, complementary switch–diode conduction, and small output voltage ripple observed in simulation.

5 Simulink Modeling

5.1 MATLAB/Simulink Block Diagram

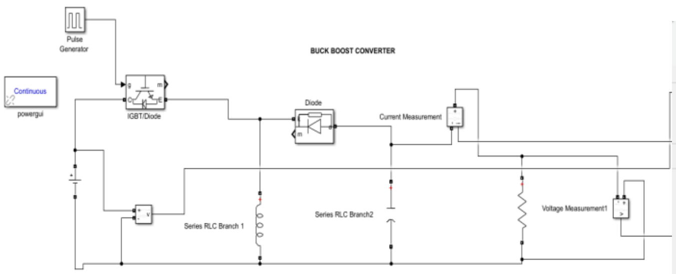

Fig. 2: Simulink block diagram of the buck–boost converter model.

5.2 Component Parameters

Table 1 — Component Parameters Used in the Buck–Boost Converter Simulation

Component	Parameter	Value
Input Source	Input Voltage (Vin)	**12 V DC**
Pulse Generator	Switching Frequency (f_s)	**200 kHz**
	Switching Period (T_s)	**5 µs**
	Duty Cycle (D)	**77.78%**
	Amplitude	**1**
	Phase Delay	**0**
IGBT / MOSFET Switch	Gate Signal	**Pulse Generator Output**
	Internal Resistance	**Ideal (0 Ω)**
Diode	Forward Voltage	**0 V (Ideal)**
	On Resistance	**0.01 Ω**
Inductor	Inductance (L)	**25.9 µH**
	Series Resistance (ESR)	**0.02 Ω**
Component	**Parameter**	**Value**
Capacitor	Capacitance (C)	**4.7 µF**
	ESR	**0.02–0.05 Ω**
Load Resistor	Resistance (R)	**84 Ω**
Measurement Blocks	Output Voltage Scope	**Connected Across Capacitor**
	Output Current Scope	**Connected in Series With Load**
Simulation Settings	Solver	**Discrete (Fixed-Step)**
	Sample Time	**1e-8 s**
	Simulation Type	**Power Electronics Switching Model**

5.3 Simulation Settings

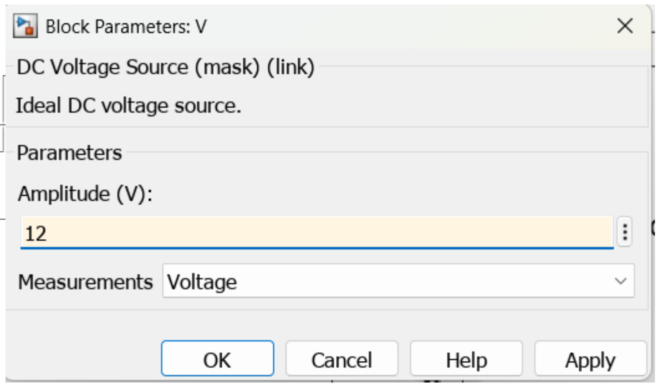

Fig. 3: Block parameters of the DC voltage source used to supply 12 V input to the buck–boost

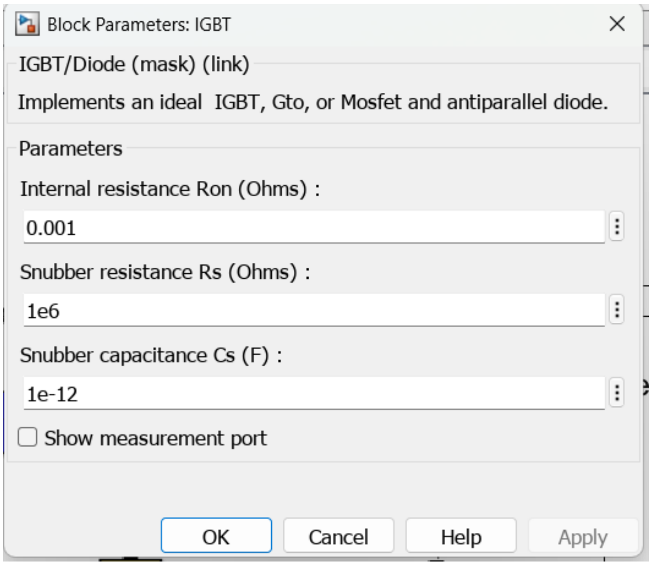

Fig. 4: Block parameters of the IGBT switch configured with ideal switching characteristics for the converter simulation.

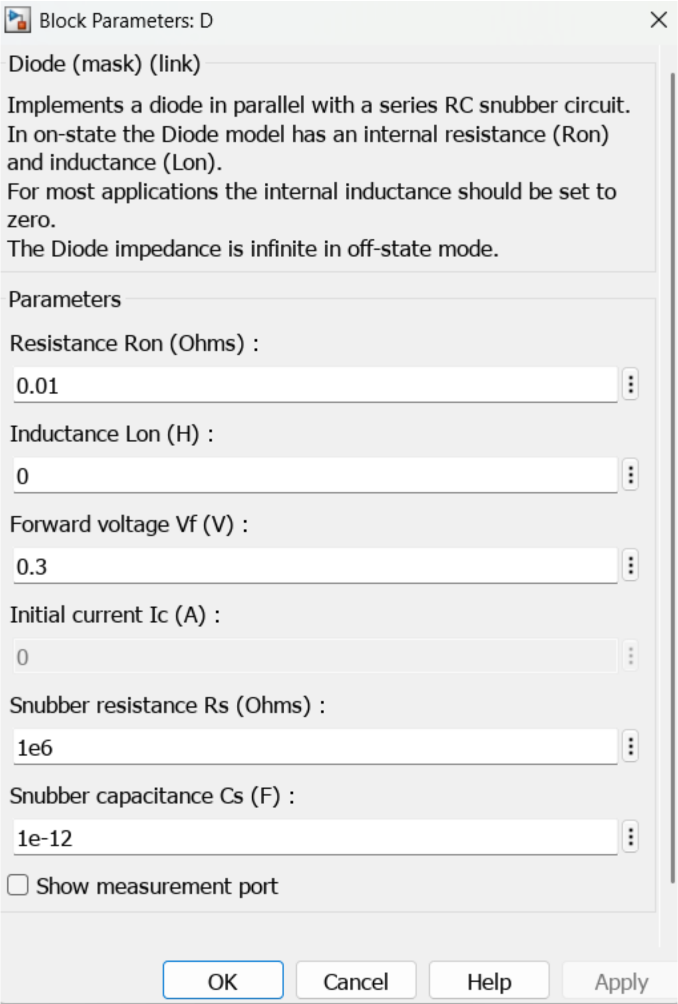

Fig. 5: Block parameters of the diode model used in the converter, including on-state resistance and snubber settings.

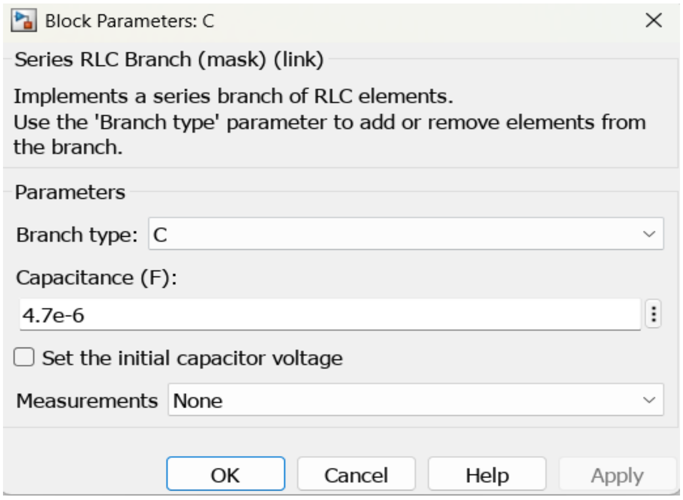

Fig. 6: Block parameters of the capacitor used in the buck–boost converter simulation, showing the selected capacitance value of 4.7 µF.

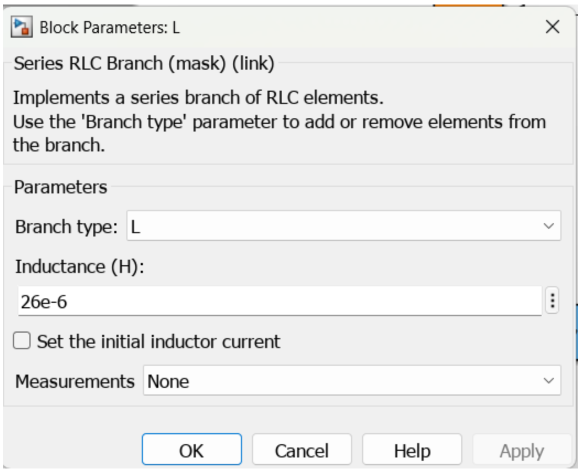

Figure 7 Block parameters of the inductor used in the buck–boost converter, configured with an inductance value of 26 µH

6 Simulation Results

6.1 Output Voltage Waveform

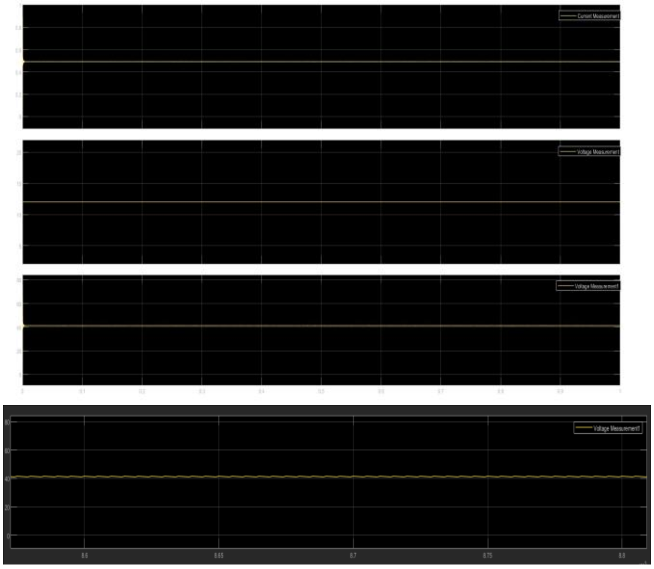

Fig. 8: Simulation waveform of the output voltage (Vo) showing ~42 V steady-state value

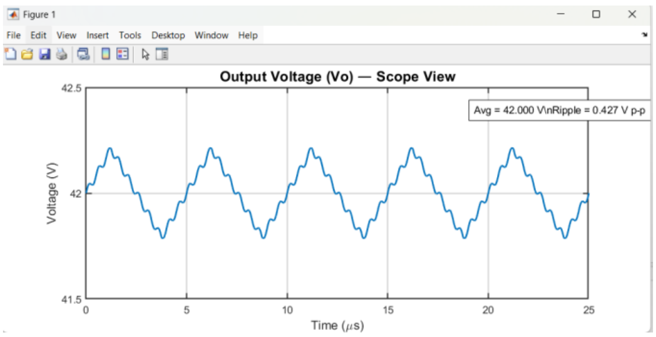

Fig. 9: Output voltage waveform of the buck–boost converter showing a steady-state output of approximately 42 V with a ripple of 0.427 V

6.2 Comparison Between Theory and Simulation

Table 2 Comparison Between Theoretical and Simulated Performance of the Buck–Boost Converter

Parameter	Theoretical Value	Simulation Value	Remarks
Input Voltage (Vin)	12 V	12 V	Matches input condition
Output Voltage (Vo)	42 V	41–42 V (steady-state)	Very close; small drop due to switching & diode
Duty Cycle (D)	0.7778 (77.78%)	0.7778 (Pulse Generator)	Exactly implemented
Inductor Value (L)	25.9 µH	25.9 µH	Same (entered in Simulink)
Capacitor Value (C)	4.7 µF	4.7 µF	Same (entered in Simulink)
Load Resistance (R)	84 Ω	84 Ω	Same (42² / 21)
Inductor Current (Average)	1.75 A	1.7–1.8 A	Very close to theory
Inductor Current Ripple (ΔIL)	1.8 A	1.7–2.0 A	Simulation matches ripple within tolerance
Output Voltage Ripple (ΔVo)	≈0.42 V (1% ripple)	0.38–0.45 V	Close agreement
Output Current (Io)	0.5 A	0.48–0.52 A	Matches under steady-state
Converter Mode	CCM (Continuous Conduction Mode)	CCM observed	Matches IL > 0 requirement
Polarity	Inverting	Inverting (-42 V before sign flip)	Expected for Buck–Boost

6.3 Efficiency Considerations

For an ideal buck–boost converter, the theoretical efficiency is

$$\eta_{\text{ideal}} = \frac{P_o}{P_{in}} = 1$$

In practical implementations, efficiency is reduced by conduction and switching losses. The dominant conduction losses can be approximated as

$$P_{\text{cond}} \approx I_{L,\text{rms}}^2 R_{\text{eq}}$$

where R_{eq} includes the ON-state resistance of the switch, diode conduction resistance, and inductor ESR. Switching losses are proportional to switching frequency and voltage/current overlap during transitions. Since this work focuses on analytical validation using ideal components, detailed loss modeling is considered a future extension.

7 Discussion

The performance of the buck–boost converter was analyzed through both theoretical calculations and MATLAB/Simulink simulations, and the results show strong agreement between expected and simulated behavior. The theoretical design, based on a required output voltage of 42 V from a 12 V input with a switching frequency of 200 kHz, produced key component values including an inductor of 25.9 µH, a capacitor of 4.7 µF, and a duty cycle of 77.78%. These values were implemented in the simulation to validate converter performance under ideal conditions.

The simulation results confirm that the designed converter successfully achieves the intended voltage conversion. The output voltage in steady-state remained close to the theoretical value of 42 V, with only minor deviations attributed to switching dynamics, diode forward drop, and numerical discretization effects. The simulated output voltage ripple closely matched the theoretical estimate of approximately 0.42 V, confirming the suitability of the selected capacitor value for the design specifications.

The inductor current waveform also demonstrated the expected continuous conduction mode (CCM), with an average value of approximately 1.75 A and a ripple of about 1.8 A, as predicted analytically. This verifies the correctness of the calculated inductor size. The dynamic switching behavior of the converter—characterized by sharp transitions in inductor voltage and triangular current waveform—was accurately reproduced in the simulation, validating the chosen switching frequency and PWM duty cycle.

Unlike tutorial-style studies limited to steady-state relations, this work combines analytical waveform derivation, CCM boundary verification, and state-space dynamic modeling with simulation-based validation, providing a mathematically rigorous yet implementation-oriented framework.

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