Double Gates and Short-Channel Carbon Nanotube Transistors

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Abstract: - In this paper, through solving Poisson equations, a precise model for double-gates and dual-material carbon nanotube transistors is presented that is more comprehensive than the previous models. Thus, considering a double-gate transistor with a two-material gate, modeling and solving the Poisson equation are taken into consideration in two dimensions for a more accurate analysis of the inner potential of the channel. In this method, the inside electrostatic potential of the channel is obtained by summing two parts of the long channel potential. Also, the dependence of the inside load of the channel on its inside potential is considered in a way that gives a more accurate answer to the potential of the transistor. The potential is generally considered based on the sum of the one-dimensional potential in the channel (without any dependence on the surface potential) and the lateral potential changes in two dimensions. The charge in the Poisson relation is also considered to evaluate the dependence on the potential within the channel which provides a more complete analysis of the Poisson equation.

Key-Words: - Two-material,-Double-gate transistor, Two-dimensional Poisson equation, Laplace equation.

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1 Introduction

In recent years, miniaturizing the transistors has gained special importance, [1]. The most important reasons are saving costs, decreasing power consumption, increasing speed and volume, and making lighter electronic tools. Despite having these advantages, the physical shrinkage of ordinary transistors proves physical limitations and side effects such as changing the threshold voltage, an increase of the current leakage, reducing the barrier potential by draining the inductor, reducing the slope below the threshold voltage, and reducing the switching speed. Electron thrust properties are observed through the behavior of transistors, some of them are related to short channel effects, [1], [2]. In fact, because of these short-channel effects, downsizing a transistor faces a big challenge. To resolve this problem, double-gate MOSFET transistors can be used.

In recent years, one of the suitable structures to reduce these effects in nanometer-sized transistors is Double-Gate MOSFET, which is technologically the best compatible structure with ordinary MOSFETs and short-channel effects, [2], [3], [4], [5], [6]. Figure 1 shows the structure of this transistor. Some of the advantages of this structure are the reduction of current leakage in the off-state compared to ordinary MOSFETs, reducing the effect of impurity dispersion in reduction of mobility and eliminating their fluctuations (because of low channel impurities), a barrier potential by inducing and controlling the reduction of the barrier potential (through inducing drain) [6].

2 Materials and Methods

For double-gate transistors, various models have so far been introduced based on the analytical surface potential and current load, but the development of an appropriate analytical current model for these transistors is still under investigation, [6].

On the other hand, double-gate MOSFETs with very high impurities and very thin layers are expected options for CMOS technology with very small dimensions [1]. High securities against short channel effects, high transconductance, and below-threshold voltage have been reported by many experimental and theoretical studies on the mentioned devices, [2], [3], [4]. Particularly, double-gate asymmetric MOSFETs (upper gate with p + poly and lower gate with n + poly) have drawn special attention because such structures have a good threshold voltage (neither too large nor too small). If the channel length decreases for any reason, the gate voltage control loses over the threshold voltage. Therefore, reducing the threshold voltage by reducing the channel length is an important issue that needs to be considered. To increase security against short channel effects, a new structure titled two-material MOSFET has been proposed, [4], [5], [6]. This structure has two metals M_1 and M_2 with different working functions in the gate. This type of structure increases transconductance and reduces the short channel effects compared to MOSFET's gate because of the step in the potential profile. In the DMG structure, the peak of the electric field decreases at the end of the drain in a way that the average electric field increases below the gate, [5]. The step potential profile of the surface potential prevents potential changes from the effect sides on the source. After saturation, M_2 absorbs any additional drain-source voltage, and thereby, the area below M_1 is separated from the drain potential changes.

In the second part of the paper, a proposed model is presented for a dual-material double-gate transistor. In the third part, the transistor simulation results are presented based on the proposed model.

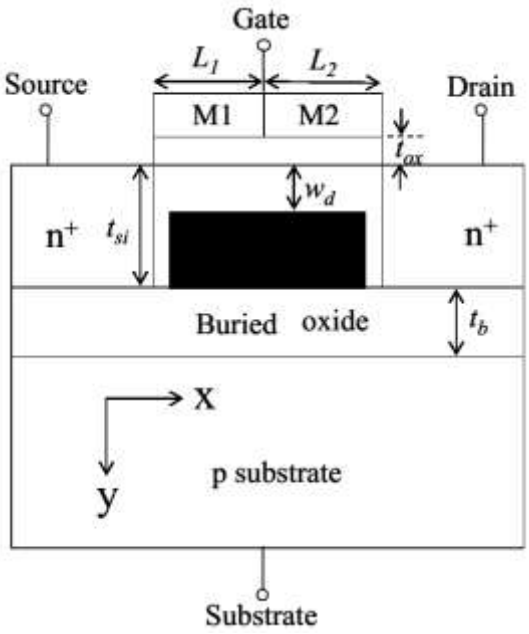

Fig 1. The structure of a double-gates carbon nanotube transistor

2.1. The proposed model for dual-material-double-gate carbon nanotube transistors

A schematic outline of silicon MOSFET is drawn in Figure 2 through the insulation of an impure dual-material-double-gate. The gate has metals M_1 and M_2 with lengths L_1 and L_2, respectively. The source/drain areas in this rectangle are considered, and their concentration is supposed to be uniform. The amount

of channel impurity is displayed with N_A and it is also supposed to be uniform.

Considering the charge as a potential function across the channel, the potential distribution can be expressed in silicon thin-film before creating a strong inversion as follows.

$$\frac{\partial^2 \Phi(x,y)}{\partial x^2} + \frac{\partial^2 \Phi(x,y)}{\partial y^2} = \frac{q}{\varepsilon_{si}} n_i e^{\frac{KT\Phi}{q}} \; for 0 \le x \le L, 0 \le y \le t_{si} \quad (1)$$

Where:

n_i is the intrinsic impurity concentration, ε_{si} is the dielectric constant of silicon, t_{si} is the film thickness, and L is the length of the device. At this time, the potential profile is approximated as follows:

$$\Phi(x,y) = \Phi_s(x) + G(x).H(y) \quad (2)$$

Φ_s (x) shows the surface potential, and the functions H (y) and G (x) show the dependence of the potential function on y and x. It is supposed that the potential function can be categorized into two dependent functions namely x and y. In silicon MOSFET on dual-material insulation, the upper gate contains one material that is p + poly-silicon, but in the dual-material-double-gate-structure, the upper gate contains different materials (p^+ poly-silicon and n^+ poly-silicon) with different functions that are Φ_{M1} and Φ_{M2}. Therefore, the upper channel voltages of poly-silicon p^+ and poly-silicon n^+ differ from each other in the upper gate, and are expressed as follows.

$$V_{FB,fp} = \Phi_{MS1} = \Phi_{M1} - \Phi_{Si} \quad (3)$$

$$V_{FB,fn} = \Phi_{MS2} = \Phi_{M2} - \Phi_{Si} \quad (4)$$

That Φ_{Si} is a function of silicon work and is expressed as follows.

$$\Phi_{Si} = \chi_{Si} + \frac{E_g}{2q} + \Phi_F \quad (5)$$

Where:

E_g is a silicon energy gap at 300 K, χ_{Si} is the electron-silicon adjacency, $\Phi_F = V_T \ln (N_A / n_i)$ is the Fermi potential, V_T is the heat voltage and n_i is the intrinsic impurity concentration. Since there are two regions in the upper gate of the dual-material-double-gate structure (according to Equation (2)), the surface potentials below p^+ poly-silicon and n^+ poly-silicon can be written as follows:

$$\Phi_1(x,y) = \Phi_{s1}(x) + G_1(x).H_1(y) for 0 \le x \le L_1, 0 \le y \le t_{si} \quad (6)$$

$$\Phi_2(x,y) = \Phi_{s2}(x) + G_2(x).H_2(y) for L_1 \le x \le L_1 + L_2, 0 \le y \le t_{si} \quad (7)$$

Φ_{s1} and Φ_{s2} are surface potentials below M_1 and M_2. G_1 (x), G_2 (x), H_1 (y), $V_{Fb,fp}$, $V_{Fb,fn}$, and H_2 (y) are potential functions depending on x and y.

$$E_1(x) = \frac{d\Phi_1(x,y)}{dx}\Big|_{\&_{y=0}} = \frac{d\Phi_{s1}(x)}{dx} + \frac{dG_1(x)}{dx} H_1(0) \quad (8)$$

$$for: 0 \le x \le L_1 \; under \; M1$$

$$E_2(x) = \frac{d\Phi_2(x,y)}{dx}\Big|_{\&_{y=0}} = \frac{d\Phi_{s2}(x)}{dx} + \frac{dG_2(x)}{dx} H_1(0) \quad (9)$$

$$for: L_1 \le x \le L_2 \; under \; M2$$

The equations above are helpful for determining how to change the electric field on the side of the drain by the dual-material-double-gate structure.

In the dual-material-double-gate transistor, shown in Figure 1, t_f and t_b are the thicknesses of the upper and lower gate oxide layers, respectively, and the same gate voltage V_G is designated to both gates. The

channel with a concentration of impurity 120 becomes impure by the donor atoms uniformly. When studying the dependence of the potential distribution on the gate voltage, it is observed that at first, an inversion layer is formed on the inner surface of the n-type poly-silicon back gate. Then, the potential distribution changes linearly while the surface potential is constant. After that, an inversion layer is formed in p-type poly-silicon, and then the potential distribution is unchanged in the channel, and the voltage applied by both oxide gates remains constant. This analysis implies that the structure has two different threshold voltages depending on the upper and lower gates.

The expressions for the upper and lower threshold voltages are as follows.

$$V_{th1} = V_{FB,fp} + 2\Phi_F + \frac{Q_{si}}{2}\left(1 + V_T\frac{4C_{si}}{Q_{si}}\right)\left(\frac{1}{4C_{si}} + \frac{1}{C_f}\right) + V_T\,ln\left(V_T\frac{4C_{si}}{Q_{si}}\right) - \frac{\gamma t_f + t_{si}}{\gamma t_f + t_{si} + \gamma t_b} \quad (10)$$

$$V_{th2} = V_{FB,fp} + 2\Phi_F + \frac{Q_{si}}{2}\left(1 + V_T\frac{4C_{si}}{Q_{si}}\right)\left(\frac{1}{4C_{si}} + \frac{1}{C_f}\right) + V_T\,ln\left(V_T\frac{4C_{si}}{Q_{si}}\right) \quad (11)$$

V_{th1} is the low gate threshold voltage with poly n and V_{th2} is the high gate threshold voltage with poly p and n, in a way that $\gamma = \frac{\varepsilon_{si}}{\varepsilon_{ox}}$ and $Q_{si} = qN_A t_{si}$ are the channel acceptor charge. In the above models, discharging and charge-making are considered. But, for short-channel components, both charges are ignored in the inference of the threshold voltage model [7-8].

3 Results and Discussion

The surface potential diagram for a dual-material-double-gate transistor is shown in Figure 2 using the proposed model, thus, V_{gs} = 0.15 and V_{DS} = 0.75 V are considered. As observed in Figure 2, the potential function at the center has a step function on the surface. As a result of this step function, the area below the upper gate (M_1) is obtained against the changes of potential in the drain. In other words, it can be said that the step function eliminates the effect of the electric field created by the drain-source potential within the area below M_1. It means that the drain potential has a little effect on the drain current after the saturation zone.

It is clear that the less the thickness of the silicon layer decreases, the step function becomes sharper at the middle of the channel. Also, whenever the film thickness decreases, the difference between the surface and center potential decrease too. The main reason is that the central potential is closer to the surface potential.

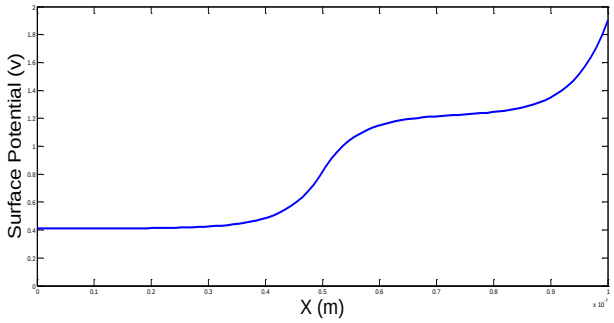

Fig 2. Diagram of the surface potential for dual-material and double-gate transistor per V_{gs} = 0.15 and V_{DS} = 0.75 V

4 Conclusion

In this research, by plotting the surface potential function for different values of V_{DS}, the minimum potential function occurred constant for the first time for different values of V_{DS} in a way that it is always below the M_1 region, and the potential function changes slightly through changes in V_{DS}. It is also concluded that the more the gate-source voltage increases, the surface potential increases. The surface potential for the different amounts of impurity concentration was also plotted, and it is observed that the increase of the impurity concentration causes the surface potential to increase. By drawing the electric field, it is observed that there is a peak in the distribution of the electric field in the common

boundary of M_1 and M_2. The peak in the electric field causes an increase to be escalated in drift velocity and in the performance speed of dual-material-double-gate devices.

References:

[1] Singh A.K., An analytical study of undoped symmetric double-gate MOSFET (SDG). *Int. J. Numer. Model.: Electron. Netw. Devices Fields* 24, 515-525 (2011).

[2] Woo J.H, Choi J.M, Choi Y.K., Analytical Threshold Voltage Model of Junctionless Double-Gate MOSFETs with Localized Charges. *IEEE Trans Electron Devices* 60, 2951-2955 (2013).

[3] Chiang T.K., A quasi-two-dimensional threshold voltage model for short-channel junctionless double-gate MOSFETs. *IEEE Trans Electron Devices* 59, 2284-2289 (2012).

[4] Singh A.K., An analytical study of undoped symmetric double-gate MOSFET (SDG). *International Journal of Numerical Modelling: Electronic Networks, Devices, and Fields* 24, 515-525 (2011).

[5] Jin L, Hongxia L, Bo Y, et al., A two-dimensional analytical model of fully depleted asymmetrical dual-material gate double-gate strained-Si MOSFETs. *J. Semicond* 32, 044005-1-7 (2011).

[6] Tsormpatzoglou A, Pappas I, Tassis D.H, et al., Analytical threshold voltage model for short-channel asymmetrical dual-gate material double-gate MOSFETs. *Microelectron. Eng* 90, 9-11 (2012).

[7] Tafakori P, Orouji A., Investigation of multiple material gate impact on short channel effects and reliability of nanoscale SOI MOSFETs. *International Journal of Electrical and Computer Engineering* 7. 128-131 (2013).

[8] Subramaniam S, WALE R.N.A, JOSHI S.M., Drain current models for single-gate mosfets & undoped symmetric & asymmetric double-gate soi mosfets and quantum mechanical effects: a review. *International Journal of Engineering Science and Technology* 5. 96-105, 2013.

Contribution of individual authors to the creation of a scientific article (ghostwriting policy)

Reza Akbarpourani has carried out all of the scientific works belonging to this research consisting of calculations, simulation, and extraction of the results.
Hassan Ghalami Bavil Olyaee has advised Reza Akbarpourani for his research work.
Seyed Alireza Mousavi Shirazi has organized the paper.

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