Simulation and Analysis of Fully Adiabatic Circuit Designing with Single Power Clock for High Frequency Low Power VLSI Circuits

YASHU SWAMI,
Department of ECE, Aditya Engineering College, Surampalem, INDIA

Abstract: Adiabatic logic guarantees vast diminishments of power utilization since it doesn't disperse power. This paper audits ongoing advancement in adiabatic circuits. First, the fully adiabatic circuit designing technology called as pass-transistor adiabatic logic (PTAL) is discussed. Next, the operation of the dual rail logic and the power clock supply with the logic operation of the PTAL technology is discussed. Further, many basic logic circuits using the PTAL technology are designed, compiled and simulated. Finally, the performance results, power dissipation, speed, efficiency and load analysis of the circuits are compared with the conventional and existing CMOS technology under same simulation conditions using standard 45nm technology with VDD = 1V and proves that even at high frequencies above 2GHz, it is able to outperform the dominating conventional CMOS logic designing in the field of power dissipation. The simulation results are provided to support our claim. We used 45nm technology for all our simulations.

Keywords: Adiabatic circuit, pass-transistor logic, nano-electronics, Low power VLSI, high speed IC.

Received: July 8, 2021. Revised: March 26, 2022. Accepted: April 21, 2022. Published: May 31, 2022.

1. Introduction

As the demand for portable devices such as laptops and cell phones grows, so does the need to reduce their power consumption. Traditional methods such as voltage scaling are slowly reaching their limits, making it increasingly difficult to achieve these stringent power needs, especially as system complexity grows. It is now more important than ever to use non-conventional and logical methods to reduce power use. One of the prominent approach to address this existing issue is to use fully adiabatic circuits. We apply some of the notions of thermodynamics to electrical circuits in this method [1]-[4]. If the energy transfer is purposely retarded in thermodynamics, it is possible to transfer energy between two heat sinks while losing very little amounts of energy. Similarly, if charge transfer in electrical circuits occurs at a far slower rate than the natural RC, we dissipate very little power. The quantity of power dissipated is directly proportional to the rate of charge transfer. [5]-[8].

In the surge of nano-electronics industry, we have been encountering a remarkable spurt in development, because of the utilization of IC design in data computations, media communications and customer electronics. From the single transistor era in 1958 to today's ULSI (Ultra Large Scale Integration) architectures with over 50 million transistors in a single chip, we've come a long way. In recent decades, the expanding number of transistors fabricated and synchronized on a chip, as well as the increasing transistor switching speed, has empowered incredible execution and performance change in IC frameworks. Shockingly, such amazing execution changes and improvements have been accompanied with an increase in framework power usage. High energy-power consumption characteristics in extra-efficient frameworks necessitate more expensive bundling, fabrication, and cooling improvements, resulting in cost increment and lower framework reliability quality.

The key driving force for the improved performance has been the advanced digital CMOS IC logic and circuit architecture. It motivates nano-electronics advancements for a variety of scientific and technological applications. Because of its vital outstanding upgrades and features, such as high speed, low power, dependable execution, and advancements in fabrication and processing technology, the demand and interest for digital CMOS nano-chip design will continue to rise in the future. In any event, when performance and execution demand rise, the level of on-chip integration and clock frequency will rise as well. The increased performance framework's power usage and energy consumption will be a major design constraint [9]-[12].

Integrated circuits' advanced features and applications have created a demand for low-power nano-electronic circuit design. With 2300 transistors and a clock frequency of 1 MHz, the Intel 4004 microprocessor, introduced in 1971, dissipated roughly 1 watt of power. With 42 million transistors and a clock speed of 2.4 GHz, the Pentium released in 2001 dissipates roughly 65 watts of power. While power dissipation grows linearly over time, power density grows exponentially due to the shrinking size of integrated circuits. If this exponential increase in power density continued, a computer developed would have the same power as a nuclear reactor. Due to the high power density, reliability issues arise such as electro-

migration, thermal strains, and hot-carrier effects in resulting in device degradation [13]-[16]. This further results in the loss of performance. Another element driving the demand for low-power ICs is the growing market for battery-powered portable consumer electronics. The desire for smaller, lighter, and more durable electronic items interprets to low power consumption indirectly. In the portable systems, battery life is quickly becoming a prime concern. Low power consumption is a top priority for these systems because it has a direct impact on performance by reducing battery life. In this context, low-power VLSI design has risen to prominence as a vibrant and quickly evolving subject. Hence, in portable and battery-operated systems, low-energy operation is essential. Therefore, in this manuscript, we try to explore the key sources of power/energy dissipation; and propose a PTAL technology corresponding logics to reduce power/energy dissipation. The recommended advanced low power PTAL technology outcomes are supported by the simulation results. The proposed model outcomes are compared with conventional CMOS technology and validated using the TCAD circuit simulator.at 45nm technology node.

2. Adiabatic Circuit Design

Adiabatic circuits can be categorized as semi-adiabatic circuits and truly-adiabatic circuits. Semi-adiabatic circuits have some un-adiabatic power dissipation at each stage of the adiabatic pipeline, whereas truly adiabatic circuits do not have any un-adiabatic power dissipation at any stage in ideal cases. A good example of the former is the 2N2N-2P circuit logic style, whereas a good example of the latter is split level charge recovery logic (SCRL).

It should be noted that, SCRL circuit design style, despite the lack of un-adiabatic power dissipation, they have numerous drawbacks as compared to the 2N2N-2P circuit logic design. It requires more power-clocks and greater area due to the presence of reversible power pipelines. Hence, we use 2N2N-2P circuit logic style in designing our models. We could observe that the development of adiabatic logic, as a method of reducing the energy consumption of digital logic, has succeeded in achieving the limits to some extent. It makes an efficient use of ac power supply to recycle the energy utilized to charge the node-capacitances of the logic circuits. Despite the fact that various innovative techniques have been developed, each including many creative ideas, there are several flaws in those circuits. The flaws can be listed as; the logic implementation is extremely complicated [1]-[5], the logic gates are not well suited for CMOS implementation, several power-clock supplies are required for effective stage-to-stage interfacing, and non-adiabatic transitions may jeopardise the energy savings.

The proposed pass-transistor CMOS adiabatic logic (PTAL) is a dual rail semi-adiabatic logic that uses only one power clock supply and has a comparatively low gate complexity (two-phase). In terms of performance and energy consumption, the simple implementation of PTAL outperforms previously disclosed adiabatic logic families.

3. Fully Adiabatic Ptal Operation

PTAL is a four-stage trapezoidal power-clock (PC) that supports dual-rail logic with pass-transistor NMOS functional blocks of F and $\overline{F}$, as well as a pair of cross-coupled PMOS devices in each stage. The PTAL four stages can be listed as evaluate-stage, hold-stage, discharge-stage and idle-stage. During the Evaluate (E) stage, the PC is rising and evaluating the logic output. Hold (H) stage, the evaluated logic output is held at the respective logic level with the PC at its peak. While the PC is falling down; in the discharge (D) stage, the charged logic output node capacitor discharges and the charge is flown back to the PC. In the final stage, Idle (I) stage, when the PC is at its low, the output returns to its initial logic state. The operation is exemplified and demonstrated by 2X1 MUX function shown in Fig. 1:

$$Y = A.S + B.\overline{S}$$

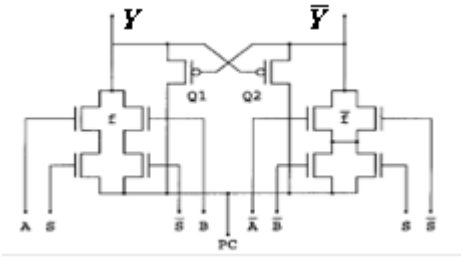

Fig 1: PTAL 2X1 Multiplexer

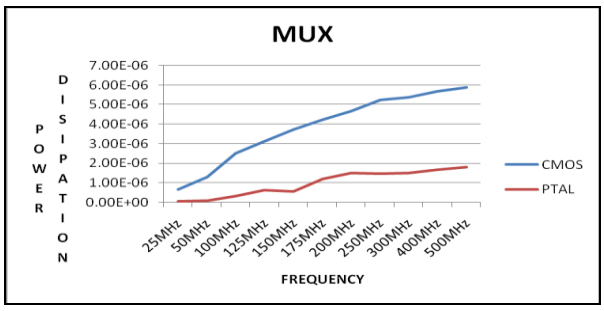

Fig 2: Power analysis for PTAL vs. CMOS 2x1 Mux.

DOI: 10.37394/232022.2022.2.20

PTAL Mux consists of true complementary pass transistor NMOS functional blocks (F and $\bar{F}$), and a cross-coupled PMOS latch (Q1, Q2). At the beginning, PC = 0 and starts to ascend. Assume that the inputs A and S are both high, and that a conducting path exists between the power-clock PC and the output *Y*. Given that f is connected to PC, *Y* will begin to rise from zero toward PC's peak. The load capacitance of the successive gates will keep the node $\bar{Y}$ "tri-state" and near to 0V.

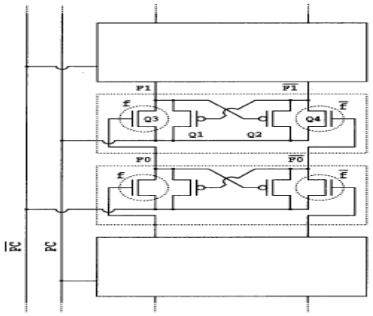

Fig 3: PTAL Shift Register

The PMOS Q1 with gate $\bar{Y}$ switches ON when the power clock PC ramps up, and the output *Y* is charged up to the peak of PC. The gate *Y* of the PMOS Q2 will stay in the OFF state. After that, the power clock will ramp down to 0V, restoring the energy held in the *Y* output-node capacitance. The logic gate has a comparatively low level of complexity. Because of the PTAL's dual-rail design, the function also need to be replicated as $\bar{Y}$. However, because it is possible to share transistors in the fabrication of NMOS functional blocks F and $\bar{F}$, this will not always result in 100% duplication.

The voltage-PC feeds all Even-Logic stages in a series of PTAL gates, while the inverted voltage-PC (phase-shifted by 180) supplies all Odd-Logic PTAL gates of series. An efficient single-inductor LC oscillator that can act as the PTAL power source can provide both PC and $\overline{PC}$. The stage-to-stage interface of the PC and $\overline{PC}$ with the series of PTAL logic gates is illustrated in Fig. 3, with a single NMOS pass transistor acting as the functional block per stage. A simple shift register exemplified in Fig. 3, is made up of a series of PTAL gates. Fig. 4 represents the schematic of PTAL designed inverters in series. The power analysis simulation result shown in Figure 5, is obtained when a periodic binary sequence of '1010' is propagated through the series of PTAL inverters illustrated in Fig. 4. The energy consumption analysis demonstrates how energy is transferred from the power-clock supply to the output logic nodes and partially recovered back. During the part of the clock period, the output logic block is powered when the PC is ascending, and then partially energy is recovered during the part of the clock period when the PC is descending. The simulation results claim that the energy loss in each clock period in this example is even less than 19 Fj/gate.

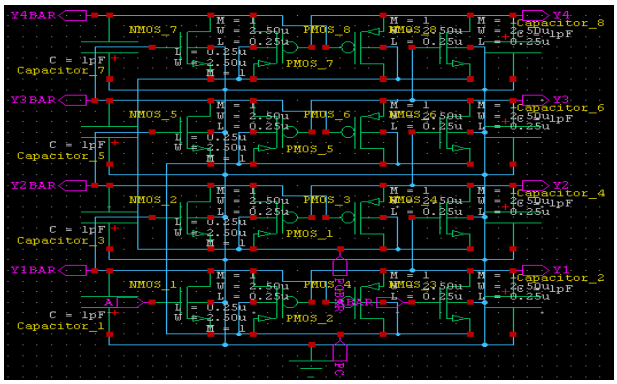

Fig 4: PTAL Inverter chain

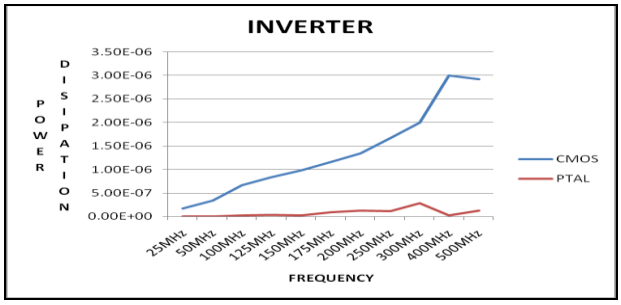

Fig 5: Power analysis for PTAL vs. CMOS inverter.

There are main two stages to the logic operation: evaluate (E) when the power clock is ascending up, and discharge (D) when the power clock is descending down. The E phase of an odd stage and the D phase of an even stage are the same. In Fig. 3, initially, when PC = 0, both output nodes are discharged. When PC is ascending up, there is a path via one of the functional blocks during this E phase. The path exists because one of the logic inputs is at the peak of the power clock. As a result, the output node *Y* will begin to ramp up in time with the power clock PC. PMOS switches on when the voltage difference between *Y* and $\bar{Y}$ exceeds Vtp (PMOS threshold voltage), and the output node capacitance is charged to the peak of PC. The charge is first delivered to the output node via (via the NMOS functional block *F*) and subsequently by the PMOS device. Because *Y* closely follows PC and is always greater than $\bar{Y}$, the other PMOS device remains in OFF state during this clock period. $\bar{Y}$ is a tri-stated complementary output that should ideally stay at logic

'0' during the clock period when *Y* follows the power clock. Although the tri-stated output is sensitive to parasitic charge coupling, the correct logic levels can be sampled at the peak of the power clock. The power clock descends down during the discharge phase. The discharge of the output node is first aided by the PMOS device. When PC approaches zero, the logic high inputs are close to the peak of PC. The final portion of the discharge process is completed through the conducting functional block. Above-threshold logic low inputs allow both outputs to be discharged to 0 volts without wasting energy.

4. PTAL Simulation Results

The schematic and the Spice simulation waveforms of various PTAL circuits were obtained by using standard 45nm technology with Vdd = 1V for various high speed operating frequencies. The results of the designed PTAL circuits are compared for the performance and power dissipation with conventional CMOS logic under same simulation conditions and inputs. It proves that even at high operating frequencies, it is able to outperform the dominating conventional CMOS logic designing in the field of power dissipation. Simulation results for the basic logic gates and common digital circuits are compiled.

4.1 Two Input PTAL AND/NAND Gate

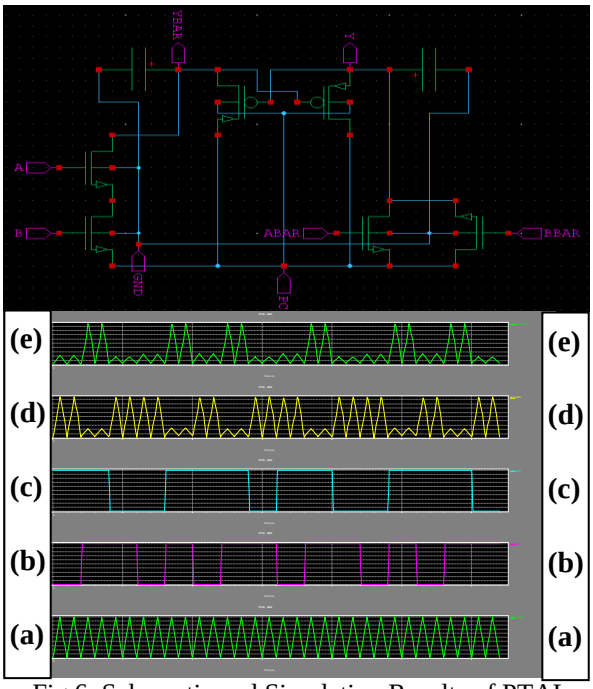

Fig 6: Schematic and Simulation Results of PTAL Two-Input AND / NAND Gate: (a) PC, (b) Input Signal A, (c) Input Signal B, (d) NAND Output (e) AND Output.

The PTAL two-input NAND/ AND gate is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Fig. 6. The Power analysis of the circuit, PTAL vs. conventional CMOS logic is shown in Fig. 7.

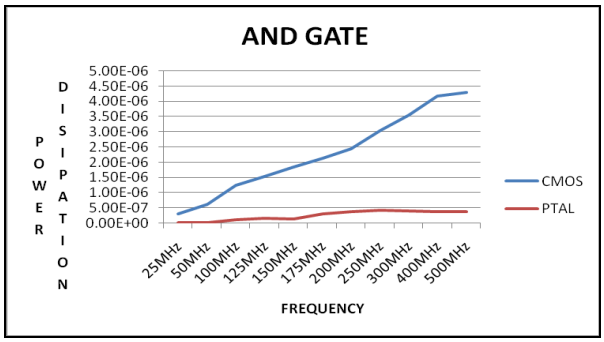

Fig 7: Power analysis for PTAL vs. CMOS AND gate.

4.2 Two Input PTAL OR/NOR Gate

The PTAL two-input OR/NOR gate is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Fig. 8. The Power analysis of the circuit, PTAL vs. conventional CMOS is shown in Fig. 9.

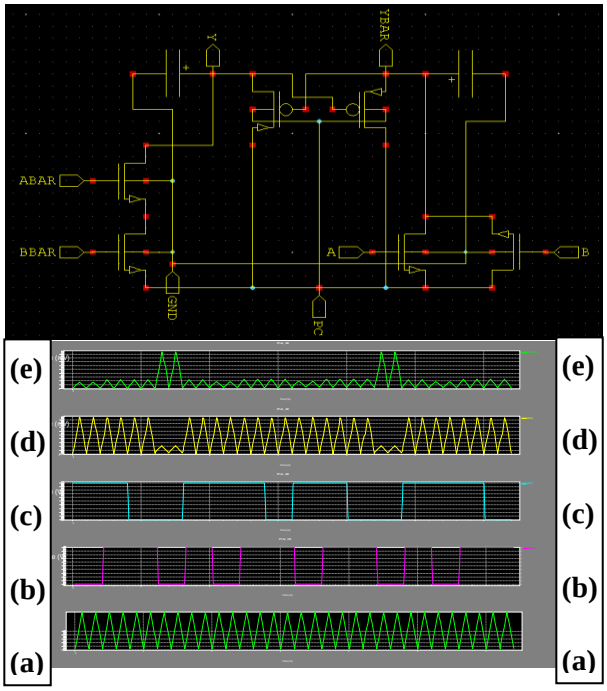

Fig 8: Schematic and Simulation Results of PTAL Two-Input OR / NOR Gate: (a) PC, (b) Input Signal A, (c) Input Signal B, (d) OR Output (e) NOR Output

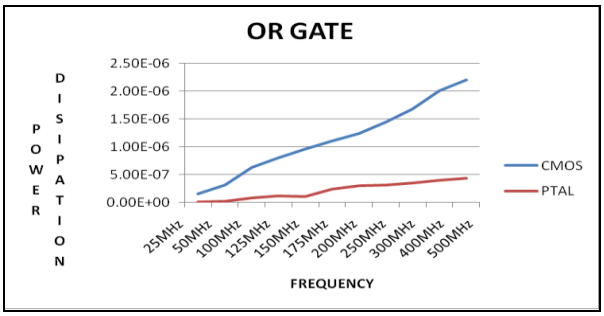

Fig 9: Power analysis for PTAL vs. CMOS OR gate.

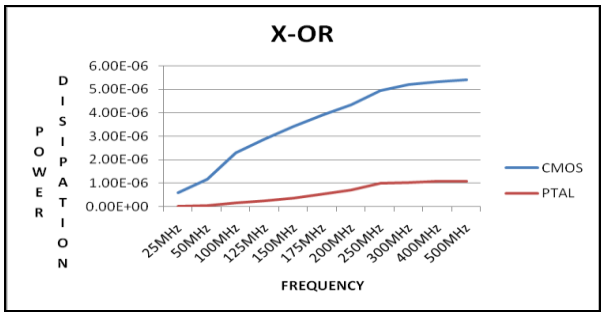

Fig 11: Power Analysis for PTAL vs. CMOS XOR gate.

4.3 Two Input PTAL XOR/XNOR Gate

The PTAL two-input XOR/XNOR gate is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Fig. 10. The Power analysis of the circuit, PTAL vs. conventional CMOS is shown in Fig. 11.

4.4 2x1 PTAL Multiplexer

The PTAL 2X1 Multiplexer is implemented and simulated using standard 45nm technology. The schematic and the simulated waveforms are shown in Fig. 12. The Power analysis of the circuit, PTAL vs. conventional CMOS is shown in Fig. 13.

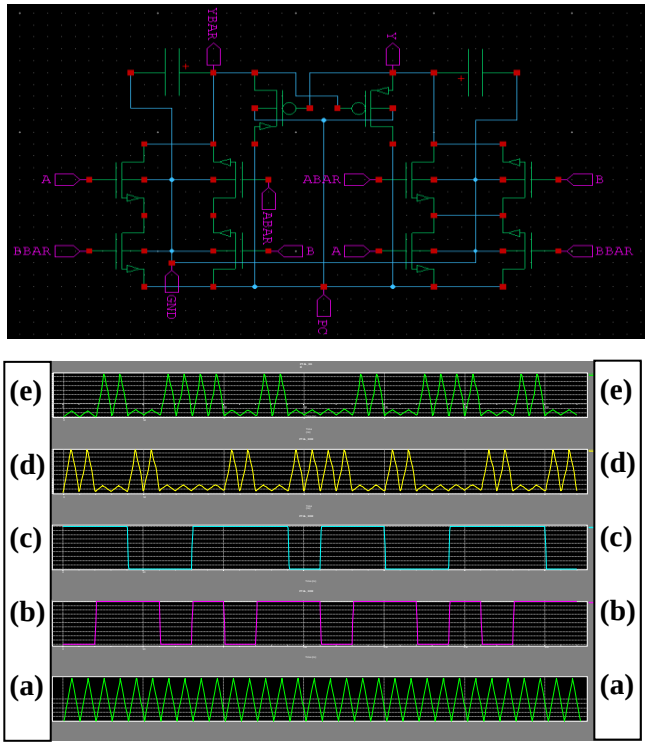

Fig 10: Schematic and Simulation Results of PTAL Two-Input XOR / XNOR Gate: (a) PC, (b) Input Signal A, (c) Input Signal B, (d) XOR Output, (e) XNOR Output,

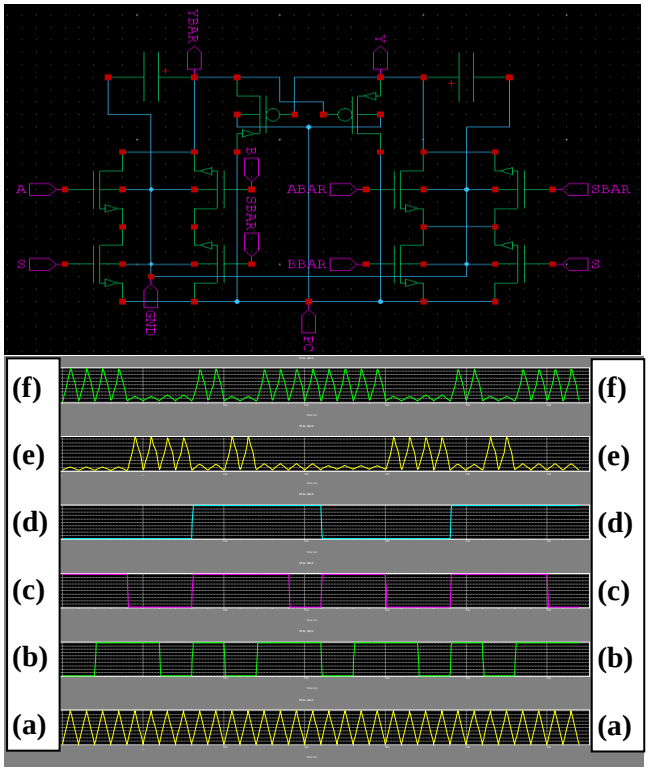

Fig 12: Schematic and Simulation Results of PTAL 2X1 MUX: (a) PC (b) Input Signal A (c) Input Signal B (d) Input Signal S (Select Bit) (e) MUX Output (f) $\overline{MUX}$ Output.

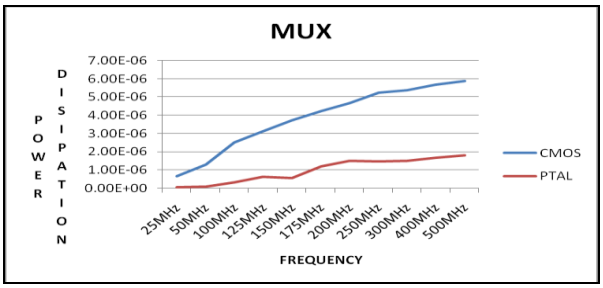

Fig 13: Power analysis for PTAL vs. CMOS MUX.

5. Conclusions

We did a preliminary investigation of Fully Adiabatic Circuit Designing with Single Power Clock for High Frequency Low Power VLSI Circuits in this paper. Logically, we show that the proposed adiabatic circuit logic can save a significant amount of energy. Experiments on simple gates and more sophisticated arithmetic circuits backed up our theoretical findings. The fully Pass Transistor CMOS Adiabatic Logic (PTAL) circuit designing was implemented and rigorously studied and analyzed against the conventional CMOS technology. We could conclude that PTAL supports dual-rail logic. It uses a single two-phase AC power clock to power both the rails. The complexity of a proposed PTAL gate models are quite low as it consists of true and complementary NMOS functional blocks, as well as a pair of cross-coupled PMOS devices. The rigorous and precise simulation results claim that the modeled circuits can be operated even above 2 GHz clock frequency and power-clock supply down to 1V peak-to-peak using conventional 45nm technology. In terms of fast speed and energy consumption, it outperforms previously documented adiabatic logic approaches.

The power savings that we have in adiabatic circuits come at a cost. We need specially designed charge recycling power-clock supplies which have less power dissipation associated with them. However, the use of charge in recycling power supply is essential for the successful implementation of adiabatic circuits in practice. Additionally, better circuit designs with less power-clock supplies must be developed. These are few of the areas that need further investigation and solid starting points for research and development in the stream of Fully Adiabatic Circuit Designing with Single Power Clock for High Frequency Low Power VLSI Circuits.

References

[1] Shinghal D, Saxena A, Noor A. Adiabatic logic circuits: a retrospect. MIT International Journal of Electronics and Communication Engineering. 2013 Aug;3(2):108-14..

[2] Rabaey JM, Pedram M, editors. Low power design methodologies. Springer Science & Business Media; 2012 Dec 6..

[3] B. Voss and M. Glesner, "A Low Power Sinusoidal Clock," *In Proc. of the International Symposium on Circuits & Systems*, ISCAS 2001.

[4] Swami Y, Rai S. Comparative methodical assessment of established MOSFET threshold voltage extraction methods at 10-nm technology node. Circuits and Systems. 2016;7(13):4248.

[5] Bhuvana BP, Bhaaskaran VK. Design of FinFET-based energy efficient pass-transistor adiabatic logic for ultra-low power applications. Microelectronics Journal. 2019 Oct 1;92:104601..

[6] Swami Y, Rai S. Ultra-thin high-K dielectric profile based NBTI compact model for nanoscale bulk MOSFET. Silicon. 2019 Jun;11(3):1661-71.

[7] T. Indermauer and M. Horowitz, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," *Technical Digest IEEE Symposium Low Power Electronics*, 102-103, Oct' 02.

[8] Swami Y, Rai S. Modeling and analysis of sub-surface leakage current in nano-MOSFET under cutoff regime. Superlattices and Microstructures. 2017 Feb 1;102:259-72.

[9] A. Blotti and R. Saletti, "Ultralow- Power Adiabatic Circuit Semi-Custom Design," IEEE Transactions on VLSI Systems, vol.12, 1248-53, Nov' 04.

[10] Hu J, Xu T, Xia Y. Low-power adiabatic sequential circuits with complementary pass-transistor logic. In48th Midwest Symposium on Circuits and Systems, 2005. 2005 Aug 7 (pp. 1398-1401). IEEE.

[11] Kumar A, Swami Y, Rai S. Modeling of surface potential and fringe capacitance of selective buried oxide junctionless transistor. Silicon. 2021 Feb;13(2):389-97.

[12] Roy K, Prasad SC. Low-power CMOS VLSI circuit design. John Wiley & Sons; 2009 Feb 2.

[13] MOSIS: MOS Integration Service. Available online: www.mosis.org.

[14] Swami Y, Rai S. Modeling and characterization of inconsistent behavior of gate leakage current with threshold voltage for Nano MOSFETs. American Journal of Modern Physics. 2018;7(4):166-72.

[15] C. HU, "Future CMOS Scaling and Reliability," Proceedings IEEE, Vol. 81, No. 05, pp. 682-689, February 2004.

[16] Swami Y, Rai S. Comprehending and Analyzing the Quasi-Ballistic Transport in Ultra Slim Nano-MOSFET Through Conventional Scattering Model. Journal of Nanoelectronics and Optoelectronics. 2019 Jan 1;14(1):80-91.