

A New Approach to Analysis and Synthesis of Incompletely Defined Sequential Systems

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Abstract: - The Present paper refers to an interesting topic regarding the analysis and synthesis of incompletely defined digital sequential systems. For these systems, the number of states is different from 2^k , where ‘k’ represents the bits of the state code, and the difference is represented by the so-called parasitic states, as the states where the system may be accidentally. For cost reasons, systems are usually designed with a small number of states, which is why the system could transit a parasitic state, and we can say that the system presents a digital logic hazard. The digital logic hazard can be induced into the system due to electromagnetic interference, parasitic signals due to voltage inputs, defects of the circuits, system hazards, etc. The novelty of the digital system synthesis solution proposed in this paper consists of taking into account the transitions for parasitic states to the initial reset state.

Key-Words: - incompletely sequential systems, parasitic states, fluency graph, digital system, ASM flow diagram, signal diagram, stand-by state, Veitch-Karnaugh table.

Received: April 11, 2026. Revised: May 4, 2026. Accepted: June 26, 2026. Published: October 21, 2026.

1 Introduction

A system that has several states, where ‘k’ represents the bits of the state code, is called an incompletely defined sequential system as described in [1], [2], [3]. We also define the number of parasitic states as the states where the system may be accidentally. Although some current researches [4], [5], [6], [7], [8], [9], [10], [11], on various aspects of incompletely defined systems has been done, the topic we refer to has a high degree of novelty, because it introduces the concept of parasitic states, considered as transition states to the initial reset state in the process of analysis and synthesis of such systems. The rest of the paper is organized as follows: Section 2 presents the working methodology, Section 3 refers to the method for system correction by imposing the transitions of parasitic states into an idle “stand-by” state, Section 4 addresses some related works, and, finally, Section 5 presents our conclusions.

2 Working Methodology

Let’s consider the following implementation, where the synthesis of a digital automatic system with the design described in Figure 1 is proposed.

The signals notated with SW_1 , SW_0 represent the logic values which are provided by the two types

of switches ($SW_i=0$ - switch commuted to ‘0’, $SW_i=1$ - switch commuted to ‘1’). We noted with S - start value, which has the following values: $S=0$ if the B button is not pushed; $S=1$ if the B button is pushed. The C_K signal represents the synchronization clock, which allows the transfer between states when the negative front toggles.

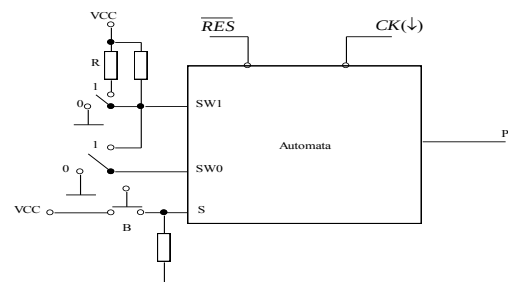


Fig. 1: – Digital automatic system.

Source: created by the authors

The signal notated with $\overline{RES}$ represents an asynchronous reset signal. The signal notated with $P = P_1 \cdot CK$ represents the output signal. The generated output pulses are described in Table 1 (Φ represents the indifferent value).

Table 1. The generated output pulses

S	SW1	SW0	P
0	Φ	Φ	0
1	0	1	1 pulse
1	1	0	2 pulses
1	1	1	3 pulses

Source: created by the authors

The system's flow description is shown as a signal diagram (waves) behavior in Figure 2 $SW_1 = SW_2 = 1$.

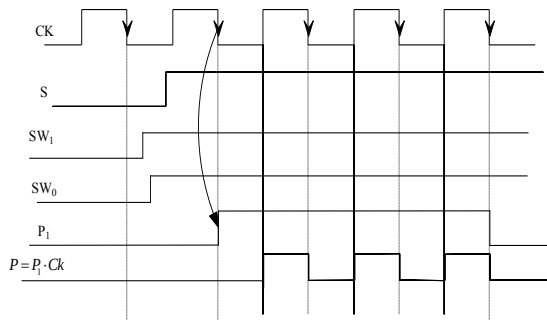


Fig. 2: Signal diagram.

Source: created by the authors

It can be observed that the SW_1 , SW_0 values are stable while $S=1$ (button B is ON). The values of the SW_1 , SW_0 could be changed only when $S=0$ (button B is OFF). The ASM flow diagram is presented in Figure 3.

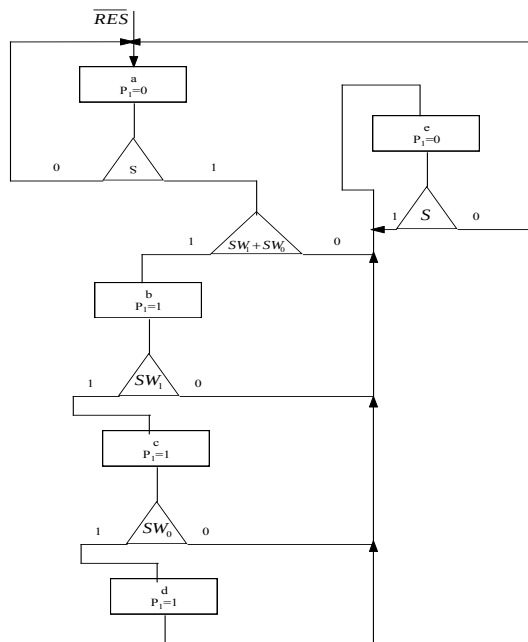


Fig. 3: ASM flow diagram.

Source: created by the authors

Initially, the system is reset in state 'a' ($\overline{RES} = 0$). If $S=0$, the system will remain in the

present state. When $S=1$, the system will jump next, where if $SW_1 + SW_0 = 0$ the system will jump to state 'e'.

If $SW_1 + SW_0 = 1$ the system jumps to state 'b', where the output pulse signal $P=1$ is generated. If $SW_1 = 0 \Rightarrow SW_1 SW_0 = 01$ and the next state will be 'e'. We will convert the ASM diagram into the fluency graph where the transition to the next state is produced by the transfer function equation (1), as in Figure 4.

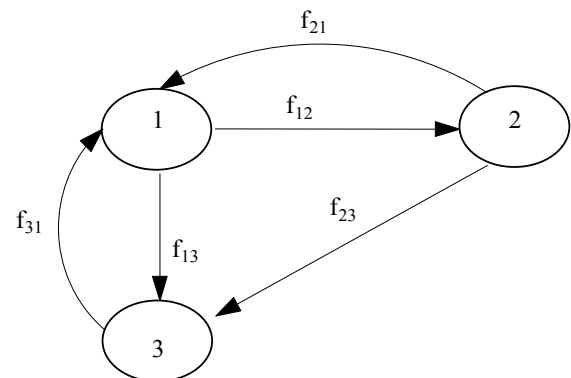


Fig. 4: Fluency graph.

Source: created by the authors

From state 1, the system will jump to the next state 2 only if the transfer function $f_{12} = 1$, otherwise it will jump to state 3 if the transfer function $f_{13} = 1$ etc.

It's obvious that $f_{12} \cdot f_{13} = 0$, $f_{21} \cdot f_{23} = 0$ etc. $\left(\sum_{j=1}^3 f_{ij} = 1, i=1,2,3 \right)$

The binary codification of the states is chosen as follows: $a = 000, b = 011, c = 111, d = 101, e = 001$.

It can be observed that, other than these 5 states, there are also 3 parasitic states $f = 010, g = 100, h = 110$.

Figure 4 shows the new fluency graph, which was deducted from Figure 3, taking into consideration also the above relations. From Figure 5 the following relations are calculated:

$$\begin{aligned}
 f_{aa} &= \overline{s}, f_{ab} = s \cdot (SW_1 + SW_0), f_{ae} = s \cdot (\overline{SW_1} \cdot \overline{SW_0}) \\
 f_{bc} &= SW_1, f_{be} = \overline{SW_1} \\
 f_{cd} &= SW_0, f_{ce} = \overline{SW_0} \\
 f_{de} &= 1 \\
 f_{ea} &= \overline{s}, f_{ee} = s
 \end{aligned} \tag{1}$$

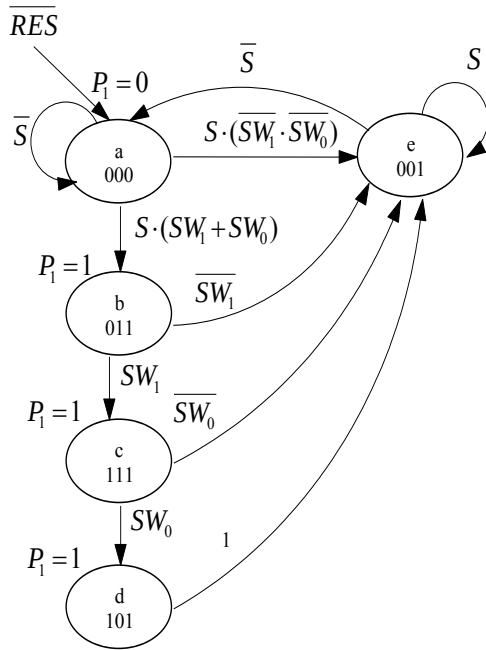


Fig. 5: Fluency graph.
Source: created by the authors

A possible implementation of the system with the fluency graph is illustrated in Figure 6.

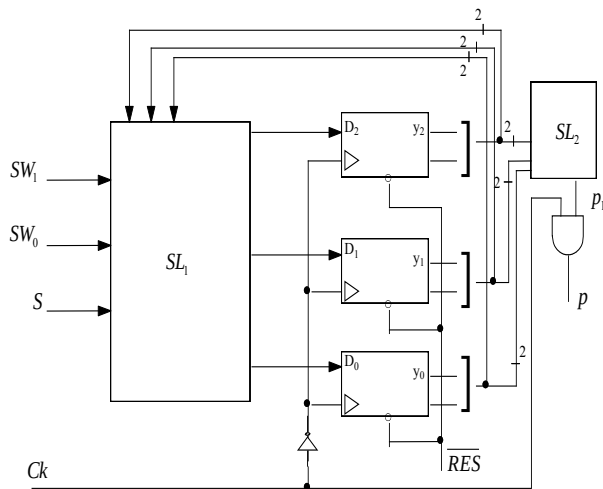


Fig. 6: Possible implementations of the system.
Source: created by the authors

Considering the partial Veitch-Karnaugh tables, the equations of the digital systems become:

$$\begin{aligned} D_2 &= \bar{y}_2 y_1 SW_1 + y_2 y_1 SW_0 \\ D_1 &= \bar{y}_2 y_1 SW_1 + y_0 S (SW_1 + SW_0) \\ D_0 &= S + y_2 + y_1 \\ P &= P_1 \cdot Ck = (y_2 + y_1) Ck \end{aligned} \quad (2)$$

Using the Fairchild Semiconductor Data Book, the full timing analysis for the propagation delays for the used logic gates (AND, OR, INV) is described in Table 2:

Logic gate	$T_{p(LH)}$	$T_{p(HL)}$
AND 2 inputs	7.6ns	8.8ns
AND 3 inputs	18ns	14ns
AND 4 inputs	7.8ns	8.89s
OR 3 inputs	11.4ns	7.4ns
OR 2 inputs	10ns	14ns
D latch	8.5ns	13ns
INV	9.5ns	13ns

Source: created by the authors

In case of using the $T_{p(LH)}$ (Time Propagation delay from Low to High), the implementation cost for (3) equations is:

$$\text{Cost}_{(2)} = 7 \cdot \text{AND}(3in) + 6 \cdot \text{OR}(2in) + 2 \cdot \text{INV} = 7 \cdot 18ns + 6 \cdot 10ns + 2 \cdot 9.5ns = 205ns \quad (3)$$

The Cost value represents the number of logic gates multiplied by the propagation delay from each one.

3 The Analysis of the Digital System Considering Also the Parasitic States (F, G, H)

3.1 Transitions from State f=010. The Equations for the Input D_2, D_1, D_0 from (2) are:

$$\begin{aligned} D_2 &= SW_1 \\ D_1 &= SW_1 + S(SW_1 + SW_0) = SW_1 + S \cdot SW_0 \\ D_0 &= 1 \end{aligned} \quad (4)$$

The new transitions for the fluency graph are presented in Figure 7. The state code and the value of the P_1 variable are indicated by $\frac{y_2 y_1 y_0}{P_1}$.

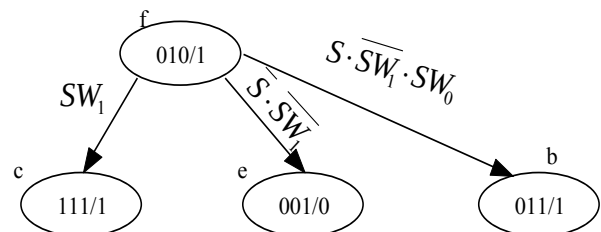


Fig. 7: Fluency graph considering the 'f' parasitic state.
Source: created by the authors

3.2 Transitions from state g=100

The equations for the input D_2, D_1, D_0 are expressed as shown in Equation (5):

$$\begin{aligned} D_2 &= 0 \\ D_1 &= S(SW_1 + SW_0) \\ D_0 &= 1 \end{aligned} \quad (5)$$

The new transitions for the fluency graph, Figure 8:

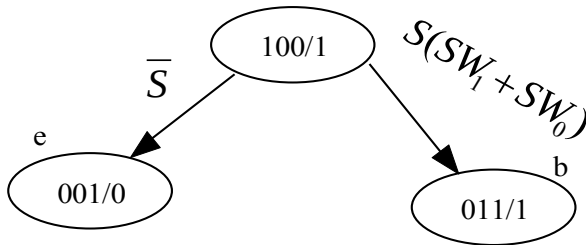


Fig. 8: Fluency graph considering the 'g' parasitic state.

Source: created by the authors

3.3 Transitions from State h=110

For this transition with state h=110, the equations for the input D_2, D_1, D_0 , is expressed as shown in Equation (6):

$$\begin{aligned} D_2 &= SW_0 \\ D_1 &= S \cdot (SW_1 + SW_0) \\ D_0 &= 1 \end{aligned} \quad (6)$$

The new transitions for the fluency graph, Figure 9:

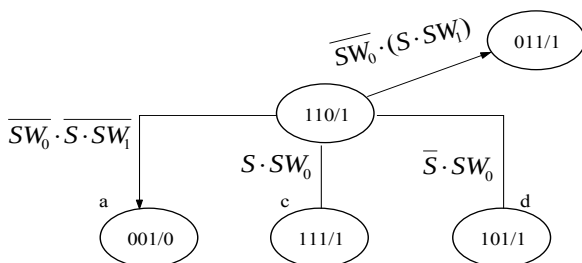


Fig. 9: Fluency graph considering the 'h' parasitic state.

Source: created by the authors

The final fluency graph with the additional parasitic states 'f', 'g', and 'h' is shown in Figure 10.

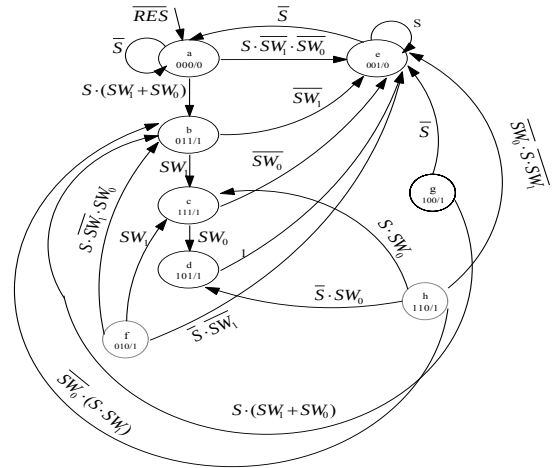


Fig. 10: Final fluency graph with the additional parasitic states 'f', 'g', 'h'.

Source: created by the authors

4 System Correction by Imposing the Transitions of Parasitic States into An Idle "Stand-By" State

Let's consider the fluency remodeled graph as in Figure 11:

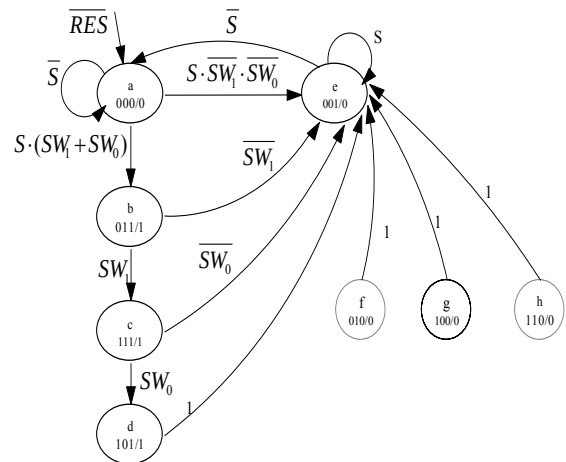


Fig. 11: Fluency graph remodel.

Source: created by the authors

The structure of the automatic digital system is the same as in Figure 5, but a new set of D_i, P_i functions will be computed. Considering that the 'e' state is the most convenient, the parasitic state transitions are forced, as shown in the Veitch-Karnaugh partial tables are described in Figure 12.

P_1				
$y_2 \backslash y_1 y_0$	00	01	11	10
0	0	0	1	0
1	0	1	1	0

D_1				
$y_2 \backslash y_1 y_0$	00	01	11	10
0	$S(SW_1 + SW_0)$	0	SW_1	0
1	0	0	0	0

D_2				
$y_2 \backslash y_1 y_0$	00	01	11	10
0	0	0	SW_1	0
1	0	0	SW_0	0

D_0				
$y_2 \backslash y_1 y_0$	00	01	11	10
0	S	S	1	1
1	1	1	1	1

Fig. 12: Partial Tables.

Source: created by the authors

The following equations (7) are deduced from partial tables:

$$\begin{aligned}
 P &= P_1 \cdot Ck = y_0(y_2 + y_1)Ck \\
 D_2 &= y_1 y_0 (y_2 SW_0 + \overline{y_2} SW_1) \\
 D_1 &= \overline{y_2} [y_1 \overline{y_0} \cdot S(SW_1 + SW_0) + y_1 y_0 SW_1] \\
 D_0 &= y_2 + y_1 + S
 \end{aligned} \quad (7)$$

In case of using the $T_{p(LH)}$ (Time Propagation delay from Low to High), the implementation cost for (4) equations is (8):

$$\begin{aligned}
 \text{Cost}_{(4)} &= 3 \cdot \text{AND}(3\text{in}) + 9 \cdot \text{AND}(2\text{in}) + 3 \cdot \text{OR}(2\text{in}) \\
 &+ 1 \cdot \text{OR}(3\text{in}) + 3 \cdot \text{INV} = 3 \cdot 18\text{ns} + 9 \cdot 7.6\text{ns} + \\
 &1 \cdot 11.4\text{ns} + 3 \cdot 10\text{ns} + 3 \cdot 9.5\text{ns} = 192.3\text{ns}
 \end{aligned} \quad (8)$$

Due to simplified logic equations (4), (7) there is no such critical path.

The fluency state table, which corresponds to the fluency graph remodel from Figure 11, is described in Table 3:

Table 3. Fluency State Table.

Present State	Symbol	S SW_1 SW_0	Next State	Symbol
000/0	a	0ΦΦ	000	a
		100	001	e
		101	011	b
		11Φ	011	b
001/0	e	0ΦΦ	000	a
		1ΦΦ	001	e
011/1	b	Φ0Φ	001	e
		Φ1Φ	111	c
010/0	f	ΦΦΦ	001	e
110/0	h	ΦΦΦ	001	e
111/1	c	ΦΦ0	001	e
		ΦΦ1	101	d
101/1	d	ΦΦΦ	001	e
100/0	g	ΦΦΦ	001	e

Source: created by the authors

The quantitative metric comparison between the uncorrected synthesis (equations 1-3) with a cost of $\text{Cost}_{(2)} = 205\text{ns}$ and the corrected synthesis (equation 4) with a cost of $\text{Cost}_{(4)} = 192.3\text{ns}$ demonstrates that the implementation of the corrected synthesis is much more economical in the case of using the elementary logic gates.

For future related work, it will be demonstrated that a more economical approach is to consider Programmable Logic Devices (PLD).

The technical reason is that's why 'e' state is the optimal choice over the initial reset state a ' or any other stable state is because the other states 'b', 'c', 'd' transits also to the 'e' state, which can be considered as a 'hub' state. Also, it should be clarified that this approach is the best fit considering such graph states' transitions. In other situations, with different graph state transitions, for sure, the convenient state can differ from any other stable state, but also, a timing cost analysis should be done accordingly.

5 Related Work

In [12] a heuristic method for the minimization of an incompletely specified finite state machine with unspecified values of output variables is presented. They consider, at the stage of minimizing internal states, as optimization criteria the power consumption and the possibility of merging other states. The proposed method is based on merging two states. The main goal of this method is not to find the minimal number of states, but such a representation of the FSM, which consumes a minimal amount of power as described in [13].

A new method for the minimization of Incompletely Specified Finite State Machines (ISFSMs), as is presented in [14], where he takes into account as optimization criteria the critical delay path. In addition, the method allows for minimizing the number of transitions and input variables of the FSM. The method is based on the sequential merging of two internal states, including the optimization criteria.

Rao and Biswas proposed a simple procedure for the state minimization of an incompletely specified sequential machine whose number of internal states is not very large. The minimal state machine covering the incompletely specified machine is then obtained from the implication trees. From the recursive nature of the procedures developed, it is evident that the methods are programmable, as described in [15].

A greedy algorithm to produce a small set of

incomplete ADSs (Adaptive Distinguishing Sequences) and use experiments to compare this with two previously published algorithms for generating state identifiers, as described in [16]. In the experiments was found that incomplete ADSs produced by the proposed greedy algorithm led to relatively compact state identifiers.

Pena and Oliveira proposed an algorithm for the problem of state reduction in incompletely specified finite state machines. This algorithm is not based on the enumeration of compatible sets, and therefore, its performance is not dependent on the number of prime compatibles. It's proven that the algorithm is exact and presents results that show that, in a set of hard problems, it is much more efficient than both the explicit and implicit approaches based on the enumeration of compatible sets, as described in [17].

A heuristic method for state reduction in Incompletely Specified Finite State Machines (ISFSMs) is described in [18]. The algorithm is based on checking sequence generation and identification of sets of compatible states. There was obtained results as good as the best exact method in the literature but with significantly better run-times. In addition to finding a reduced FSM, this algorithm also generates an I/O sequence that can be used as test vectors to verify the FSM's implementation, as described in [19], [20], [21].

Based on the above methods, it's proven that our proposed method, which represents the consideration of the transitions for the parasitic states to the initial reset state, is much more robust, faster, and, in the case of implementation with logic gates, it uses less logic.

6 Conclusion

In the present paper, the authors proposed for analysis a digital system with $N_s \neq 2^k$ a number of states, where k represents the number of code state bits. Also, the new notion of parasitic states $N_p = 2^k - N_s$, where N_p represents the number of parasitic states, and a case study is shown. The paper addresses the analysis and synthesis of incompletely defined sequential systems by introducing a novel correction method centered on the concept of "parasitic states". It is identified a practical scenario is identified in the design. When the actual number of states is less than the number of state code bits, the remaining unused states might represent a 'parasitic state' where the system can accidentally enter due to a defect or

noise, leading to a digital hazard that can alter the normal behavior of the digital system.

The novelty of the proposed idea for the digital system synthesis resides in the consideration of the transitions for the parasitic states to the initial reset state through the 'e' hub state.

Declaration of Generative AI and AI-assisted Technologies in the Writing Process

During the preparation of this work, the author(s) utilized artificial intelligence (AI) technologies solely for the purpose of linguistic refinement and grammatical correction. Following the application of these tools, the author(s) comprehensively reviewed, verified, and edited the resulting text. The author(s) maintain full accountability and responsibility for the accuracy, integrity, and final content of the publication.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

Author Al Valachi, M Timis: Conceived the study, performed the experiments, analyzed the data, and wrote the manuscript.

Author M Timis: Contributed to the final version of the manuscript.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

This research is NOT part of any kind of governmental/educational funds.

Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article

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