Design of a Linear LNA for 5G Applications using 45 nm Technology

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Abstract—A low noise amplifier (LNA) plays a very significant role in communication systems. Despite having a good amplification of the signal it must offer other attributes like noise figure, linearity etc for making the communication system more robust. With the advent of 5G communication, the requirement of a high BW LNA is becoming important. This paper presents the design of a LNA which have a common gate input configuration, an active inductor in place of a passive inductor, common drain amplifier at the output stage and a linearity circuit. Common gate amplifier offers a good voltage amplification while the common drain stage enhances the stability. The active inductor facilitates reduction of the die area paving the way for a cost efficient structure. This proposed design achieves a gain of 15.17dB with substantial enhancement of linearity. A good noise figure of 7dB is obtained while using 11 transistors and eliminating the need of passive inductors. The peak gain is achieved at 3.5GHz.

Keywords—Low Noise Amplifier, Noise figure, Linearization

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1. Introduction

Any communication receiver requires efficient amplification of the signal with as less distortion as possible. LNA is prominent structure to be used for this purpose. Different designs of LNAs have been realized but as the trend in communication is shifting towards high frequency spectrum, different design challenges are arising. The primary challenge is to have a sufficiently better gain while maintaining a good noise figure at higher frequencies. Also it should have a good linearity so as to have less distortion in the system, thus making it more robust. Moreover feasibility of fabrication needs to be maintained with a look towards cost effectiveness.

LNA finds its applications in different domains of electronics. We find its applications in

• Communications receivers like in cellular telephones, GPS receivers, wireless LANs (WiFi), and satellite communications.

• In a satellite communications system, the bottom station receiving Antenna uses an LNA as a result of the received signal is weak since satellites have restricted power and thus use low-power transmitters

• The LNA boosts the antenna signal to beat feed line losses between the antenna and therefore the receiver.

• LNAs will enhance the performance of software-defined radio (SDR) receiver systems. SDRs square measure usually designed to be general purpose and thus the noise figure isn't optimized for anyone explicit application.

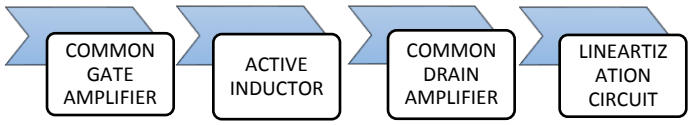
To maintain the input matching in each gain modes a LNA topology relies on the cascode stage with inductive degeneration an efficient gain control is done by decomposing the input circuit into two separate ways, one in all that is disabled within the low-gain mode [1] . For minimum noise figure relies a differential cascode topology with inductive source degeneration. M_{main} -main amplifying transistor whose width power constraint condition. M_{AUX} transistor and a capacitor, C_A-to cancel and improve linearity [2] . A LNA schematic consists of three stages which are common gate amplifier, common drain amplifier and active inductor is designed to mitigate gain, noise figure, area constraint. Common gate and common drain are used for input and output stages in every LNA [3]. For high linearity and to minimizes the degradation of gain, noise figure (NF) and power consumption a technique having an additional folded diode with a parallel RC circuit as an intermodulation distortion (IMD) sinker [4].

This paper presents a LNA design with a common gate input configuration, an active inductor in place of a passive inductor, common drain amplifier at the output stage and a linearity circuit. Common gate amplifier offers a good voltage amplification while the common drain stage enhances the stability. The active inductor facilitates reduction of the die area paving the way for a cost efficient structure. This proposed design achieves a gain of 15.17dB with substantial enhancement of linearity. A good noise figure of 7dB is obtained while using 11 transistors and eliminating the need of passive inductors. The peak gain achieved at 5GHz which makes it suitable for 5G applications.

The remaining part of the paper is organized as follows. Section II deals with the theoretical and technical background. Sections III deals with the details of the design with experimental results. Section IV includes the concluding remarks

2. Technical Background

The block diagram of the system consists of four parts:



- Common gate amplifier: In electronics, a common-gate amplifier is one of three basic single-stage field-effect transistor (FET) amplifier topologies. It is used as a current buffer or voltage amplifier. In this circuit the source terminal of the transistor serves as the input, the drain is the output and the gate is connected to ground, or "common,". The

analogous bipolar junction transistor circuit is the common-base amplifier.

- Active inductor: The design of tunable and compact RF integrated circuit is challenging. Although spiral inductor is the common implementation approach in integrated circuits, it is possible to design active circuits. As reported in, active inductor occupies of the passive inductor, and the most unique feature is its tunability of inductance
- Common drain amplifier: In electronics, a common-drain amplifier, also known as a source follower, is one of three basic single-stage field-effect transistor (FET) amplifier topologies, typically used as a voltage buffer. In this circuit (NMOS) the gate terminal of the transistor serves as the input, the source is the output, and the drain is common to both (input and output), hence its name. The analogous bipolar junction transistor circuit is the common-collector amplifier. This circuit is also commonly called a "stabilizer".
- Linearity circuit: In an amplifier that exhibits linearity, the output-versus-input signal amplitude graph appears as a straight line. The gain, or amplification factor, determines the slope of the line. The steeper the slope, the greater the gain. The amplifier depicted by the red line has more gain than the one depicted by the blue line. Both amplifiers are linear within the input-signal strength range shown, because both lines in the graph are straight.

3. The proposed Design

The circuit presented in this work is an LNA that is designed with common gate, active inductor, common drain with output input matching and a linearity circuit along with it. We have evaluated the circuits without and with linearization

3.1 SECTION A

The proposed design presented here is a LNA having common gate amplifier in the input where each transistor is biased with a certain voltage. To make the circuit inductor less we have used the concept of active inductor with the help of transistors. The output of the LNA is designed with common drain amplifier and will provide a stabilized voltage gain. This is shown in figure 1.

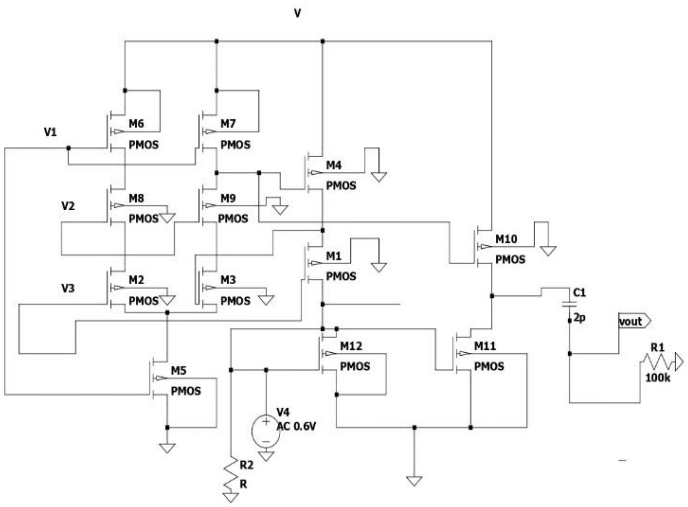


Figure 1:Circuit diagram of the LNA

EXPERIMENTAL RESULTS OF SECTION A

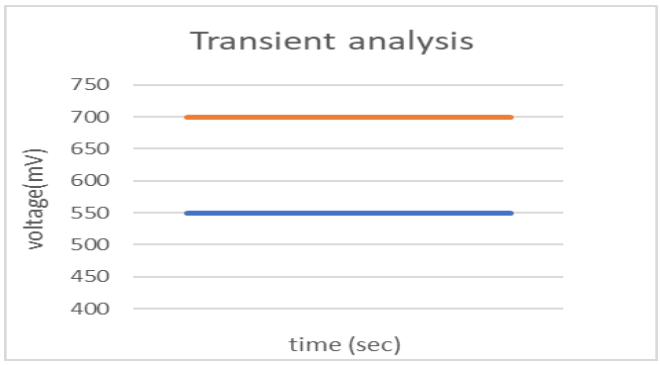


Figure 2: Transient response of the LNA

The circuit is simulated using GPDK 45 nm. The transient response is presented in figure 2.The input voltage obtained is 550mV and the output voltage is 700mV, which reflects that the circuit is working as an amplifier

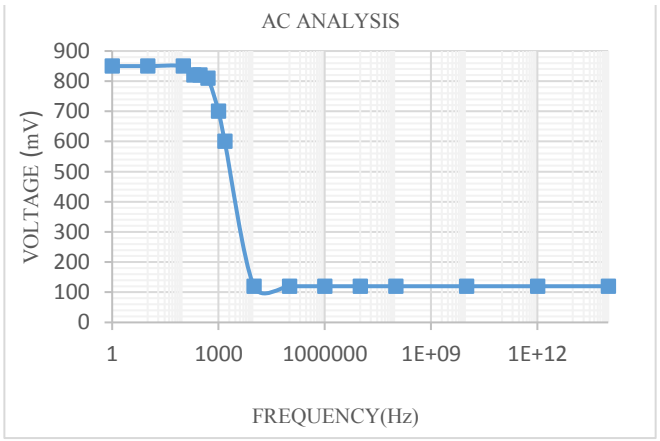


Figure 3: AC analysis of the LNA before impedance matching

The AC analysis is done but the circuit is working at low frequency and acting as the low pass filter at this stage. This necessitates remodeling of the design to make it suitable for 5G applications. Output matching is a useful technique which needs to be employed for this purpose.

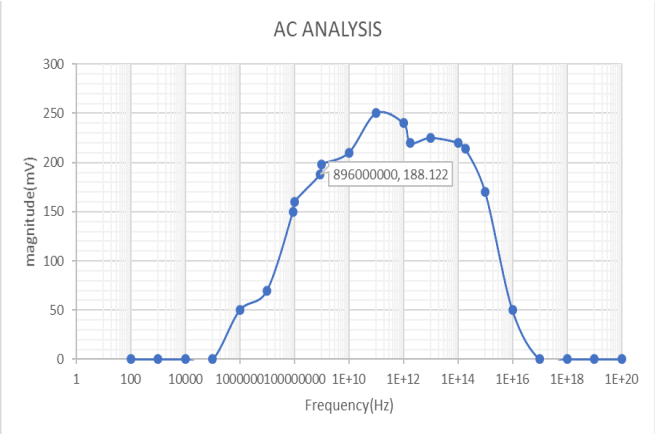


Figure 4 AC analysis after impedance matching

The input impedance is matched with a resistive load, R_l =50Ω in the input so that the power transferred is maximum. By parametric analysis, the specifications of the transistors and voltage source are given. By taking, R_l = 10K, C_l = 10uf, Supply voltage = 1V, we found Bandwidth is of the range of high frequency, f_h = 186.3 THz and Lower Frequency, f_l = 896.6 MHz. This is shown in figure 4.

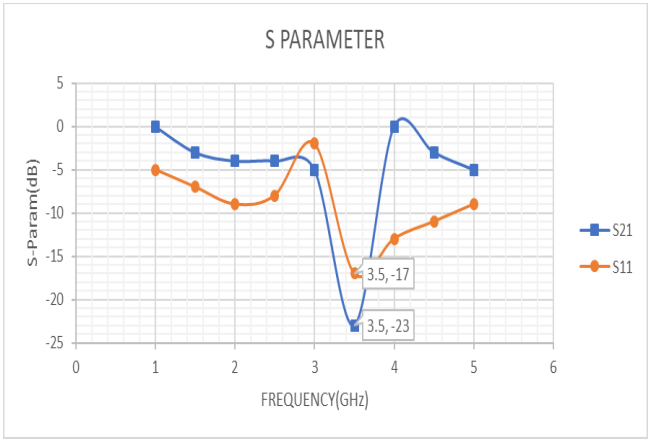


Figure 5: Stability of the LNA circuit

S parameter analysis of the linearity circuit shows us that the LNA is stable since s_{11}<1 and s_{22}<1. As a result, the amplifier

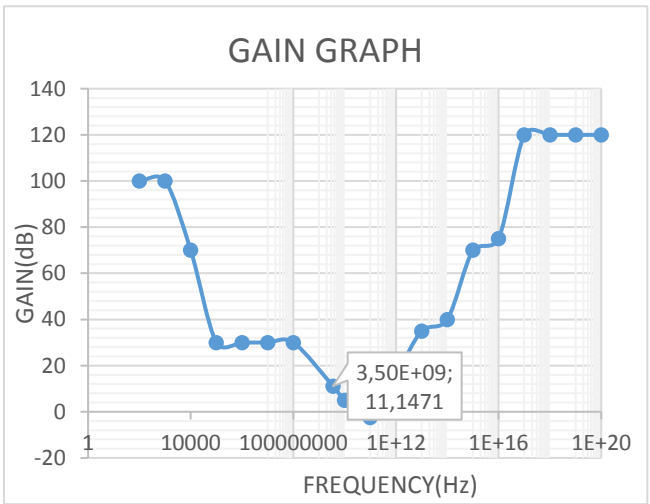


Figure :6 Gain graph before linearization

remains stable for any combination of source and load impedance which is reflected in figure 5

It is seen from the figure 6 that at 3.5GHz, the gain is achieved to be 11.1471dB.

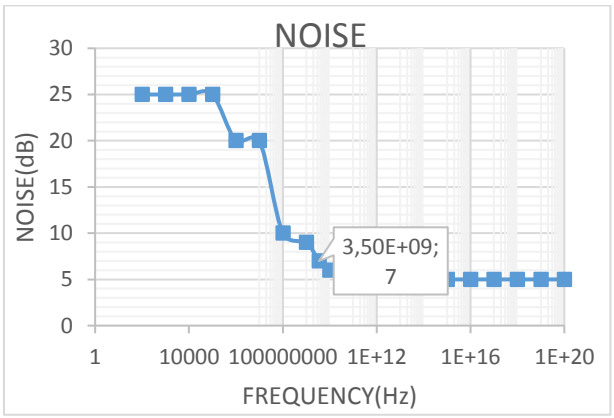


Figure 7: Noise analysis of the circuit

Noise analysis at 3.5GHz i.e at 5G spectrum it is 7 dB, which is low in comparison other lower frequencies. It is seen in figure 7.

3.2 SECTION B

The proposed circuit, is further designed with a linearization circuit to increase the linearity which will make the system more robust from distortion. This is shown in figure 8.

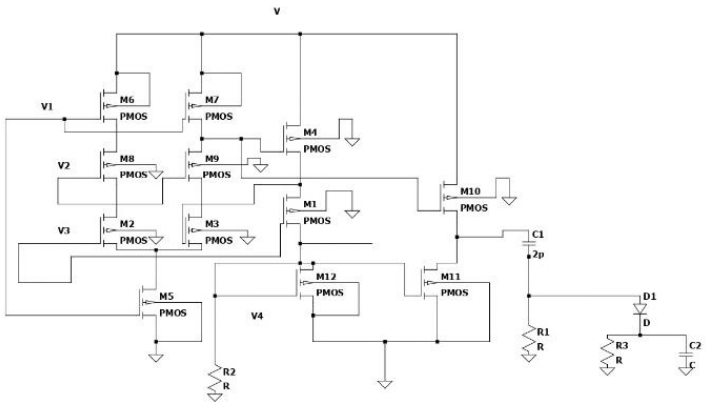


Figure 8 circuit diagram with linearity circuit

EXPERIMENTAL RESULT OF SECTION B

After employing the linearization technique, the circuit gain is further investigated and observed that at 3.5GHz, the gain is increased to 15.71dB. This can be confirmed from the figure 9. The noise analysis is also done, which is depicted in figure 10 gives the same outcome as that of the previous circuit.

The linearity increases after designing the circuit is achieved by partially cancelling the contribution from 2nd-order nonlinearity to IM3 product, resulting in a small IM3 product at the output. The slope of the graph increases and hence the linearity. This is presented in figure 11.

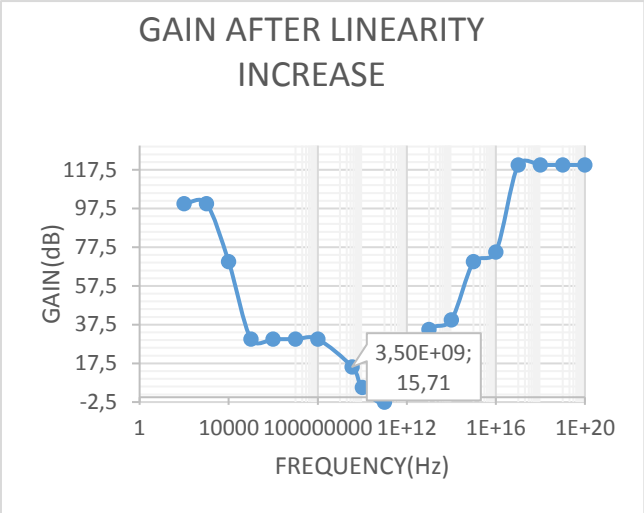


Figure 9: Gain after linearization

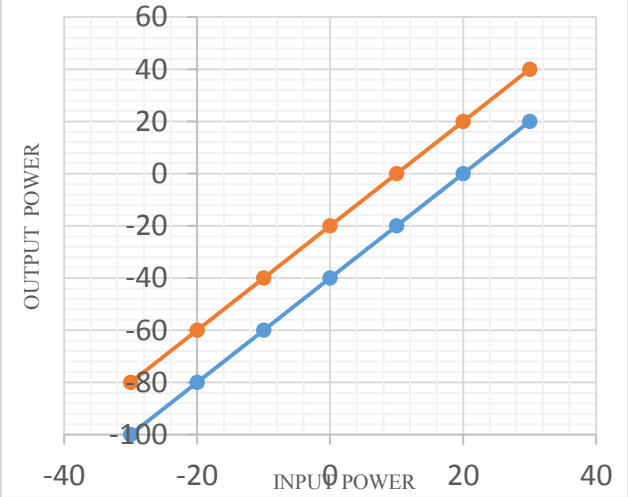


Figure 10: Linearity plot

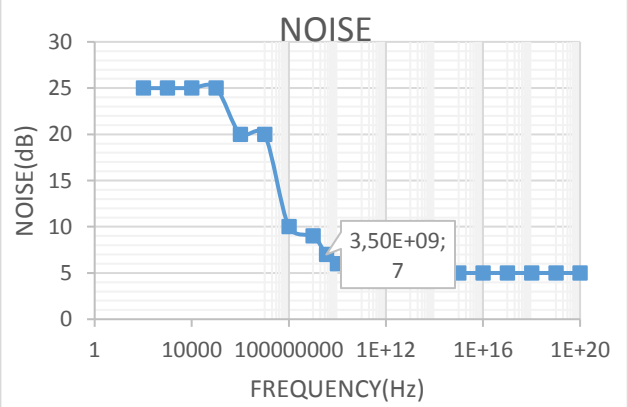


Figure 11: Noise analysis

The outcome of both the design can be summarized in table 1.

Table 1: Summary of output parameters

WORK	Frequency of operation	GAIN (dB)	No. of Transistors	Noise (dB)	No. of Inductor
A	5 GHz	11.147	11	7	0
B	5 GHz	15.71	11	7	0

We have compared the performance of the proposed circuit with other contemporary works and is presented in table 2. This clearly reflects efficacy of our design in terms of gain while making it inductor-free.

Table 2 Performance comparison with other contemporary works

Paper	Gain	No. of Transistor	Noise Figure	No of Inductors	Frequency
[2]	15.4	6	1.36	4	3 GHz
[1]	8.1	8	2.2	8	10GHz
[3]	18.6	8	4.9	4	1 GHz
[5]	`11	8	2	4	4 GHz
This work	**15.17**	**11**	**7**	**0**	3.5 GHz

4 Conclusion

In this implementation we have achieved a Gain of 11.147dB without linearity and 15.17 dB with linearization. It successfully used common drain output configuration to have a stable output and impedance matching to make frequency and BW suitable for 5G communication. The significance of this design lies in the fact that the design is completely inductor less which will contribute towards an area efficient design that will in turn make it cost efficient too. Moreover the number of transistors required is also not very high and it is achieved while maintaining the other parameters at par with other designs. The linearization technique used here makes the design less prone to distortions. The frequency of operation and the BW is sufficiently high. The noise margin is acceptable but has further scope of improvement.

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