

# An Analogue Multiplier using CNTFET Technology

SEYEDEHSOMAYEH HATEFINASAB

Department of Materials Science, Faculty of Science and Technology  
NOVA University of Lisbon, Lisbon,  
PORTUGAL

**Abstract:** The endeavor to overcome problems of complementary metal oxide semiconductor technology makes the advent of Carbon nanotube field effect transistor (CNTFET). Improvement of structure transistor CNTFET makes higher mobility and electrostatics of gate electrons. Therefore, many analog circuits are now designed based on CNTFET technology. This paper presents a low power current mode four-quadrant analog multiplier based on CNTFET and CMOS technologies. All simulations were done with the synopsys Hspice simulator using 32nm CNTFET model from Stanford University and 32nm CMOS from PTM library at a supply voltage of 3.3 v. It was shown that the simulation of a multiplier based on CNTFET technology performs better than a multiplier based on CMOS technology.

**Keywords:** carbon nanotube field effect transistor; analog multiplier; low power; single-walled CNT.

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## 1 Introduction

CMOS (complementary metal oxide semiconductor) technology has continued to scale down below 32nm. A reduction in the size of transistors may cause several problems in nanoscale. Therefore, the need for new technologies to improve the structure of nano-scale transistor increases a lot. One of the best structures of nano-scale transistors is carbon nanotube field effect transistor (CNTFET) [1]. The thermal and mechanical characteristics of CNTs, such as current density, transconductance and lower parasitic capacitance make this nanotechnology better than other technologies in nanoscale integrated circuit. This creates the platform for many integrated circuits to be simulated based on CNTFET technology such as logic gates in VLSI [2] and analog circuits in radio frequency (RF) devices [3].

One of the basic blocks in analog circuits is a multiplier and it is the most important part of adaptive filters, modulators, signal processing circuits and fuzzy logic controllers. An ideal multiplier produces a linear output signal which is obtained from two linear input signals with a constant designated as  $k$  [4]. The analog multiplier can be divided into two groups, voltage mode [5] and current mode [6-8].

This paper presents a low power and high-speed four-quadrant analog multiplier in the current mode based on dual translinear loops using 32nm CMOS and 32nm CNTFET technologies. Since different parameters of low-voltage circuits can be improved by enhancing the technology at the nano-scale, CNTFET technology is applied. All the simulations were performed using Hspice with 32nm CMOS from PTM library and 32nm CNTFET from Stanford University technologies.

## 2. Background

### 2.1. Carbon Nano Tubes Field Effect Transistor

Single carbon nanotube (SWCNT) is a rolling sheet of graphene with specific direction which is called chirality vector  $\vec{C}_h$ . Chirality vector shows the angle of the carbon to carbon (c-c) atoms. The length of the chirality vector can be calculated as shown in Eq.1 [9].

$$C_h = \alpha \sqrt{n_1^2 + n_2^2 + n_1 n_2}.$$

Where  $\alpha$  is the lattice constant which is equal to 0.249 nm,  $n_1$  and  $n_2$  are pairs of integer numbers which are dependent on the chirality vector. CNT is metallic if  $n_1 - n_2 = 3i$  ( $i \in \mathbb{Z}$ ), and other modes are semiconductor. The tube diameter ( $D_{CNT}$ ) is determined as shown in Eq.2 [9].

$$D_{CNT} = \frac{C_h}{\pi}.$$

The structure of a CNTFET transistor is similar to that of a CMOS transistor, but the channel of CNTFET transistor is carbon nanotubes as shown in Fig 1. Electrons move fast in the carbon nanotubes, so the mobility factor increases rapidly as a ballistic transport [10]. But current leakages reduce because of less parasitic parameters. In a CNTFET transistor, the number of tubes is determined by the drive current.

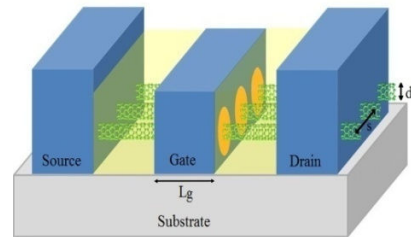


Fig 1. Three demintional CNTFET structure with multiple nanotubes.

There are three types of CNTFET transistors based on their structures. First, CNTFET transistors have the same structure as CMOS transistors. This kind of CNTFET transistors donot have any differences between n-channel and p-channel. Fig 1 shows this kind of CNTFET transistor. Second, CNTFET transistors are Schottky barrier (SB) with direct tunnels at the junction of the source-channel. The application of this kind of CNTFET transistors is in the RF frequency devices [11-12]. Third, band-to-band tunneling CNTFET transistors. The current passes through the tunnels. The best application of these transistors at the low voltage [13].

### 2.2. Analog Multiplier Design Theory

One of the most important fundamental blocks in analog integrated circuits is a multiplier. The one of the best CMOS based current mode four-quadrant analog multipliers is shown in Fig 2 [14]. The two signals which are multiplied are not entered directly. The addition and subtraction of two signals which are multiplied are entered. If the circuit designed produces the square of each inputs and subtraction of these squares, the output signal of a four-quadrant analog multiplier is multiplication of two signals determined, which is written as shown in Eq.5. The circuit in fig 2 can produce these equations, which are explained in [14].

$$I_{in1} = I_x + I_y. \tag{3}$$

$$I_{in2} = I_x - I_y. \tag{4}$$

$$(I_{in1})^2 - (I_{in2})^2 = \frac{(I_x+I_y)^2 - (I_x-I_y)^2}{I_b} = kI_xI_y \tag{5}$$

Where  $I_b$  represents a constant current in a multiplier. The use of appropriate input signals makes this circuit operate as a multiplier. All transistors in the inversion region are applied to prove that this circuit works as a CMOS multiplier. If this multiplier is implemented by using CNTFET technology, the above equations can be applied. Also, The relationship between the source-drain current and the gate-source voltage applied in the saturation region of CMOS technology can be applied for CNTFET technology. Therefore, the relationship between the input signals and the output signal of this circuit in CNTFET technology is a multiplier.

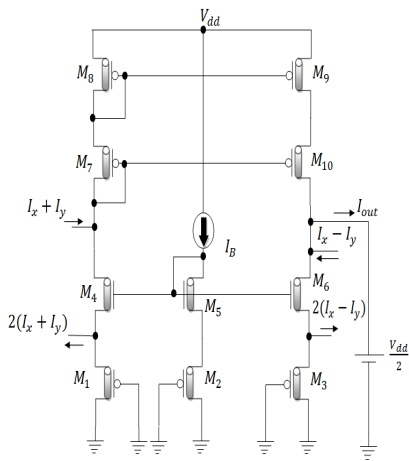


Fig 2. A CNTFET based four-quadrant analog multiplier.

$$v_{th} = v_{th0} + \gamma \left( \sqrt{|2\phi_B + v_{SB}|} - \sqrt{2\phi_B} \right). \tag{6}$$

### 2.3. Second Error Effects

This multiplier circuit has many errors. The most important of them are mismatches, channel effect modulation, body effect and mobility degradation, but these errors can be neglected because the value of these errors is smaller than the mean signals in a multiplier. In addition, a multiplier that uses CNTFETs has fewer errors introduced by the second error effects of CMOS technology. In this CMOS-based multiplier structure, m1, m2 and m3 transistors can be built in different wells; therefore, the body effect ( $\gamma$ ) can become zero in m1, m2 and m3 transistors. Therefore, Eq 6 can be simplified to  $v_{th} = v_{th0}$ . But, the body effect is not zero for m4, m5 and m6 transistors because they can not be built in different wells. Thus there is a different voltage between bulk and source in each m4, m5 and m6 transistors, which means  $v_{SB}$  is not zero in these three transistors. The body effect error is important in CMOS-based transistors because this voltage affects the threshold voltage of transistors ( $v_{th}$ ) as shown in Eq 6.

Where  $v_{th0}$  is the zero bias threshold voltage,  $\phi_B$  is the bulk potential and  $\gamma$  is the body effect coefficient. In CNTFET transistors, the voltage threshold is inversely proportional to the nanotube diameter ( $D_{cnt}$ ) as shown in Eq 7.

$$V_{th} = \frac{0.42}{D_{cnt(n_1, n_2)}} v. \quad (7)$$

Therefore, the threshold voltage can be determined by the nanotube diameter in CNTFET transistors.

Mismatch of transistors is the second most important error. The design of this multiplier is assumed that all the transistors are well matched,  $k_n = k_p$ . But, in the reality, all transistors are asymmetric ( $k_n \neq k_p$ ). In general, in silicon CMOS technology, the NMOS mobility is about 2 or 3 times higher than the PMOS mobility. However, in CNTFETs structure, p-CNTFET and n-CNTFET have the same transport carrier and transistor geometry.

#### 2.4. Leakage

Total power consumption in integrated circuits results in three power consumptions including short circuit current that leads the power consumption, static power consumption and dynamic power consumption. The appropriate circuit technique can reduce the short circuit current, however, the static power consumption of the nano-scale circuits is very high. Therefore, traditional methods used to decrease static power are not very effective. In CMOS transistors, static power consumption can be indicated by some factors such as sub-threshold, gate tunneling and reverse-biased junction band-to-band tunneling leakage current. However, in CNTFET transistors, a band-to-band tunneling leakage current is the main factor

that determines the current leakage. The current leakage is indicated by the full band gap of the CNTs and the band-to-band tunneling. In table 1, the power consumptions of the current mode four-quadrant analog multipliers using CMOS and CNTFET are highlighted.

### 3 Simulation Results

The multiplier circuit was simulated with the Synopsys Hspice simulator using 32nm CNTFET model from Stanford University and 32nm CMOS from PTM library at a supply voltage of 3.3 v. In both simulations of the multiplier using CNTFET and CMOS, the output nodes of the circuits were connected to a power source voltage with approximately  $v_{dd}/2$  volt. In the multiplier,  $I_B$  is a constant current equal to  $10\mu A$ . Fig 3 shows the DC transfer characteristics of a multiplier using 32nm CNTFET and 32nm CMOS. These figures show more linearity of the CNTFET based multiplier over a considerable range of inputs ( $-10\mu A$  to  $10\mu A$ ) which have a maximum value that is equal to  $\pm I_B$ . The output signal range of a multiplier using 32nm CMOS is between  $-7\mu A$  and  $7\mu A$ , but the output signal range of a multiplier using CNTFET technology is between  $-10\mu A$  and  $10\mu A$ . Since the input signal range is equal, the multiplier that uses CNTFETs shows a higher range of output signals than the CMOS based multiplier because a CNTFET based multiplier possesses more linearity.

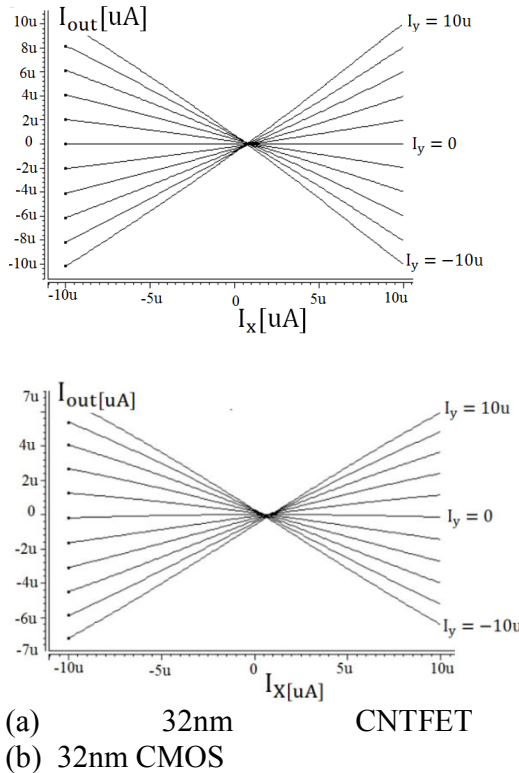


Fig 3. (a) DC transfer characteristic of a CNTFET based multiplier (b) DC transfer characteristic of a CMOS based multiplier.

In addition, a better linearity of the multiplier in CNTFET technology can be indicated in the transient simulation. The input signals of a multiplier,  $I_x$  and  $I_y$  are two sine signals. Fig 4 shows the output signals and the same input signals,  $I_x$  and  $I_y$ , for a multiplier in CNTFET and CMOS technologies. As seen in Fig 4, the output signal of the CNTFET based multiplier looks closer to an ideal output signal than that of the CMOS based multiplier. This better result of a CNTFET based multiplier in comparison with a CMOS based multiplier can be shown by transient error simulation and total harmonic distortion (THD). Fig 5 shows the error of this multiplier using CNTFET and CMOS in which a CNTFET based multiplier has less

error in comparison with a CMOS based multiplier.

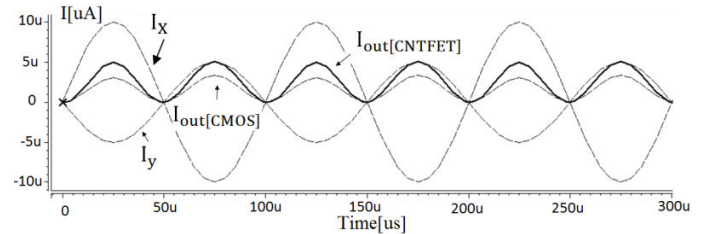


Fig 4. Simulation results for a transient analysis.

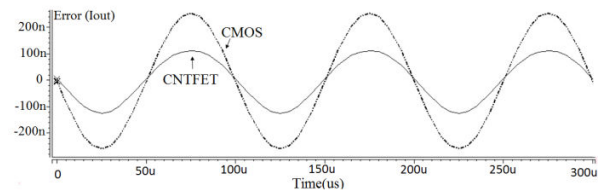


Fig 5. Simulation results for error of a transient analysis.

THDs of the multiplier using CMOS and CNTFET were calculated in three input signal frequencies such as 1MHz, 100MHz and 1GHz. The simulation results are shown in Fig 6. Comparison between the proposed multiplier and previous works are shown in Table 1.

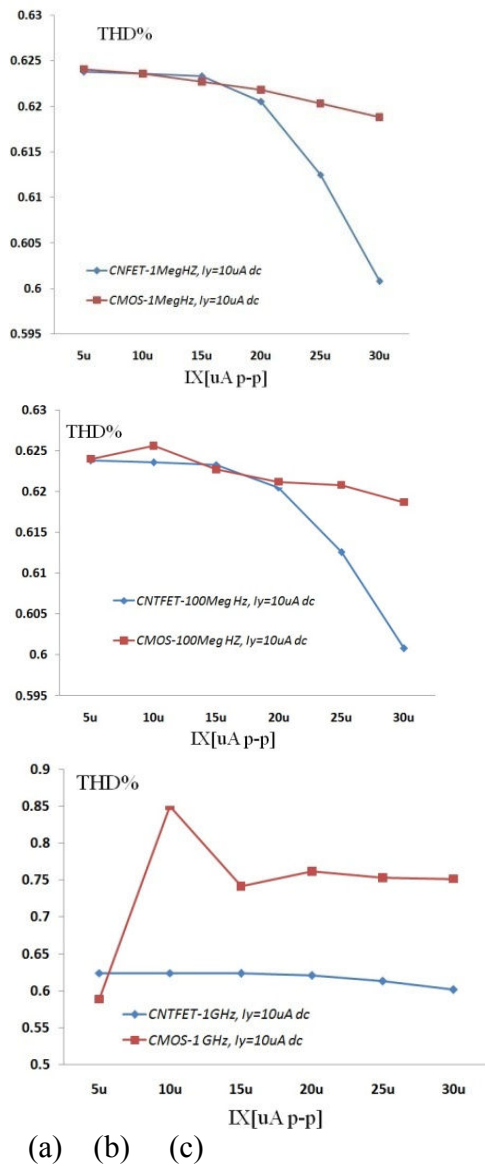


Fig 6. (a) Total harmonic distortion versus input currents at 1 MHz. (b) Total harmonic distortion versus input currents at 100 MHz. (c) Total harmonic distortion versus input currents at 1 GHz (various amplitudes of I<sub>x</sub> signal and a fixed amplitude of I<sub>y</sub> signal).

Fig 7 shows the -3db bandwidths of the multiplier using CNTFET and CMOS technologies. As can be seen, the -3db bandwidth of the CNTFET based multiplier is 110GHz, although the bandwidth of the CMOS based multiplier is approximately 2.45GHz. The CNTFET multiplier does not have any attenuation, but the CMOS multiplier has a 5db attenuation as can be seen in Fig 7.

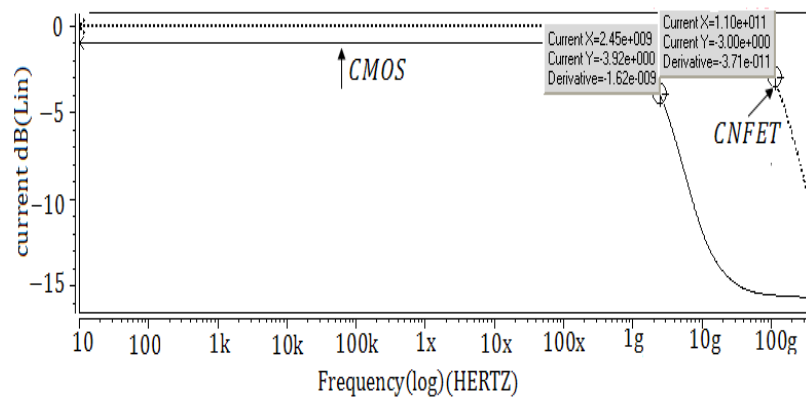


Fig 7. Simulation results for -3db bandwidth.

Table. 1 A comparison between this work and previous works.

Four-quadrant analogue multiplier	[15]	[16]	[14]	This article (cmos tech)	This article (CNTFET tech)
Technology	0.35um CMOS	0.35um CMOS	0.25um CMOS	32nm CMOS	32nm CNTFET
Power[ $\mu$ w]	5.5	340	214.5	185	99.4
I baise[ $\mu$ A]	0.25	10	10	10	10
v supply[v]	2	3.3	3.3	3.3	3.3
Thd [%]1 MHz, 20 $\mu$ A	1(1kHz)	0.97	0.96	0.6218	0.6205
-3db bandwidth	0.2	41.8	533	2450	110 GHz

## 4 Conclusion

This paper presents a current mode four-quadrant analog multiplier using CNTFET and CMOS technologies. At the same power supply, the simulations are calculated using hspice. A CNTFET based multiplier circuit has better features in comparison with a CMOS based multiplier, which includes high speed, high linearity, low power consumption in transient and dc simulations. A comparison between this work and

previous works shows improvements in many parameters including THD, -3db bandwidth in AC analyzes.

## 5 References

- [1] Paul, L.; McEuen, P.L.; Fuhrer, M. S.; Park, H. The Single-walled carbon nanotube electronics. IEEE Transactions on Nanotechnology 2002, vol. 1, 78–85.

- [2] Seyedehsomayeh Hatefinasab, " CNTFET-Based Design of a High-Efficient Full Adder Using XOR Logic " *Journal of Nano- and Electronic Physics* Vol. 8 No 4(2), 04061(6pp) (2016).
- [3] B. Heidari, M. Kord Rostami, High Performance Current-Mode Multiplier Circuit based on Carbon Nanotube Transistors, *IJAENT*. (2014) 2347-6389.
- [4] B. Gilbert, A precise four quadrant multiplier with sub nanosecond response, *IEEE J Solid-State Circ.* (1986) 430–5.
- [5] C. Chen, Z. Li, A low-power CMOS analog multiplier, *IEEE Trans Circ Syst II: Exp Briefs*. (2006).
- [6] M. Gravati, M. Valle, G. Ferri, N. Guerrini, L. Reyes, A novel current-mode very low power analog CMOS four quadrant multiplier, *IEEE proc ESSCIRC*. (2005).
- [7] A. Naderi, A. Khoei, K. Hadidi, H. Ghasemzadeh, A new high speed and low power four quadrant CMOS analog multiplier in current-mode, *Int J Electron Commun (AEÜ)*. (2009) 769-75.
- [8] F.A. Usmani, M. Hasan, Carbon nanotube field effect transistors for high performance analog applications: An optimum design approach, *Microelectronics Journal*. (2010) 395–402.
- [9] J. Deng, H. S. P.Wong, A compact SPICE model for carbon nanotube field effect transistors including non-idealities and its application—Part I: Model of the intrinsic channel region, *IEEE Transactions on Electron Devices*. 54 (2007) 3186–3194.
- [10] P.L. McEuen, M. S. Fuhrer, H. Park, The Single-walled carbon nanotube electronics, *IEEE Transactions on Nanotechnology*. (2002) 78–85.
- [11] P.L Gowri Sankar, K. Udhayakumar, MOSFET-like CNFET based logic gate library for low power application: a comparative study, *Journal of Semiconductors*. 35 (2014).
- [12] Zarhoun, R.Moaiyeri, M.H. Hossein Farahani, S. Shirinabadi, N. Keivan, An Efficient 5-Input Exclusive-OR Circuit Based on Carbon Nanotube FETs, *ETRI Journal*. (2014).
- [13] A. Raychowdhury, K. Roy, Carbon Nanotube Electronics: Design of High Performance and LowPower Digital Circuits, *IEEE Trans. Circuits Syst I*. 54 (2007) 2391-2401.
- [14] A. Alikhani, A. Ahmadi, A novel current-mode four-quadrant CMOS analog multiplier/divider, *Int. J. Electron. Commun (AEÜ)*. 66 (2012) 581– 586.
- [15] M. Gravati, M. Valle, G. Ferri, N. Guerrini, L. Reyes, A novel current-mode very low power analog CMOS four quadrant multiplier, *IEEE proc ESSCIRC*. (2005).
- [16] A. Naderi, A. Khoei, K. Hadidi, H. Ghasemzadeh, A new high speed and low power four quadrant CMOS analog multiplier in current-mode, *Int J Electron Commun AEÜ*. (2009) 769–75.