

Yield Enhancement in Wafer Manufacturing Through Applying Statistical Process Control Concepts

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Abstract: - Although semiconductor fabrication has advanced significantly in recent years, manufacturing lines frequently encounter operational inefficiencies when processing highly specialized or non-standard substrates. These disruptions degrade overall line performance and ultimately reduce product yield. This issue is equally pronounced at the single-device level, where performance degradation and elevated defect rates necessitate substantial resource allocation for post-fabrication screening and inspection to prevent faulty components from reaching end users. The better practice is to try and discover, and consequently, eliminate the bad devices before they run through multiple processes, costing time and money towards a useless end. In some cases, the solution to overcome these difficulties becomes as costly as it involves modification of properties at the individual device level. This in turn saves the product quality, but still consumes resources to a point making the production process marginally profitable. A better solution to such problem is one that approaches the wafer as a whole and not at the device level. Given that these wafers typically accommodate roughly a thousand individual devices, adopting a global, wafer-level approach becomes highly advantageous. This paper addresses a real-world industrial challenge encountered during wafer fabrication when attempting to meet strict target specifications. This issue consistently arises in wafers processed via evaporated metal thin-film deposition. A prominent example of such components includes passive filters designed around Surface Acoustic Wave (SAW) principles. A solution that replaces the existing custom-made one is proposed. This solution eliminates approaching every device on the wafer individually and looks at the wafer as a whole. The proposed solution applies a statistical approach to the problem using the concepts of statistical process control. Implementing this solution yields substantial improvements, including a marked increase in product yield, significant cost reductions, and the successful integration and promotion of process automation.

Key-Words: - SAW devices, Wafer Fabrication, Statistical Process Control (SPC), Mass Production line Yield, etching, Center Frequency.

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1 Introduction

Manufacturing processes efficiency is measured by their yield. To improve production yield in electronic wafer fabrication, millions of dollars are spent to govern the manufacturing process and keep it running within the process specifications. During semiconductor fabrication, each wafer progresses through a sequential manufacturing line a single time. Because a single wafer typically accommodates approximately one thousand individual components, the quality of each discrete device directly influences the final overall yield, which serves as the primary metric for the chip fabrication process. This introduces the need to individually verify the quality of each device. While laboratory-scale solutions proposed by specialists

successfully optimize individual device performance, scaling these methods to mass production introduces a new set of operational challenges. This is because of the immanent effect they have on the surrounding population of devices. If each device is to be modified individually, the cost of manufacturing would exceed all limits, making the process unprofitable. A prominent case study illustrating these manufacturing constraints occurs during the production of wafer chips featuring Surface Acoustic Wave (SAW) IC's. Largely implemented in telecommunication circuits due to their high precision as resonators, oscillators, and filters, these components are typically manufactured by depositing a thin metal film onto piezoelectric substrates such as Lithium Niobate (LiNbO3) or quartz using sputtering or evaporation

techniques. The specific components investigated in this study comprise evaporated aluminum structures on a quartz substrate. Given the exceptionally narrow frequency margins required for these applications, achieving high manufacturing yields remains a persistent challenge. Device-level performance variations stem primarily from inherent fluctuations across the manufacturing processes, including metal deposition non-uniformity, photolithographic tolerances, and etching capabilities. Within the context of SAW architectures, even minor deviations in film thickness, groove depth, or geometric features shift the operational frequency away from target specifications. While extensive literature has sought to mitigate this issue, historical efforts have predominantly focused on localized tuning procedures targeting the center operating frequencies of discrete devices [1], [2]. Similar methodologies have addressed this issue by introducing plasma etching techniques at the individual chip level [3], [4]. While SAW researchers have introduced alternative solutions capable of being integrated as post-fabrication manufacturing steps, these approaches generally require an additional development phase to effectively treat the wafer fabrication sequence as a holistic, unified process. The most important implication resulting from missing the global approach is the huge rise in capital investment and production cost.

This work examines the challenges related to implementing chip-level methods within the high-volume production line of SAW devices, and proposes a practical alternative to mitigate operating frequency shifts. By addressing these variations at the mass-production scale rather than treating individual components, the proposed methodology directly enhances fabrication line efficiency. Consequently, this holistic approach yields substantial improvements in manufacturing throughput, cost reduction, and overall device quality.

2 SAW Devices

Surface acoustic wave (SAW) technologies have expanded well beyond their traditional role as radio-frequency (RF) filters, evolving into a versatile platform for diverse applications in telecommunications, microfluidics, sensing, and advanced manufacturing. Acoustic wave propagation within solid media is generally categorized into surface and bulk waves based on the nature of the energy confinement. As elastic

waves, SAWs propagate along the substrate boundary, with exponential decay in amplitude as advance into the depth of the medium. Consequently, the vast majority of acoustic energy remains localized at the surface. Documented applications of these devices span from Telecommunications & RF Front-Ends, Analog Signal Processing [5], [6], Base Stations & Satellite Systems, Radar & Electronic Warfare, Passive Sensors [7], [8], and more recently, Quantum Control and Single-Electron Transport [9], [10]. SAW devices are typically manufactured by fabricating metal thin-film grating structures on a piezoelectric substrate. The precise thickness of finger gratings, alongside the intervening cavity depth and length, establishes a narrow passband for the device. Figure 1 illustrates a typical SAW resonator configuration, where a central resonant cavity is sandwiched between two identical reflector grating arrays. However, a significant portion of fabricated devices exhibit frequency dispersion levels that exceed strict application tolerances. As previously noted, these deviations stem directly from irregularities inherent to standard manufacturing processes, where photolithographic, etching, and thin-film deposition variations introduce localized frequency shifts. To mitigate these discrepancies, post-fabrication dry etching is frequently utilized as a frequency-trimming technique.

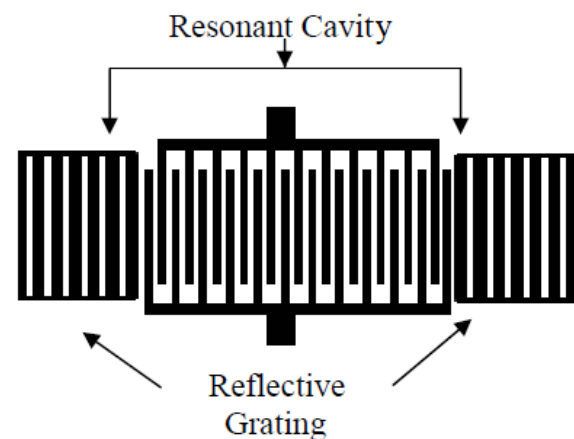


Fig. 1: Typical SAW resonator

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Frequency trimming is utilized by changing the groove depth of the substrate through the metal gratings via a dry etching process using Tetrafluoromethane CF_4 gases and oxygen. During this procedure, the aluminum electrodes serve as a self-aligned mask while etching occurs on the exposed quartz substrate. This methodology

leverages the highly comparable densities of aluminum and quartz ($\rho_{\text{Quartz}} = 2.65 \text{ g/cm}^3$; $\rho_{\text{Al}} = 2.7 \text{ g/cm}^3$), meaning that recessing the grooves yields an acoustic loading effect equivalent to thickening the metal layer. Because the quartz etch rate under these conditions is approximately 100 times faster than that of aluminum, the process provides an exceptionally selective and practical mechanism for final specification adjustments. Ultimately, this structural modification decreases the resonance frequency of the device, as governed by equation (1).

$$V = V_p \left[\frac{1 + \frac{2d}{\lambda} \left(-5.8 \times 10^{-4} - \frac{0.2(h+h_1)}{\lambda} \right)}{-3.5 \left(\frac{(h+h_1)}{\lambda} \right)^2} \right] \quad (1)$$

Here, V represents the acoustic wave velocity, V_p denotes the acoustic wave velocity within the piezoelectric material, d is the electrode width, and h is the electrode thickness. Figure 2 illustrates the cross-sectional geometry of the etched SAW structure, where h_1 corresponds to the additional depth induced by the quartz etching process. To determine the resulting resonant frequency shift, the following empirical formula is conventionally applied:

$$\frac{\Delta F}{F} = \left(\frac{-h}{\lambda^2} \right) (0.4d + 7h + 3.5h_1) \quad (2)$$

The plasma etching process is conducted within a vacuum chamber under continuous gas evacuation.

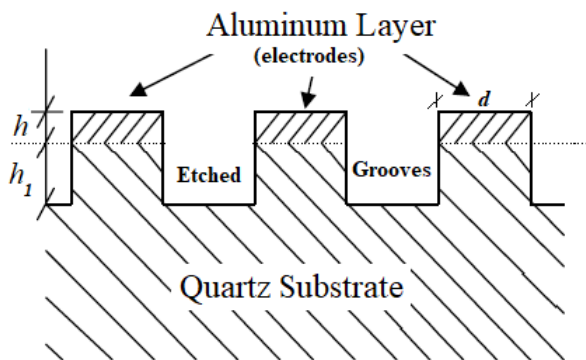


Fig. 2: Cross Section of plasma etched SAW device. The etched grooves are in the substrate

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2.1 Problem Description

Current industry practice involves characterizing device performance post-dicing, followed by individualized dry etching as a trimming step. This

approach necessitates specialized, custom-built machinery, which imposes a substantial cost penalty on high-volume manufacturing lines. For context, frequency-trimming a batch of one thousand components requires approximately 50 hours of processing time [2], escalating unit production costs by roughly 150%. Consequently, this methodology demands prohibitive capital expenditures and intensive routine maintenance, severely marginalizing process profitability. The manufacturing equipment typically features a multi-chamber configuration where devices are isolated via automated shutters. While a cluster of 24 to 36 devices undergoes parallel plasma processing, individual shutters actuate independently once a specific device reaches target specifications. This operational complexity drives up maintenance overhead, requiring daily calibration and servicing. Machine components require frequent replacement due to continuous plasma exposure, which strictly limits material selection to specialized variants, precluding the use of standard components like conventional rubber seals or generic bearings. Furthermore, cross-contamination and plasma leakage frequently occur when a shutter actuates for one chamber while active etching continues in an adjacent node, due to containment difficulties.

To address these inefficiencies, this work introduces a scalable alternative to conventional post-dicing tuning. By analyzing and mitigating these systemic production line bottlenecks, this paper demonstrates a highly optimized, high-yield methodology designed to restore manufacturing profitability.

Conventional fabrication workflows require individual device performance to be characterized pre and post post-dicing, followed by customized dry etching as needed to trim the frequency. This individualized approach depends on highly specialized, custom-built machinery, making dry etching a primary cost driver in high-volume production line manufacturing environments. To put this in perspective, processing a batch of just one thousand devices demands approximately 50 hours of total trimming time and a capital expenditure for specialized equipment about US\$1.6 million [2]. Consequently, this process drives a 150% increase in unit production costs, necessitating a substantial upfront capital investment. The required instrumentation demands continuous maintenance and significantly inflates operating costs, severely constraining profitability. In this legacy setup, machines utilize a multi-chamber design where individual devices are isolated behind automated shutters. While a batch of devices undergoes

concurrent dry etching, each chamber's shutter is independently triggered once that specific device converges on target specifications. This architecture introduces severe maintenance liabilities, requiring daily calibration and servicing. Because components are subjected to relentless plasma exposure, they degrade rapidly and require frequent replacement. This harsh environment strictly limits material selection; for instance, standard rubber seals and generic bearings degrade too rapidly to be viable. Furthermore, structural challenges like plasma leakage frequently occur when a single chamber shutter is actuated while adjacent chambers are actively etching, primarily due to the physical difficulty of isolating localized plasma fields. To address these manufacturing bottlenecks, this work introduces an alternative framework designed to comprehensively optimize mass production. By diagnosing and addressing the root vulnerabilities of the existing production line, this approach establishes a highly profitable manufacturing methodology optimized for maximum volumetric yield.

2.2 Proposed Solution

The methodology proposed herein adopts a holistic framework that evaluates the collective ensemble of devices on a wafer as a unified entity, thereby offering broad compatibility with diverse surface acoustic wave (SAW) device fabrication protocols. By treating the wafer in its entirety, this approach effectively obviates the requirement for highly specialized instrumentation and intricate setup configurations. Theoretically, maintaining stringent statistical control and continuous monitoring across the sequential stages of the manufacturing line ensures that the constituent devices exhibit highly uniform, or nearly identical, performance characteristics. Prior to the etching phase, the devices undergo in situ evaluation via an automated probing station, which yields a comprehensive statistical distribution of their baseline attributes. Within this paradigm, the center frequency serves as the primary parameter of interest. Consequently, a rigorous analysis of the standard deviation and the mean of this distribution provides a precise information of the requisite CF shift to be achieved during etching, ultimately ensuring that the finalized components conform to established performance specifications. The efficacy and viability of this framework fundamentally depend upon its deterministic impact on the broader device population and its inherent repeatability, wherein systematic shifts in the population's statistical

profile serve as the primary metric for process regulation.

3 Experimentation and Process Model

Surface acoustic wave (SAW) devices fabricated via electron-beam evaporation often exhibit unstable performance metrics across successive manufacturing and testing stages, leading to inconsistent outcomes during center frequency trimming and a failure to maintain baseline production specifications. To mitigate this instability and stabilize the metallic film on the substrate, an annealing step at 350°C was integrated into the workflow [5]. Evaluation across three distinct wafers containing 753 individual devices demonstrated that the mean center frequency shifts exponentially over time, achieving 95% of its total 118 kHz stabilization shift value within 40 minutes, after which device characteristics remain entirely static. The results of these evaluations illustrated in Figure 3.

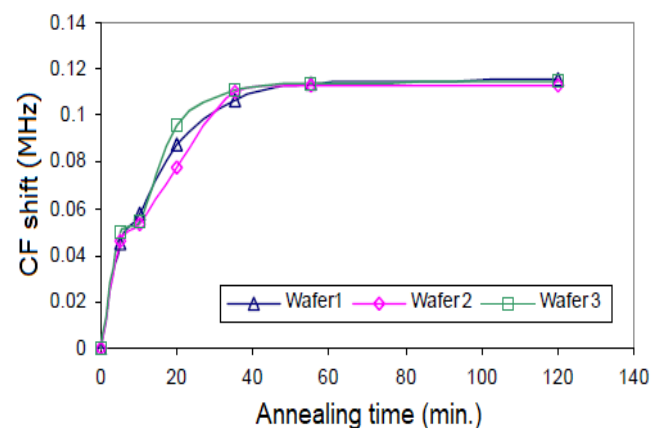


Fig. 3: Annealing time effect on center frequency shift for different wafers.

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Consequently, subsequent thermal exposure at or below the 350°C threshold does not degrade the performance of these devices. Given this robust thermal stability, the annealing process has been standardized across all production wafers prior to center frequency trimming. Notably, this thermal treatment induces a general upward shift in the wafer's center frequency. Mechanistically, annealing relieves internal stresses within the evaporated metallic film and eliminates inter-atomic voids. The inherent instability of the un-annealed film stems from the e-beam deposition process, which lacks the high-energy atomic bombardment characteristic of sputtering. This milder deposition allows random gaps and structural voids to form in the metal film

between atoms, ultimately altering the density of the metallic film until stabilized by the thermal process. Consequently, this structural instability manifests physically during operation, inducing a perceptible shift in the Center Frequency (CF) of the SAW device. The thermal treatment also reduces the electrical resistance of the metallic film, compounding the previously noted factors that drive the operating frequency upward. To evaluate how frequency trimming via etching affects the individual characteristics across a single wafer, a sample consist of over 700 devices was put in the etching chamber. Prior to the process, the baseline center frequency of each device was mapped. Etching was then executed sequentially on the same wafer for intervals of 70 seconds, 30 seconds, and 175 seconds, with the updated frequencies recorded after each step. The resulting dataset is illustrated in Figure 4.

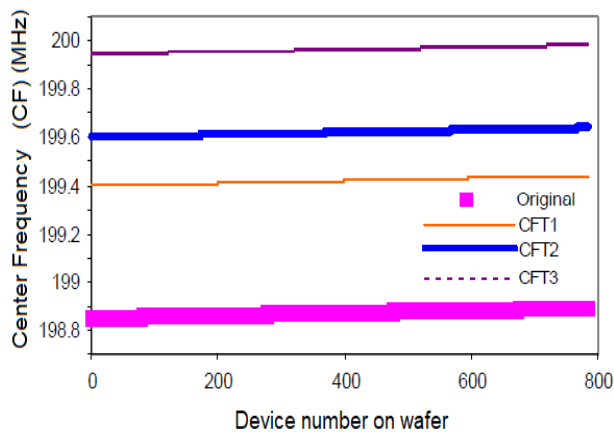


Fig. 4: CF shift for every individual device on the wafer after 3 etching trials.
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As illustrated in Figure 4, the device population across the wafer experiences a uniform and highly consistent center frequency shift during the etching process. This high degree of repeatability enables sequential trimming cycles to be performed until the target center frequency is precisely achieved, without compromising the overall characteristics of the wafer. These empirical findings strongly validate the hypothesis that wafer-level devices can be governed statistically as a collective population, bypassing the need for individual device trimming. Leveraging this structural consistency, an empirical model was developed to simulate the relationship between etching duration and the manufacturer's target frequency shift. The experimental data underlying this model are plotted in Figure 5, which comprises 20 distinct data points; each point represents the mean center frequency of a wafer

averaged across three separate measurement trials. A second-order polynomial regression provided the optimal fit for this relationship, yielding equation (3) as follows:

$$T = 15.67 + 0.24 CFS + 8 e^{-5(CFS)^2} \quad (3)$$

where T denotes the trimming duration in seconds, and CFS represents the target center frequency shift in kilohertz (kHz).

By utilizing this empirical model, the desired frequency adjustments can be precisely executed through the deterministic control of the etching interval. It is worth noting that this model can only be used for the etching setup system that is used in this experiment and can't be generalized to all etching systems. However the statistical approach method is applicable to similar situations and can be used keeping in mind that equation similar to equation 3 has to be fitted for each etching chamber and can be used later in the manufacturing process. Because of this fact expanding the mathematical analysis by providing rigorous derivations of the proposed model, or formal proofs of the mathematical model is not useful in this case.

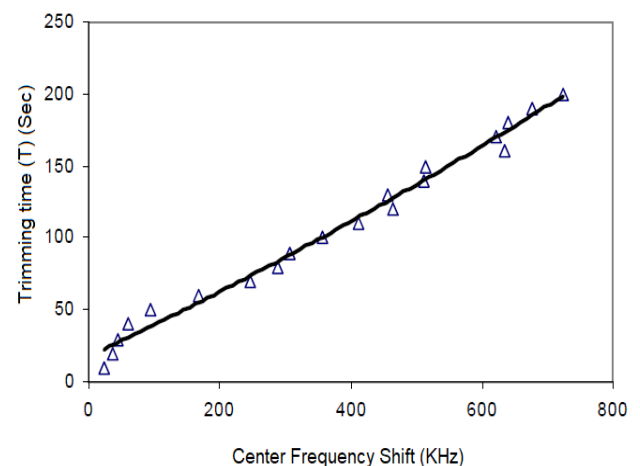


Fig. 5: The relation between plasma etching time and CF shift (model equation).
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4 Application and Results

Guided by these empirical insights, the production workflow was modified to treat the wafer as a collective unit throughout the post-deposition phases. Under this optimized sequence, the entire wafer undergoes initial thermal annealing, followed by a targeted etching cycle for a duration derived directly from equation (3). The required trimming interval is calculated based on the mean center

frequency of the wafer population recorded post-annealing. To demonstrate this manufacturing protocol, Figure 6 illustrates the execution steps applied to a randomly selected production wafer. Following the annealing stage, the wafer exhibited a baseline mean center frequency of 199.94 MHz. The wafer was then etched to achieve a primary target frequency of 199.62 MHz. Subsequent trimming cycles were performed to shift the mean center frequency to a secondary target of 199.42 MHz, and ultimately to a final target of 198.92 MHz. For this entire operations sequence, the upper and lower specification limits were defined at $\pm 5\%$ of the population mean.

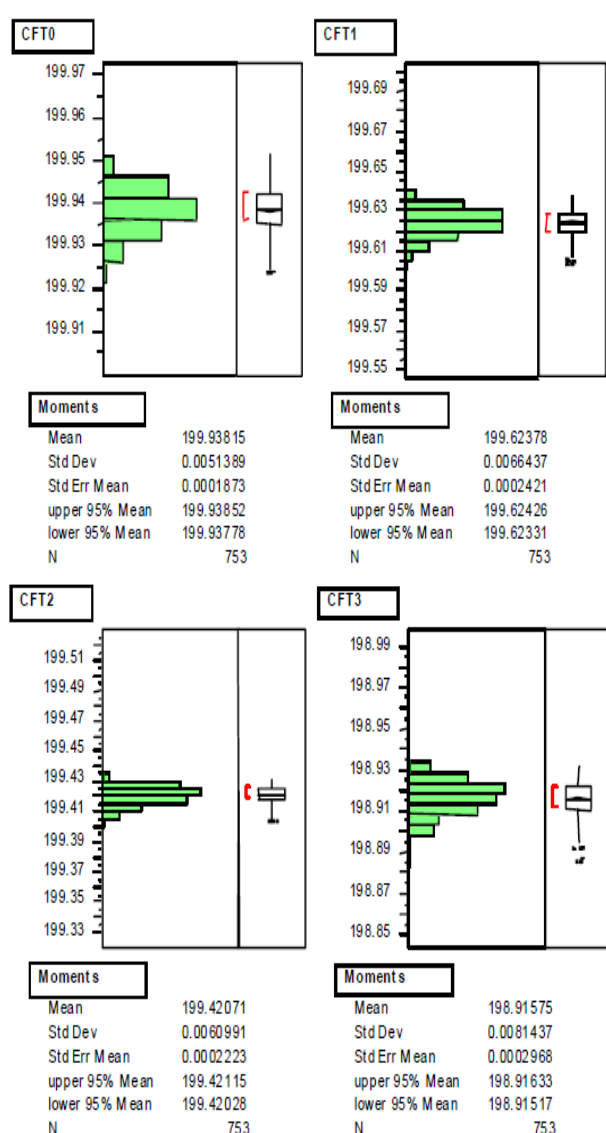


Fig. 6: implimenting the proposed method to a production line in actual manufacturing.

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Due to the exceptional stability of the center frequency standard deviation across the wafer

throughout processing, the resulting frequency distribution histogram remained strictly within the predefined specification limits. This demonstrates that the fabrication method is highly controllable, repeatable, and statistically capable, as the overall frequency spread around the mean is preserved during the trimming process. To evaluate the impact of this sequence on alternative performance metrics, the device bandwidth was subsequently characterized. Finally, Figure 7 provides a comparative analysis between two distinct cohorts of wafers: one processed via the legacy manufacturing workflow and the other via the modified procedure. The figure illustrates both the mean and standard deviation of the total wafer yield for each group. The modified process achieved a mean yield of 97% with a tight variance of $\pm 3\%$. Conversely, the legacy workflow resulted in a lower mean yield of 60%, accompanied by a severe, wide-spectrum variation.

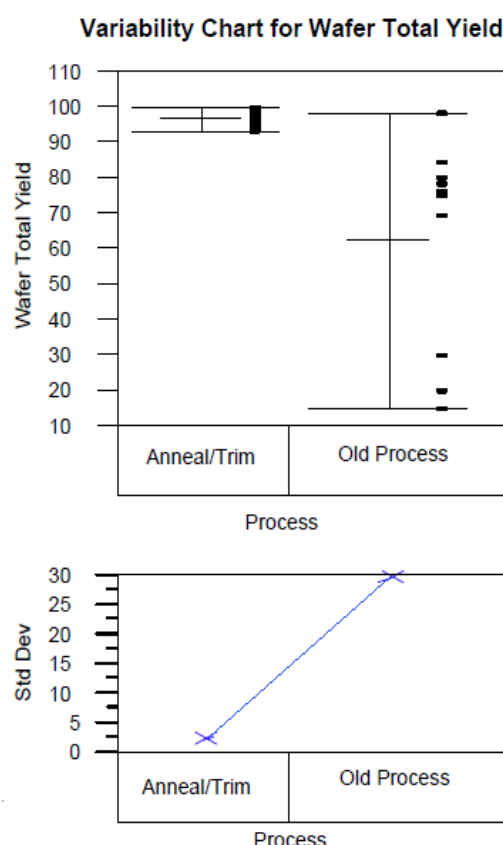


Fig. 7: Comparison between the previous and the proposed process yields.

Source: created by the authors

By implimenting this framework for wafer level processing in the production line, the capital expenditure for specialized equipment was estimated to be reduced from US\$1.6 million –old process- to US\$100,000 for the new technique.

5 Conclusion

A novel statistical framework for wafer-level processing in surface acoustic wave (SAW) device manufacturing has been proposed and experimentally validated. By treating the devices on a wafer as a unified statistical population, this approach replaces the need for individual device testing with holistic process control. To mitigate material instability and secure reproducible device performance, a global wafer annealing step was integrated into the workflow, which induces a systematic upward shift in the center frequency. Subsequent center frequency trimming via etching demonstrated high spatial uniformity and repeatability across the entire wafer, allowing the relationship between etching duration and frequency shift to be mathematically modeled. Utilizing this empirical model, precise trimming durations are calculated to achieve target frequency shifts, allowing the manufacturing sequence to be dynamically optimized. Implementation of this modified framework yielded substantial improvements in both production throughput and manufacturing economics. Specifically, the total device yield rose from a legacy baseline of 60% to 97%, while tuning cycle times were dramatically compressed from 50 hours per wafer to just 4 minutes. Furthermore, the required capital expenditure for specialized equipment was reduced from US\$1.6 million to US\$100,000.

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Declaration of Generative AI and AI-assisted Technologies in the Writing Process

During the preparation of this work, the author(s) utilized artificial intelligence (AI) technologies solely for the purpose of linguistic refinement and grammatical correction. Following the application of these tools, the author(s) comprehensively reviewed, verified, and edited the resulting text. The author(s) maintain full accountability and responsibility for the accuracy, integrity, and final content of the publication.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The author contributed in the present research, at all stages from the formulation of the problem to the final findings and solution.

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Conflict of Interest

The author has no conflicts of interest to declare that are relevant to the content of this article.

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