A Practical Methodology for Designing and Optimizing a Three-Stage Ring Oscillator in 180-nm CMOS Technology using Particle Swarm Optimization (PSO)

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Abstract: - This paper presents the design and optimization of a three-stage ring Oscillator (RO) with enhanced performance in terms of phase noise and power consumption. The proposed design is implemented using TSMC 0.18 µm CMOS technology and operates at a central frequency of 2.93 GHz with a 5 V supply voltage. To address design challenges and achieve optimal performance, Particle Swarm Optimization (PSO) is employed to determine the optimal design parameters, targeting low phase noise, reduced power dissipation, and an improved figure of merit (FOM). The ring oscillator topology is implemented and simulated using the ADS tool. The obtained results demonstrate a phase noise of −117.667 dBc/Hz at 1 MHz offset, with a power consumption of only 7.25 mW, confirming the effectiveness of the proposed approach.

Key-Words: - CMOS Ring oscillator, Phase noise, PSO; Metaheuristic, Optimization, Figure-of-merit (FOM), Power consumption.

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1 Introduction

Analog circuit design is a very difficult task. It is due to the continuous nature of the signals, the unpredictable behavior of components, and the need to balance multiple parameters simultaneously. It's a field where experience, intuition, and an understanding of underlying principles make a huge difference in achieving a successful design, [1]. Metaheuristics are powerful tools in analog integrated circuits (IC) design because they offer flexibility, robustness, and the ability to deal with complex optimization problems. Among the main metaheuristics used were Ant Colony Optimization (ACO) [2], Artificial Bee Colony (ABC) [3], Particle Swarm Optimization (PSO) [4], etc. In integrated circuits, the oscillators are the interface between analog control domains (control voltage, low-frequency noise, bias) and RF or clock domains, making them a core application of analog-intensive IC design.

The oscillators are significant and essential analog circuits in several modern-day wireless communication applications [5] and are widely used in circuits including phase-locked loops (PLLs), clock recovery circuits, and frequency synthesizers, [6]. During the last few years, owing to their excellent phase noise performance, LC oscillators are widely implemented in wireless transceivers. Despite their advantages, LC-based architectures typically experience limitations in tuning range and need considerable silicon area required for the presence of inductors, [7].

Among the commonly used oscillator architectures, the CMOS ring oscillator offers advantages such as a compact area, absence of inductors [8], wider low power consumption, and and the feasibility of integration into standard CMOS processes, [9]. Due to size and cost constraints in modern ICs, ring oscillators are considered a favorable alternative, [10].

The oscillator proposed in this study is a simple inverter-based ring oscillator, often referred to as a single-ended ring oscillator, it a chain consisting of an odd number of inverter stages, each built employs PMOS and NMOS transistors arranged in a loop, where the last stage's output is looped back to the input of the first stage.

The total delay of all stages determines the oscillation period and, consequently, the oscillation frequency, [11].

2 Particle Swarm-Based Optimization

Design Optimization via Particle Swarm Algorithm (PSO) is an advanced optimization approach that enables solving a collection of complex problems in various fields within a reasonable time. This technique emerged in 1995 as a result of the research work [12], and is based on the social behavior of particles, which can be birds or fish [13], to achieve a given objective in a search space where each particle has a certain ability for memory and information processing.

In the PSO algorithm, social behavior is modeled by a mathematical equation that guides the particles during their movement, [14]. Its initialization is based on a randomly generated distribution of particles within a defined search space, where each particle is characterized by its position and velocity, [15].

The evolution of particles is described by mathematical equations. Their position changes iteratively, starting from an initial velocity vector. Each particle identifies its best position and determines whether its current position corresponds to the global optimum or not as shown in Figure 1. Consequently, the particle update process depends on both position and velocity, [16].

The update equations, given by equation (1) and equation (2), define the new position pi(t+1) and the new velocity vi(t+1) of a particle at iteration t, [17]. Pbest and Gbest represent the particle's best individual position and the best global position achieved by the swarm, respectively as shown in Figure 1, [18]. The coefficients c_1 and c_2 reflect the particle's confidence in its own experience and in the swarm's collective knowledge. Finally, r_1 and r_2 are real random numbers generated with a uniform distribution between 0 and 1.

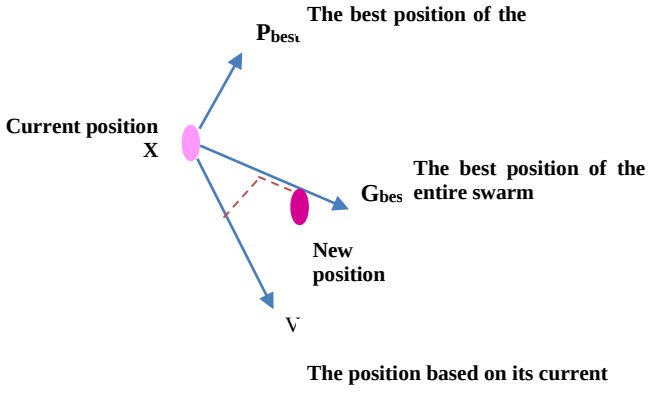

Fig. 1: Displacement of a particle
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$$v_i(t+1) = v_i(t) + c_1 r_1 (p_{best_i}(t) - p(t)) + c_2 r_2 (g_{best}(t) - p(t)) \quad (1)$$

$$p(t+1) = p_i(t) + v_i(t+1) \quad (2)$$

3 CMOS Inverter

A conventional ring oscillator is composed of multiple inverters functioning as delay elements, connected in series to form a closed loop. The output from the final stage is connected back to the input of the first stage, completing the feedback path. Figure 2 illustrates the schematic representation of a single-ended ring oscillator. The Barkhausen conditions for sustained oscillation dictate that the total phase shift be π and that the voltage gain equals unity. Every delay stage provides a phase shift of π/N, where N is the number of delay stages, which implies that the number of stages must be odd, [19], [20].

This configuration is widely used in various communication systems, particularly due to its simplicity and the ability to achieve high-frequency oscillations with low power consumption. Several design optimizations, including power consumption and phase noise, have been proposed for improving ring oscillators in CMOS technology, as outlined in [21], [22].

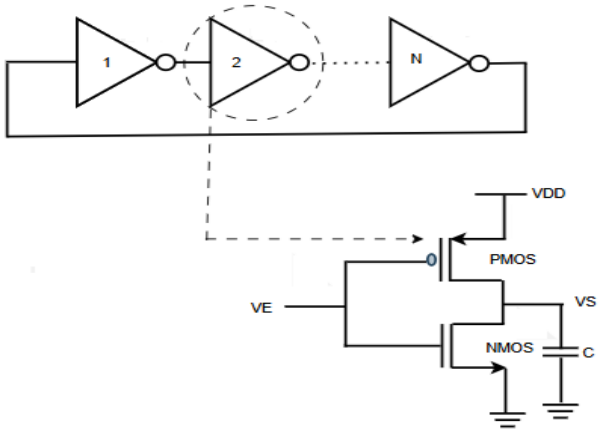

Fig. 2: N stage ring oscillator architecture
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4 Ring Oscillator Description

The ring oscillator comprises an odd number of sequentially connected stages, with the output of the last stage connected to the input of the first stage, forming a feedback loop. These stages are composed of PMOS and NMOS transistors that function as CMOS inverters; in this work, a configuration of three cells is adopted. The gain

stages inside the ring oscillator are connected sequentially to form a closed loop, where the output of the last inverter stage feeds back into the input of the first stage, [19], [21]. In order to attain sustained oscillation, the circuit must satisfy the Barkhausen criteria, which require a total phase shift of 2π and a unity voltage gain. The CMOS inverters provide an inherent DC inversion of π radians, and the remaining phase shift is distributed equally among the N delay stages, [23], [24]. Figure 3 illustrates a typical three-stage ring oscillator architecture.

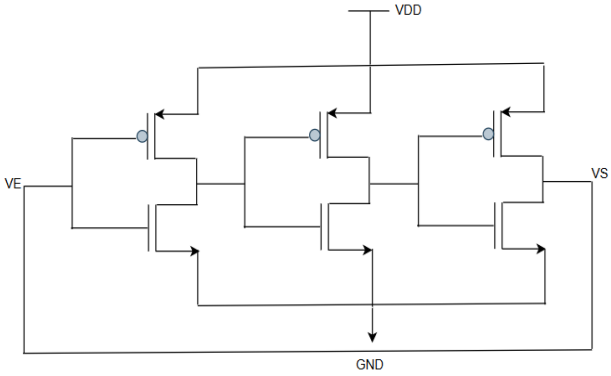

Fig. 3: Single ended Ring Oscillator schematic
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5 Ring Oscillator: Design Parameters and Constraints

In the design of a 3-stage ring Oscillator, six primary parameters are considered: the width and length of NMOS and PMOS transistors (Wn, Ln, Wp, Lp), the supply voltage (V_{DD}), and the load capacitance (Cload). These parameters play a pivotal role in the performance of the circuit and need to be carefully optimized for efficient operation.

5.1 Tank Amplitude Condition

In a 3-stage ring oscillator, the tank amplitude condition ensures that The output voltage variation of each stage is sufficient for oscillation. Since we are not using inductance or resistance, the amplitude is determined by the MOS transistors and the load capacitances. The voltage swing at the output of each stage is related to the current driving the transistor and the load capacitance.

The minimum amplitude V_{min} of the output signal to maintain oscillation can be approximated as follows, as reported in equation (3):

$$V_{min} = \sqrt{I_D . C_{load} . V_{DD}} \tag{3}$$

where:
In this context, I_D is the MOS transistor drain current, C_{load} corresponds to the load capacitance at the output of each stage, and V_{DD} stands for the supply voltage.

5.2 Centre Frequency

The center frequency of a ring Oscillator is dictated by the delay present in each inverter stage as well as the total number of stages in the ring configuration. For a conventional N-stage ring oscillator. As presented in equation (4), the oscillation frequency can be approximated using the following expression:

$$f_{osc} = \frac{1}{N . t_d} = \frac{I_D}{N . \eta . C_{tot} . V_{DD}} \tag{4}$$

Here, I_D corresponds to the drain current of the transistors, N indicates the number of inverter stages, and C_{tot} signifies the total capacitance, as given in Equation (5), it is expressed as:

$$C_{tot} = C_{in} + C_{out} \tag{5}$$

where C_{in} represents the input capacitance of the inverter stage, and C_{out} corresponds to the output capacitance.

In equation (6) the input capacitance C_{in}, primarily determined by the gate oxide capacitances of the PMOS and NMOS transistors, can be expressed as

$$C_{in} = \frac{3}{2} C_{OX} (W_P . L_P + W_n . L_n) \tag{6}$$

From equation (7), the output capacitance C_{out} is given by:

$$C_{out} = C_{OX} (W_P . L_P + W_n . L_n) \tag{7}$$

The total capacitance C_{tot} is defined in equation as:

$$C_{tot} = \frac{5}{2} C_{OX} (W_P . L_P + W_n . L_n) \tag{8}$$

where C_{ox} represents the oxide capacitance, and Lp, Ln correspond to the lengths, while Wp, Wn, correspond to the widths of the PMOS and NMOS devices, respectively.

5.3 Phase Noise

The phase noise parameter [25] is of critical importance, as it can lead to severe issues In a

communications system, particularly in tasks like synchronization errors and intermodulation distortion. For a three-stage ring Oscillator, the primary contributors to phase noise are the transistors and the load capacitances at each stage.

The following equation (9) describes the phase noise within the specified range at a given frequency offset.

$$L\{f_{offset}\} = \frac{8}{3\eta}\frac{kT}{P_{avg}}\frac{V_{DD}}{V_{char}}\frac{f_{osc}^2}{f_{offset}^2} \quad (9)$$

where,

$$V_{char} = \frac{\Delta V}{\gamma} \quad (10)$$

where f_{offset} represents the offset frequency [26] from the carrier at which the phase noise is evaluated, γ is a coefficient that takes a value of 2/3 for long-channel devices operating in saturation, ΔV denotes the gate overdrive voltage, k is the Boltzmann constant, and T corresponds to the absolute temperature.

5.4 Power Consumption

Modern electronic devices are designed to minimize power consumption, making it a crucial factor in circuit design. The power usage of a circuit is directly influenced by the supply voltage, with higher supply voltages leading to increased power consumption. While incorporating a capacitor at each stage of an oscillator introduces additional delay and power consumption, it plays a vital role in reducing phase noise, [27]. The power consumption of a 3-stage ring oscillator is determined using the following equation (11).

$$P = V_{DD}.I_d \quad (11)$$

where,

$$I_d = N.V_{DD}.C_{tot}.f_{osc} \quad (12)$$

6 Ring oscillator: Simulation Results

Table 1 presents the optimization parameters of the PSO algorithm. The process is implemented using MATLAB, while the ADS software is utilized for circuit simulation and performance evaluation. The simulations are conducted based on TSMC CMOS 0.18µm technology, with a supply voltage of 5V, targeting an operating frequency of 2.93 GHz.

Table 1. PSO Parameters

Population size	500
Iteration(max)	1000
Inertia Weight	0.9
Inertia Weight Damping Ratio	0.99
Personal Learning Coefficient	2.0
Global Learning Coefficient	2.0

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Figure 4 shows the periodic output signal of the ring oscillator, demonstrating stable oscillation.

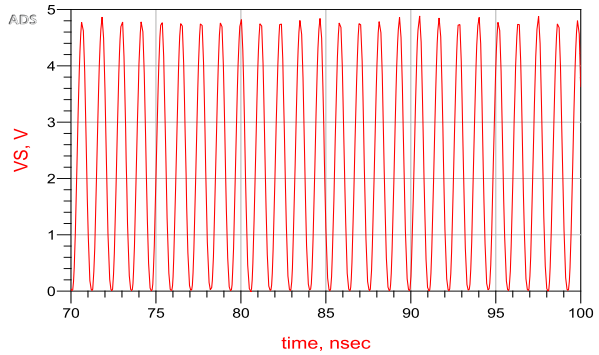

Fig. 4: The proposed three stage ring oscillator output waveform
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The Figure 5 illustrates the output signals of the three stages. Each stage produces an output that is the inverted version of its input.

This chain of successive inversions enables the generation and maintenance of oscillation in the loop.

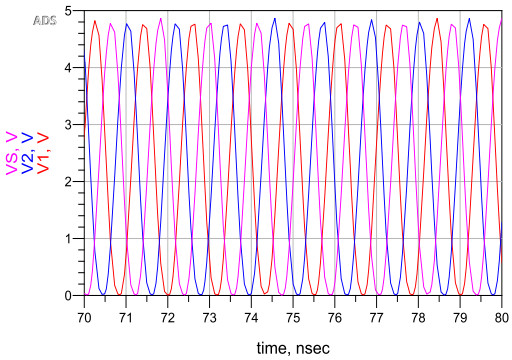

Fig. 5: Output Waveforms of a 3-Stage Ring oscillator Inverter Outputs
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As depicted in Figure 6, the phase noise of the proposed oscillator was simulated using the Pnmx procedure based on the harmonic balance method. The phase noise is observed to be 117.667 dBc/Hz at a 1 MHz offset and -126.629 dBc/Hz at a 2.806 MHz offset.

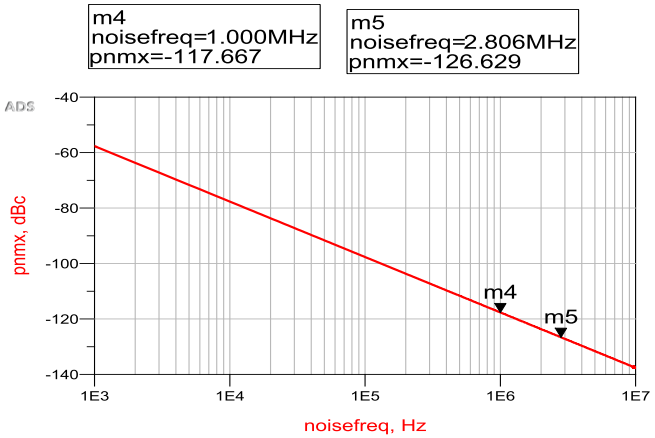

Fig. 6: Phase noise simulation of single ring oscillator
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The circuit generates stable and periodic oscillations, demonstrating consistent frequency behavior over time. This stability is further characterized by the presence of distinct harmonics, indicating the quality and purity of the output signal. These characteristics are clearly illustrated in Figure 7, which shows the harmonic content and confirms the reliable performance of the oscillator.

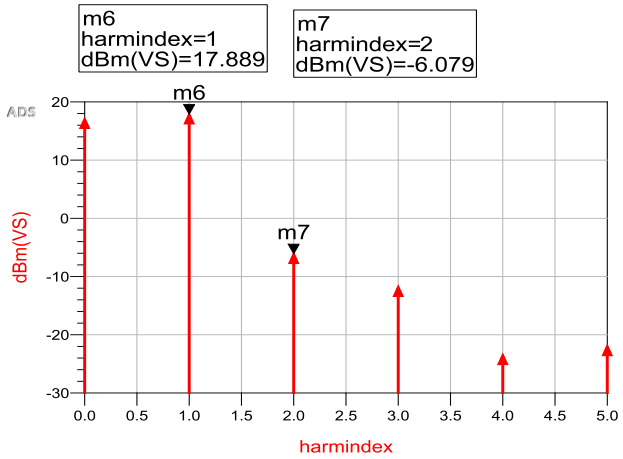

Fig. 7: Single ring oscillator Harmonic index
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The optimal values of the design parameters obtained through the PSO optimization process are summarized in Table 2.

Table 2. Optimal parameters values

NMOS		PMOS		Supply voltage (V)	Load capacity (µF)	L{1MHz} (dBc/Hz)	
Ln (µm)	Wn (µm)	Lp (µm)	Wp (µm)				
0.35	58.86	0.35	63.80	5	0.1	PSO	-112.20

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To compare various oscillators in terms of power consumption, phase noise performance and the carrier frequency, the figure of merit (FOM) is defined in equation (13) as:

$$\mathrm{FOM} = \mathrm{L} - 20\mathrm{Log}\frac{f_{osc}}{f_{offset}} - 10Log\frac{P}{1mW} \qquad (13)$$

The performance of the proposed oscillator is compared with that of previously reported oscillators in Table 3.

Table 3. Comparison between oscillators performances

Ref.	Technology (nm)	Centre Frequency (GHz)	P (mW)	Phase Noise (dBc/Hz	FOM (dBc/Hz)
This work	CMOS 180	2.93	7.32	-117.67@ 1MHz	186.98
[28]	CMOS 180	3.03	15.1	- 97.93 @ 1MHz	170.57
[29]	CMOS 180	1.22	8.5	-108.7 @ 1MHz	161.1
[30]	CMOS 180	1.0	1.2	- 106 @ 1MHz	156.3
[31]	CMOS 180	5.50	5.17	-86 @ 1MHz	153.7

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7 Conclusion

This paper presents the application of Particle Swarm Optimization (PSO) for the efficient design of a three-stage ring Oscillator. By applying PSO, the proposed three-stage ring oscillator has been evaluated and its performance benchmarked against an existing design, demonstrating superior efficiency, regarding optimization of power consumption, phase noise and a figure of merit (FOM). These results were further validated using simulations executed in ADS software. In general, the results underline the capability of PSO as a powerful tool for achieving high-performance three stage ring Oscillator designs.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The research work was mainly carried out by the PhD student authors under the supervision of the professor.

ELHAFIDI SANAE made the primary contribution to this work, including problem formulation, implementation of simulations, data analysis, interpretation of results, and preparation of the initial manuscript.

ELBEQAL ASMAE contributed to literature review, simulations support, and manuscript revision.

MAAROUFI ISMAIL contributed to validation of results and discussions.

Prof. BENHALA BACHIR provided scientific guidance, validated the methodology, and reviewed the manuscript to ensure its academic quality and correctness.

All authors contributed to discussions and approved the final version of the manuscript.

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Conflict of Interest

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