Performance Analysis of Cascaded H-bridge Inverter with SPWM and SVPWM Techniques

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Abstract: - Numerous studies have focused on multilevel inverters and their modulation strategies to minimize output harmonic distortion and enhance overall inverter performance. Among these, Sinusoidal Pulse Width Modulation (SPWM) and Space Vector Pulse Width Modulation (SVPWM) are widely recognized high-frequency modulation techniques capable of producing output voltages with reduced harmonic content. In this work, a comprehensive performance analysis of a Cascaded H-Bridge (CHB) multilevel inverter is carried out using level-shifted Phase Disposition (PD) SPWM and a recent optimized SVPWM method. The evaluation is based on total harmonic distortion (THD), fundamental output voltage magnitude, and DC bus utilization under various load conditions.

Key-Words: - Cascaded H-Bridge (CHB) Inverter; Phase Disposition (PD); Sinusoidal Pulse Width Modulation (SPWM); Space Vector Pulse Width Modulation (SVPWM); Fundamental Component of Output Voltage; DC Bus Utilization.

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1 Introduction

Multi-level inverters are a class of inverters in which multiple dc sources are used for AC wave synthesis. They play a prominent role in many applications because of their better output voltage and power levels. They are used to integrate renewable energy sources. As the number of levels in the output voltage increases, the voltage stress on the devices decreases, and the total harmonic distortion will also be reduced. Depending upon the number of switches and the DC voltage sources, different multilevel topologies have been proposed, [1]. Cascaded H-bridge inverter is one of the popular modules of multi-level inverter and widely used in motor control, reactive power compensation, and harmonic suppression because of its advantages such as modularity, high power capacity, good harmonic characteristics and easily realized redundancy. Depending on the number of voltage levels required, full-bridge inverters will be connected in series to get the desired voltage waveform. To generate 'N' number of output voltage levels (N-1)/2 full bridges are required for a single-phase output, [2]. So, two full bridges are required to generate single phase five level output waveform. Figure 1 shows three phase five level cascaded H-bridge inverter.

Control strategies are presented in section 2; Sinusoidal pulse width modulation is presented in section 3; Optimized Space vector pulse width modulation is presented in section 4; Simulation results and their discussions are presented in section 5, and the conclusion is given in section 6.

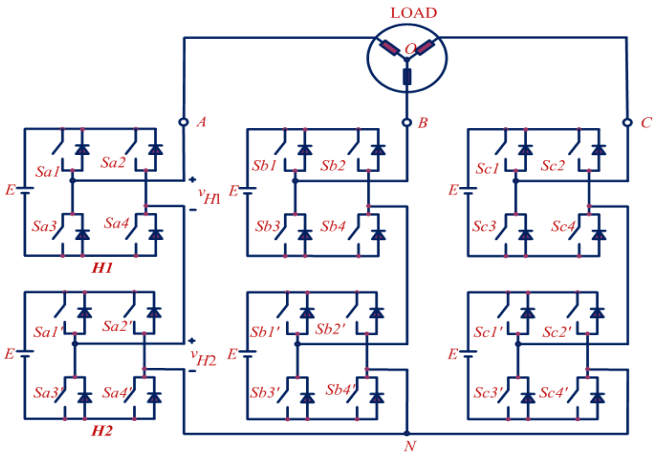

Fig. 1: Three-phase Cascaded H-Bridge Multi-level Inverter
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2 Control Strategies

Based on switching frequency, the modulation methods used in multilevel inverters can be classified into different types as shown in Figure 2. The major

drawback of fundamental switching frequency is the presence of lower-order dominant harmonics in the output voltage, which results in a larger filter size. Consequently, losses will increase, and the efficiency of the inverter will be affected. So, high-frequency modulation techniques are used to increase the order of the dominant frequency, which reduces the size of the filter. The well-known high-frequency modulation techniques are sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM).

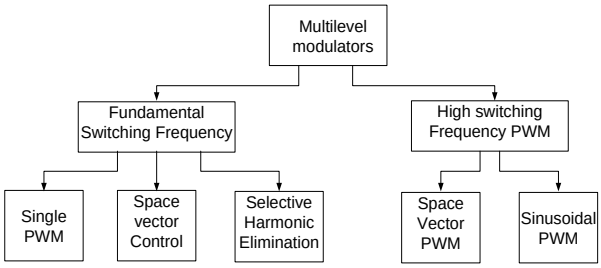

Fig. 2: Different types of multilevel control strategies
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3 Sinusoidal Pulse Width Modulation

In the Sinusoidal pulse width modulation (SPWM) technique, modulating pulses are generated by comparing a sinusoidal reference wave with a triangular carrier wave that has a frequency higher than the reference signal to get a less harmonic output voltage, [2]. The SPWM technique has advantages like low harmonic distortion compared to basic PWM techniques, [3]. SPWM is a widely used technique to generate gating signals, and depending upon the carrier wave position, this is classified into level-shifted SPWM and phase-shifted SPWM, [4]. In level-shifted SPWM, each carrier wave will have a different dc offset level with the same frequency and amplitude. In phase-shifted SPWM, carrier waves are phase-shifted with respect to one another, and they are at the same dc offset level.

In level-shifted carrier-based SPWM, carrier waves are vertically disposed, and the bands they occupy are contiguous, [5]. In this technique, there are three different schemes. They are: (A) phase disposition SPWM (PDSPWM), (B) phase opposition disposition SPWM (PODSPWM), (C) alternative phase opposition and disposition SPWM (APODPWM). In this paper, the PDSPWM technique has been used for generating gating pulses for the switches of the cascaded H-Bridge inverter. For an 'N' level inverter in the PDSPWM technique, the number of carrier waves used is 'N-1', and all carrier waves are compared with a single sinusoidal reference wave, [6]. For a five-level inverter, four level-shifted triangular carrier waves Vtr1, Vtr2, Vtr3, and Vtr4 are compared with a single sinusoidal reference wave as shown in Figure 3 to generate compare values C1, C2, C3, and C4, respectively.

The gating signals required for phase A of the inverter, shown in Figure 1, are given by the equations.

Sa1=C1 Sa2=C2 Sa1'=C3 Sa2'=C4
Sa3=C1' Sa4=C2' Sa3'=C3' Sa4'=C4'

where C1', C2', C3', C4' are complementary to signals C1, C2, C3, C4.

For the remaining two phases B and C, the reference wave is phase shifted by 120° and 240°, respectively, and are compared with the same triangular carriers. These compared values are used to generate gating signals for phase B and phase C in a similar way to phase A.

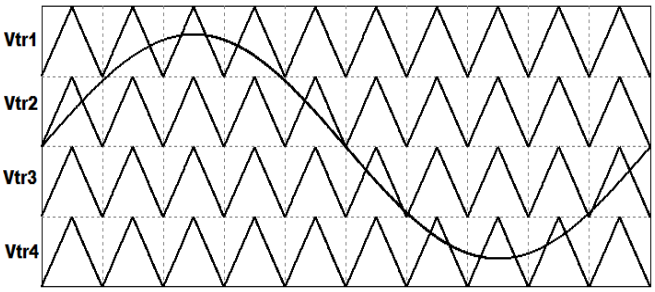

Fig. 3: Phase Disposition Pulse Width Modulation
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4 Spacevector Pulse width Modulation

Space vector PWM is a special switching scheme for the six power semiconductor switches of a three-phase power converter, [7]. Space vector PWM (SVPWM) has become a popular PWM technique for three-phase voltage-source inverters in applications such as control of induction and permanent magnet synchronous motors, [8]. Instead of using a separate modulator for each of the three phases (as in the previous techniques), the complex reference voltage vector is processed as a whole, [7], [9]. The phase voltages corresponding to the eight combinations of switching patterns can be calculated and then converted into the stator two-phase (dq) reference frame. This transformation results in six non-zero voltage vectors and two zero vectors as shown in Figure 4. The six non-zero vectors divide the vector plane into six sectors as shown in Figure 3. In each sector, the reference vector is realized by proper time switching of nearest active and zero vectors by using

dwell times (T1, T2 & T0) calculations, [7], [10]. Vref is the reference vector magnitude, α is the angle or position of the reference vector, and T1, T2 & T0 are the times of application of vector Va, vector Vb, and zero vectors, respectively, [11]. In order to obtain a fixed switching frequency and optimum harmonic performance from SVPWM, each branch should change its state only once in one switching period. This is achieved by applying a zero state vector followed by two adjacent active state vectors in a half-switching period. The second half of the switching period is the mirror image of the first half. The total switching period is thus divided into 7 parts. The zero vector is applied for 1/4th of the total zero vector time first, followed by the application of active vectors for half of their application times, and then again the zero vector is applied for 1/4th of the zero-vector time. This is then repeated in the second half of the switching period. In this way, symmetrical SVPWM is obtained, and for the first sector, the switching sequence is as shown in Figure 5.

In the case of a multi-level inverter, it is more time-consuming to work with the direct multilevel space vector diagrams. For three phase three level inverter, the space vector diagram is reduced to six two-level space vector diagrams, [12]. In the case of five level three phase inverter, five level is getting simplified to six three-level hexagons, and thereafter each three-level hexagon is simplified to six two-level space vector diagrams, [13]. Therefore, there are 36 two-level space vector diagrams, [14].

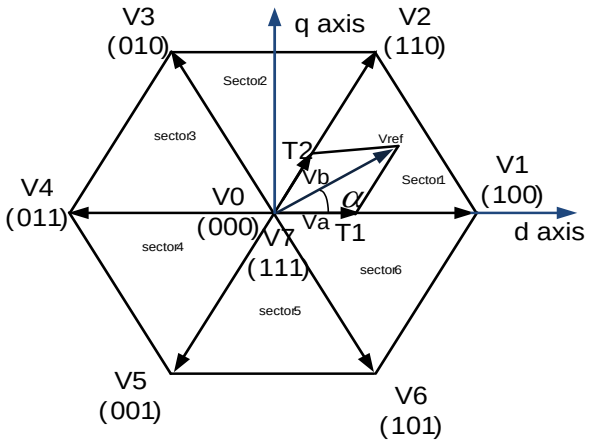

Fig. 4: Two-level space vector diagram
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Five level space vector diagram is shown in Figure 6. Optimized space vector pulse width modulation [15] is a recent technique

In which, depending upon the magnitude of the reference vector, five level space vector diagram is simplified to the inner and outer two-level hexagons [15]. If the magnitude of the reference vector is greater than 2E, then the outer hexagon is selected, and if its magnitude is less than, then the inner hexagon is selected. So, there are a total 6 inner and 18 outer hexagons, and based upon its angular position, a particular inner or outer two-level hexagon is selected [15]. Thereafter, a new reference vector is generated for the selected two-level hexagon. Now, the further process is similar to the conventional two-level space vector method. Therefore, depending upon the selection of inner or outer layer, the total output of the five-level space vector diagram is the sum of eighteen outer space vector diagrams or six inner space vector diagrams.

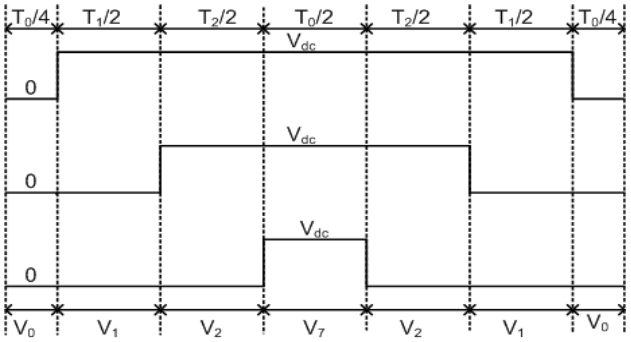

Fig. 5: Switching sequence in first sector
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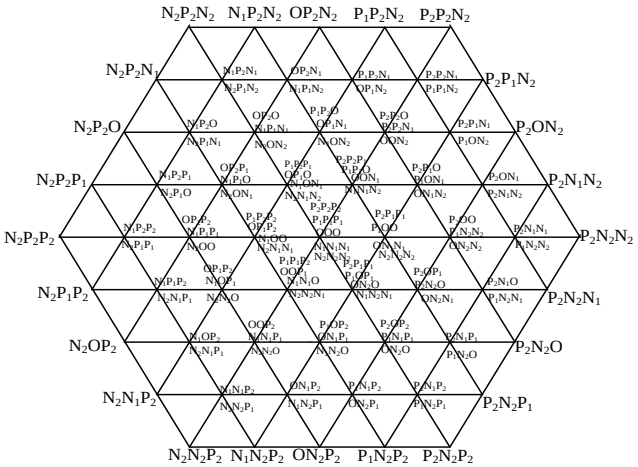

Fig. 6: Space vector diagram for five-level inverters
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5 Simulation Results and Discussions

In this paper, a comparison has been made between Sinusoidal PWM and Space vector PWM techniques with modulation indexes of 0.8 and 0.6 for load conditions of 230V, 5KVA star-connected unity power factor. Sinusoidal PWM and optimized Space vector PWM are simulated in MATLAB. In this study, DC input voltage is taken as E=160V and carrier frequency as 2000 Hz. Corresponding

waveforms and FFT analysis are shown in Figure 7, Figure 8, Figure 9, Figure 10, Figure 11, Figure 12, Figure 13 and Figure 14.

5.1 Simulation Results of Sinusoidal PWM

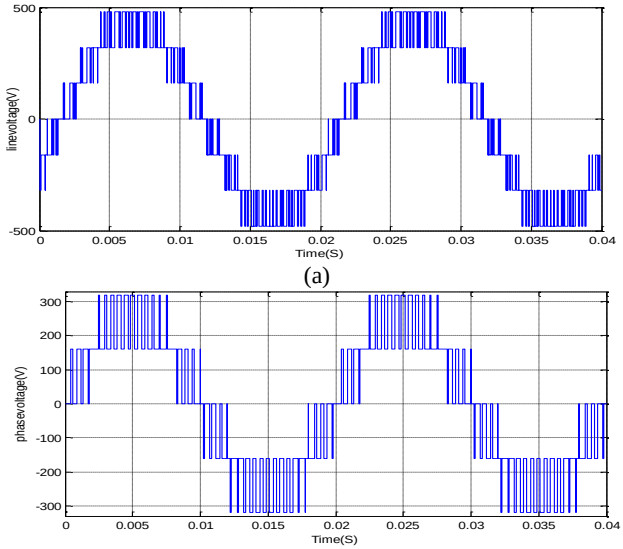

Fig. 7: For ma=0.8 (a) line voltage (b) phase voltage
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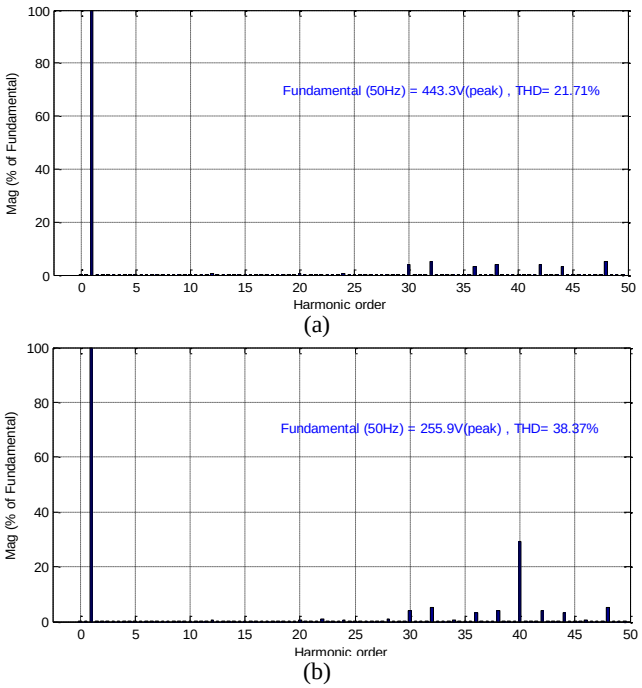

Fig. 8: Harmonic data for ma=0.8 (a) line voltage (b) phase voltage
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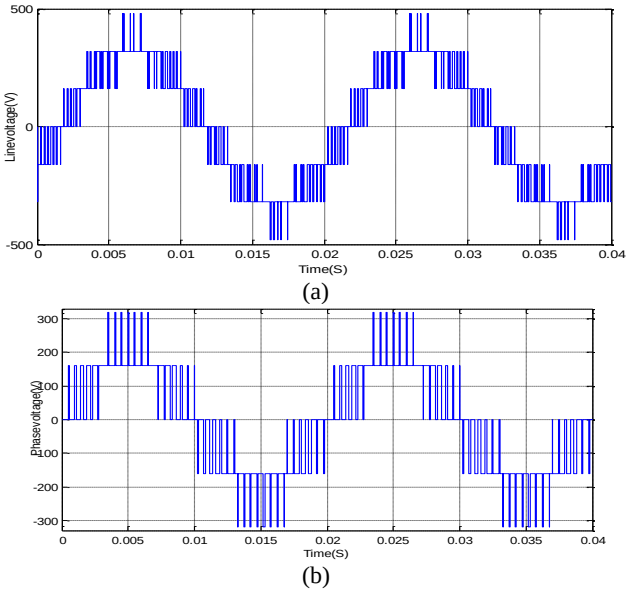

Fig. 9: For ma=0.6 (a) line voltage (b) phase voltage waveforms
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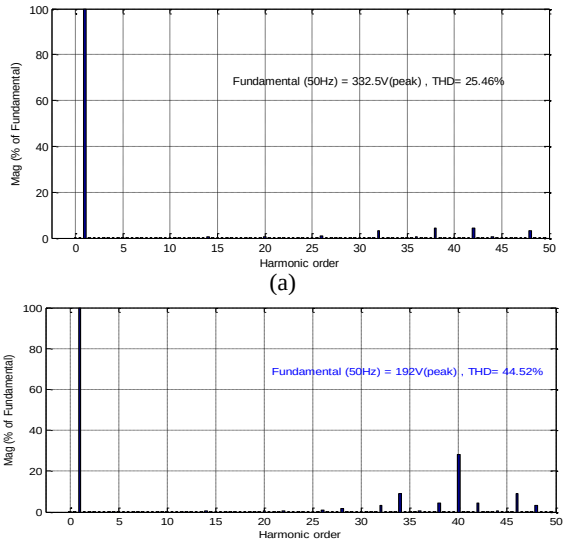

Fig. 10: Harmonic data for ma=0.6 (a) line voltage (b) phase voltage
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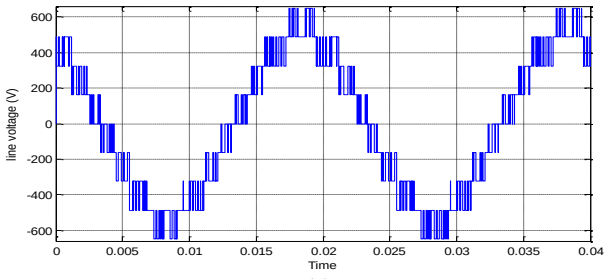
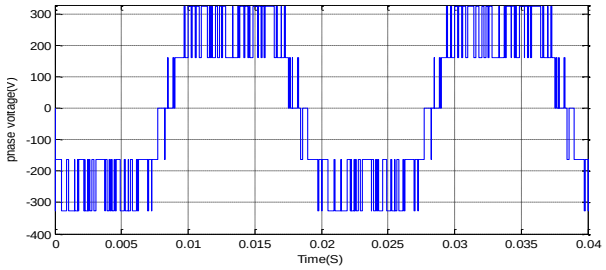
5.2 Simulation Results of Space Vector PWM:





(b)

Fig. 11: For ma=0.8 (a) line voltage (b) phase voltage waveforms

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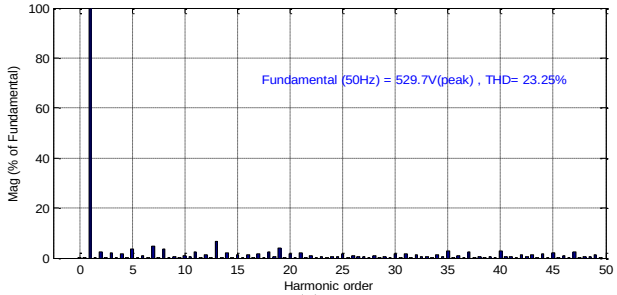
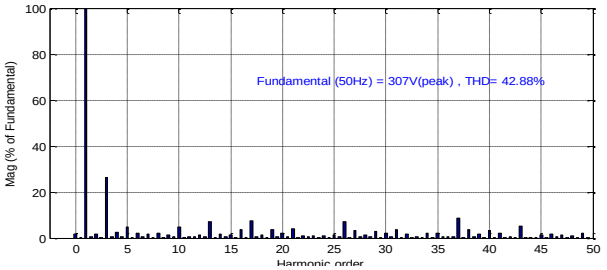


(a)



(b)

Fig. 12: Harmonic data for ma=0.8 (a) line voltage (b) phase voltage

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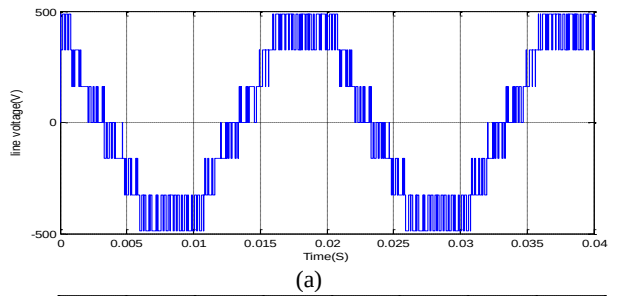
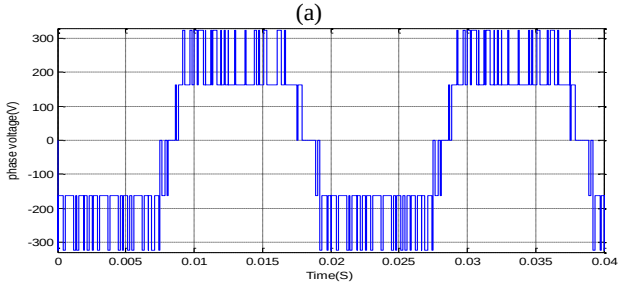


(a)



(b)

Fig. 13: For ma=0.6 (a) line voltage (b) phase voltage waveforms

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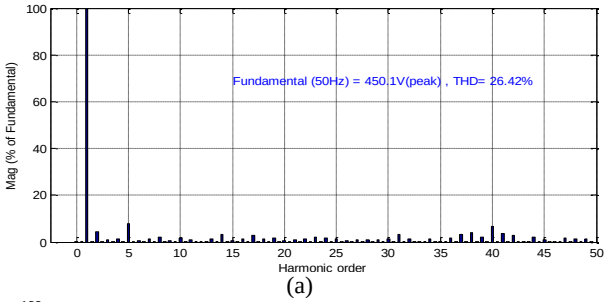
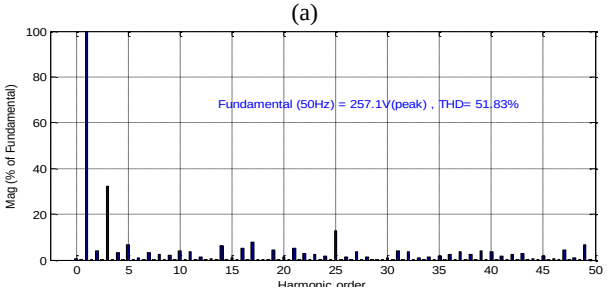


(a)



(b)

Fig. 14: Harmonic data for ma=0.6 (a) line voltage (b) phase voltage

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Table 1. Comparative analysis of SVPWM and SPWM

Parameter	Sinusoidal PWM			Space vector PWM		
	Fundamental (peak)(V)	RMS (V)	THD (%)	Fundamental (peak)(V)	RMS (V)	THD (%)
Line voltage (ma=0.8)	443.3	320.7	21.71	529.7	384.54	23.25
Phase voltage (ma=0.8)	255.9	193.6	38.37	307	236.2	42.88
Line voltage (ma=0.6)	332.5	242.3	25.46	450.1	329.19	26.42
Phase voltage (ma=0.6)	192	148.9	44.52	257.1	204.76	51.83

Source: created by the authors

Even though the harmonic content of optimized SVPWM is a little higher than SPWM, it provides a considerably higher value of the fundamental component of output voltage (Table 1). For the unity modulation index, the DC bus utilization of SVPWM is 15% more than that of SPWM, [2]. The equations (1) and (2) give the DC bus utilization for modulation indexes of 0.8 and 0.6, respectively. So, it can be said that SVPWM has better DC bus utilization than SPWM.

Voltage ratio of SVM and SPWM for modulation index 0.8 is:

$$\frac{V_{ph\max,SVM}}{V_{ph\max,SPWM}} = \frac{384.54 * \sqrt{2}}{320.74 * \sqrt{2}} = 1.19 \quad (1)$$

Voltage ratio of SVM and SPWM for modulation index 0.6 is:

$$\frac{V_{ph\max,SVM}}{V_{ph\max,SPWM}} = \frac{204.76 * \sqrt{2}}{148.6 * \sqrt{2}} = 1.38 \quad (2)$$

6 Conclusion

This paper presents the performance analysis of level-shifted phase-disposition SPWM, and optimized SVPWM for a five-level cascaded H-bridge inverter, and the results are compared at different values of modulation index, [16]. Even though optimized SVPWM has a slightly higher harmonic content, it yields higher values of the fundamental component of output voltage and utilizes the DC bus efficiently. So, it can be concluded that the SVPWM control strategy is preferred where a higher value of the fundamental component of output voltage and effective utilization of the input DC bus are major criteria.

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Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

- Ganugapanta Siddha Reddy carried out the design, simulation and validation of results.
- Venkateswara Reddy Kunduru has developed problem statement and methodology for the implementation.

The authors equally contributed to the present research, at all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

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Conflict of Interest

The authors have no conflicts of interest to declare that are relevant to the content of this article.