Design of Regulated Voltage Supply Circuit for Passive RFID Tag

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Abstract: - This paper presents the design of a regulated voltage supply circuit for a passive UHF RFID tag, which contains a matching network for maximum power delivery, a rectifier, and a voltage regulator. The proposed rectifier overcomes the limitations of conventional rectifiers by achieving both high power conversion efficiency and high output voltage. The circuit achieves 38% power conversion efficiency at 920 MHz, -21 dBm input power, and 1M DC output load. The -21 dBm threshold power improves efficiency and reduces total power consumption, which extends the communication range. The short operating distance of RFID technology has limited its application range in other fields. The theoretical equations and design techniques of the proposed regulated voltage supply circuit are presented and validated with simulation results in a 90 nm CMOS process.

Key-Words: - Passive RFID, Ultra High Frequency (UHF), Rectifier, Regulator, CMOS, Limiter.

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1 Introduction

Wireless object tracking and identification are made possible by the quickly evolving technology known as radio frequency identification (RFID). Today, RFID systems are used in a wide range of applications, including automobile and merchandise theft, collecting tolls continuously, gaining access to buildings, regulating vehicle access to gated communities, corporate campuses, and airports, granting access to ski lifts, tracking library items, asset identification, retailing and supply chain management, and tracking animals, among others, [1].

RFID is a method for storing and retrieving data remotely through the transfer of electromagnetic energy between a radio tag and an RFID transmitter. The radio tag is made up of an antenna and an electronic chip that picks up the radio signal that the RFID reader emits. Both reading and reacting to signals are accomplished by these parts.

There are three types of RFID technology: active, semi-active, and passive tags. But for long-distance identification, which is the subject of this work, the passive UHF RFID tag, which operates at frequencies between 860 MHz and 960 MHz and 2.45 GHz, is more appropriate. Applications like vehicle control access and warehouse surveillance require long-distance identification.

Figure 2 shows a diagram of the passive UHF RFID tag consisting of an antenna and a tag IC. The tag IC consists of two parts: analog and digital. The analog part consists of three parts, including a regulated voltage supply circuit, a demodulator, a modulator, a clock generator, and baseband processor & EEPROM.

The rectifier block is used to convert the received RF electromagnetic wave into a DC signal. To ensure a stable voltage supply for both the digital section and analog front-end, a voltage regulator should be connected at the output of the rectifier to obtain the desired stable power supply, over voltage protection is in the analog section managed by DC limiter.

Additionally, an RFID tag needs enough power to function properly. Therefore, low-power circuit design and increased power transfer efficiency are essential.

The transmission of power for an RFID tag is mainly influenced by the impedance alignment between the antenna and the chip circuits. When these impedances align, the chip can achieve optimal power transfer. Another important factor is the efficiency of the rectifier circuit.

Key characteristics of RFID tags include maximum range and sensitivity to orientation. To obtain the best operating conditions, the antenna impedance must be accurately matched to the chip impedance, which is known to vary with both the received power on the chip and frequency. Calculating an accurate power reflection coefficient for tag antenna design is a challenging task when

both the chip impedance and antenna impedance are complex.

The Friis free-space formula, provided by [2], can be used to determine the long communication range between the tag and reader.

$$r_{\max} = \frac{\lambda}{4\pi}\sqrt{\frac{P_t G_t G_r (1-|S11|^2)}{P_{th}}} \quad (1)$$

where P_t is the RFID reader's power transmission, G_t is the tag antenna's gain, G_r is the reader antenna's gain, $|S11|^2$ is the power transmission coefficient, P_{th} is the tag's threshold power, and λ is the wavelength.

A passive RFID tag's transmission range is determined by its input power. In addition, the tag's overall power consumption and power conversion efficiency nearly totally control the input power. Therefore, increasing power conversion efficiency and reducing overall power usage are effective strategies to increase communication range.

The power conversion efficiency (PCE) is defined as the ratio of the output DC power to the input RF power, as follows:

$$PCE = \frac{P_{DC}}{P_{RF}} \times 100\% \quad (2)$$

One of the main obstacles to the development and application of passive RFID tags is the performance of the regulated voltage supply circuit, which is composed of the following parts: matching, rectifier, and regulator.

Power efficiency and output supply voltage stabilization are the main indicators of its performance. Addressing these challenges is the focus of this paper.

In this work, we provide a novel approach to UHF passive RFID tag power management.

The block diagram of our designed circuit, which is made up of four sub-circuits, the antenna, the rectifier, the regulator circuit, and the impedance matching circuit is shown in Figure 3. An antenna model serves as the RF power source in this work.

So, for a low distance of communication, the available voltage at the input terminal of the RFID antenna is extremely small and falls in the range of less than 300 mV.

Different RFID communication bandwidths are available, including 125-134 Khz, 13.56 MHz, 920 MHz, 2.45 GHz, and 5.7 GHz microwave bands. This research is based on the maximum effective isotropic radiated power (EIRP=4W) defined by the FCC in the 902-928 MHz bandwidth, [3].

The structure of this work is as follows: the theoretical background of impedance matching is presented in section 2. Sections 3, 4, and 5 introduce the rectifier, DC limiter, and regulator, respectively. Section 7 displays the simulation results of the suggested regulated voltage supply circuit for a passive UHF RFID tag, and Section 8 presents the conclusion of this work.

2 Architecture

The matching circuit will be covered in this section. To ensure a maximum transfer of radiofrequency energy from the source to the load, an impedance matching is required. A rectifier's input impedance is usually substantially greater than its source impedance. However, an RFID system's typical RF source impedance is 50Ω.

To achieve impedance matching inside the system, the antenna's output impedance is adjusted to allow for maximum power transmission to the tag chip.

The equivalent model of the matching network is shown in Figure 1.

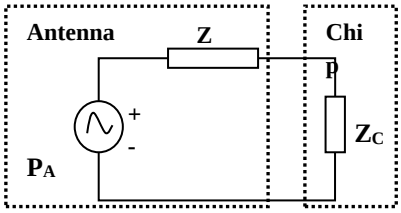

Fig. 1: Model of the matching network

The expressions $Z_A = R_A + j X_A$, $Z_C = R_C + j X_C$. P_A represents the output impedance of the antenna Z_A and the input impedance of the chip Z_C.The power received by the antenna is represented by the P_A.

The power that the chip receives is determined by impedance matching:

$$P_C = P_A \gamma \quad (3)$$

In (3), P_C represents the energy that the chip receives, P_A represents the energy that the antenna receives, and γ represents the power transmission coefficient, which is established by (4).

$$\gamma = \frac{4R_C R_A}{|Z_C + Z_A|^2} \quad (4)$$

Consequently, when $Z_C = Z_A^*$ the maximum power transmission coefficient obtains.

However, the complex impedance of $Z_C$and Z_A both changes with carrier frequency and the power tag receives. Optimization target is to have Z_C=Z_A* when the energy sensitivity of the tag is equal to the input power.

As shown in Figure.10, the S11 at the antenna in this work is around -29.68dB at 920 MHz, demonstrating an appropriate match.

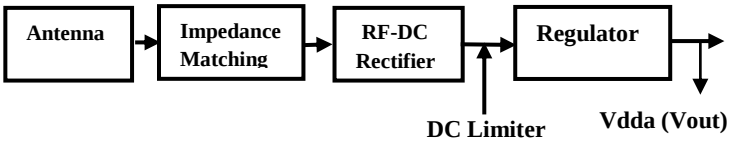

Fig. 2: Diagram of a passive tag

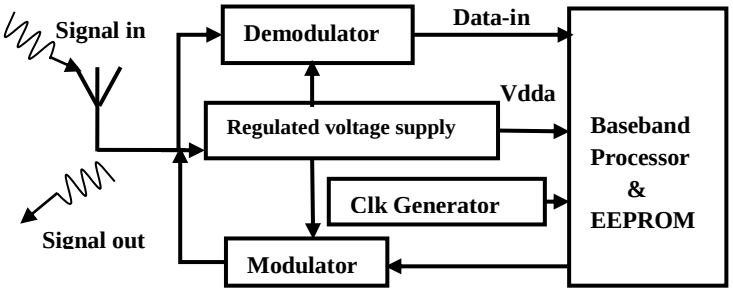

Fig.3: Diagram of the proposed regulated voltage supply circuit

3 RF-DC Rectifier

The rectifier circuit is a key component of passive RFID tags. Its power conversion efficiency (PCE) significantly increases the communication range. Longer communication lengths are possible with a high PCE. Due to system limitations, only two types of rectifier structures are feasible for UHF RFID transponders, even though there are many different varieties available, [2], [4], [5].

Among these is the gate cross-connected bridge rectifier, which eliminates the need for diode MOS transistors and regular diodes. High PCE is possible because this structure is not subject to threshold voltage penalties. It is not appropriate for applications needing a high voltage supply, nevertheless, because of their limited capacity to produce high voltage.

The other type is the Dickson charge pump rectifier, which converts incident signal power into a power supply.

A low percentage of PCE could be the result of the MOS transistor's threshold voltage. Low-threshold voltage drop Schottky diodes are available, but their implementation is costly due to the additional mask layers and processing processes needed.

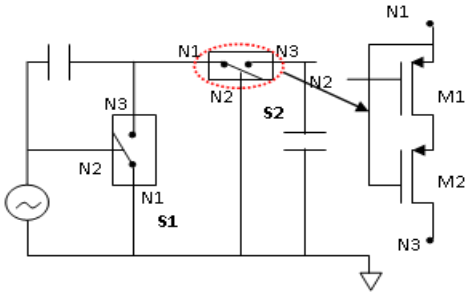

Fig. 4(a): 1 stage of proposed rectifier

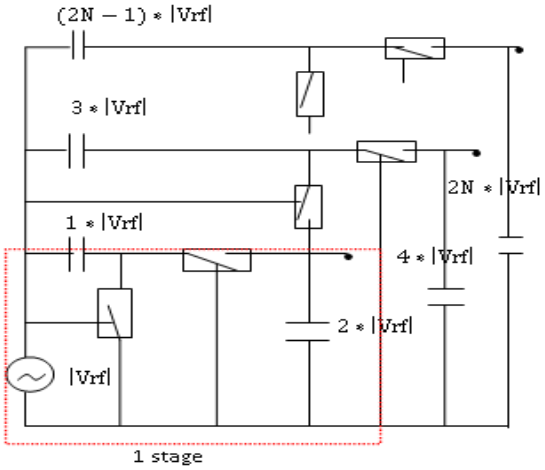

Fig. 4(b): N stage of proposed rectifier structure

The proposed circuit is shown in Figure 4(a). As seen on the right, sub-circuits S1 and S2 are made up of two PMOS transistors, respectively. Since MOS transistors M1 and M2 in Figure 4(a) are not diode-connected, the forward voltage loss can be reduced almost as much as in a cross-connected gate, [5]. M2 is added to the cross-connected circuit gate to reduce the potential reverse current drawbacks.

This M2 is used to limit the reverse current flowing from Node N3 to Node N1. Furthermore, since there is very little current in the current scenario, lowering the voltage drop on by channel resistance is less crucial. Instead, we give priority to lowering the parasitic capacitor, which could cause power loss when charging and discharging.

We can employ many stages to get the desired output voltage level by stacking the single stage as shown in Figure 4(b). The PCE is impacted by the stage number in addition to the output voltage. Because there is no threshold voltage penalty, the degradation of PCE can be tolerated even though the rectifier's PCE may decrease as the stage number rises.

When the forward current is low, channel resistance over sub-circuits S1 and S2 causes a

slight drop in voltage. Because of this, our voltage amplifier is more suitable for ultra-low-power passive UHF RFID applications. Figure 5 shows the simulation results for the proposed rectifier.

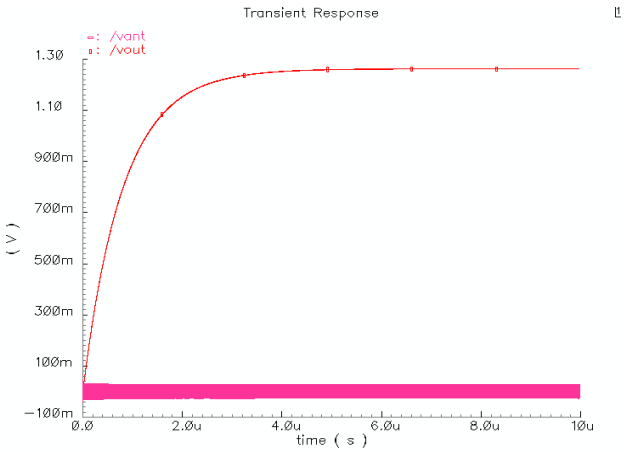

Fig. 5: Simulation results for the proposed rectifier's input/output

4 Voltage Limiter

In this section, we present the necessity of using a DC limiter circuit at the rectifier's output. Due to the wide variations in the working distance of passive UHF RFID tags, the dynamic range of the RF input power can reach up to 30 dB at short distances, which may affect the functionality of the voltage regulator circuit.

The voltage limiter is required to control the voltage amplitude while the rectifier is in the near field to safeguard the RFID tag circuits and ensure normal operation.

Figure 6 depicts the suggested voltage limiter for this system. It is composed of a current leak-off circuit and a voltage-dividing circuit.

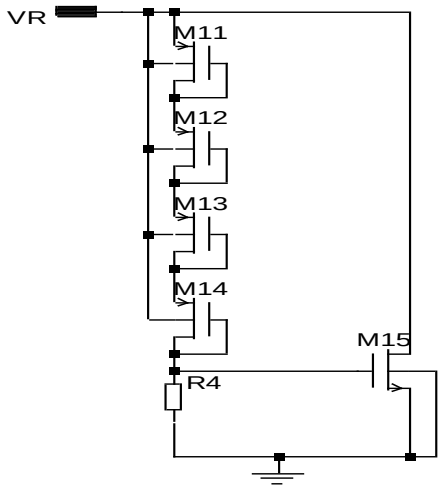

Fig. 6: DC limiter

Four PMOS transistors coupled by cascade diodes and a resistor make up the voltage-dividing circuit. When the rectifier's output voltage exceeds 1.8V.

When the leak-off transistor is activated, the deposit capacitor discharges, which results in a reduction of the rectifier's output voltage. The I-V characteristics of the voltage limiter are shown in Figure 7. The voltage limiter remains off until the rectifier's output voltage exceeds 1.8V.

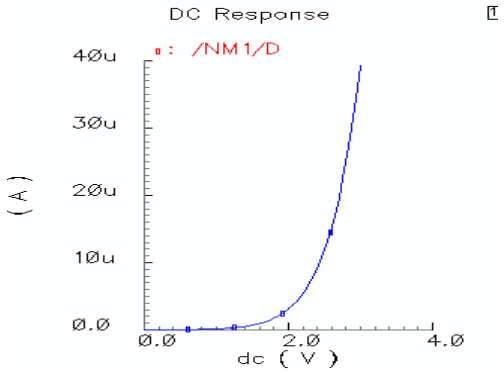

Fig. 7: I-V character of voltage limiter

5 Voltage Regulator

The main challenge in designing UHF RFID LDO voltage regulators lies in ensuring stability despite variations in load current. Unlike conventional voltage regulators, RFID voltage regulators typically use much smaller load capacitors, which shift the dominant pole of the system to a much lower frequency compared to the first non-dominant pole, [6].

In RFID applications, LDO regulators require capacitors in the range of tens of picofarads to maintain stability. However, their use is constrained by the area occupied by the load capacitor at the rectifier output, [7]. Figure 9 illustrates the topology of the LDO regulator designed for a proposed power management circuit for a passive UHF RFID tag.

The regulator comprises an error amplifier (EA), a resistive feedback network, and a PMOS transistor serving as the pass device between the input voltage V_R and the regulated output voltage V_{out}, which powers the load, modeled as $R_L \| C_L$, [8], [9].

The R_{f0}–R_{f1} feedback resistors monitor changes in V_{out} caused by fluctuations in the input voltage and/or load current. The pass transistor gate is continually driven by the amplified difference between this sampling value V_{fb} and a reference voltage V_{ref}, ensuring that the output voltage stays constant in line with the stated relationship.

$$V_{out} = (1 + \frac{R_{f0}}{R_{f1}})V_{ref} \quad (5)$$

The regulator achieves a gain of 80 dB and a phase margin of 89°, demonstrating its stability.

6 Voltage Reference

In UHF RFID tag chips, the voltage reference must consume minimal power and occupy a small chip area. However, the limited chip area of passive tags and the large layout size of BJTs in conventional voltage references [10] make BJTs unsuitable for generating a PTAT current. To address this limitation, MOSFETs operating in the sub-threshold region were used to generate the PTAT current, leading to the development of a new voltage reference design, as shown in Figure 8. In this design, transistors M6 and M7 operate in the sub-threshold region.

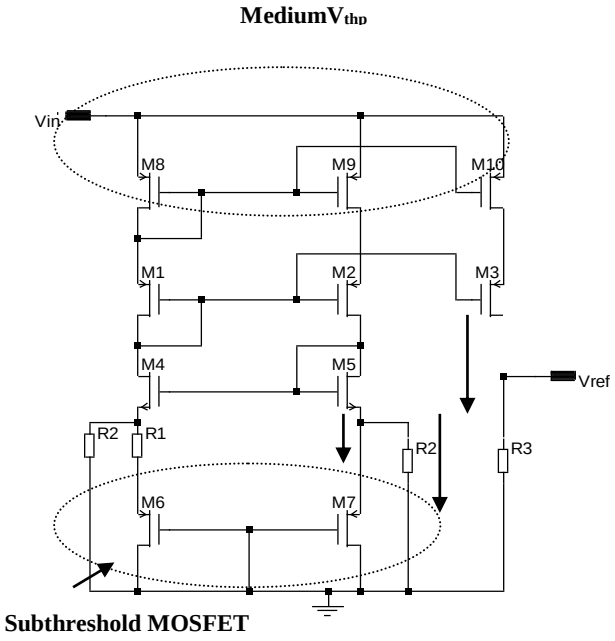

Fig. 8: Bandgap voltage reference

The resistor R3 takes the current, I3, which is the sum of I1 and I2, and generates an output oltage that can be expressed as:

$$V_{ref} = R_3(I_1 + I_2) \quad (6)$$

$$V_{ref} = \frac{R_3}{R_2}(R_2 I_1 + R_1 I_1 + V_{gs6}) \quad (7)$$

$$I_1 = \frac{nV_T\, ln(k)}{R1}, \quad k = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_7} \quad (8)$$

$$V_{ref} = \frac{R_3}{R_2} * \left[V_{gs6} + nV_T\, ln\left(\frac{\left(\frac{w}{L}\right)_6}{\left(\frac{W}{L}\right)_7}\right) * \frac{R_2}{R_1}\right] \quad (9)$$

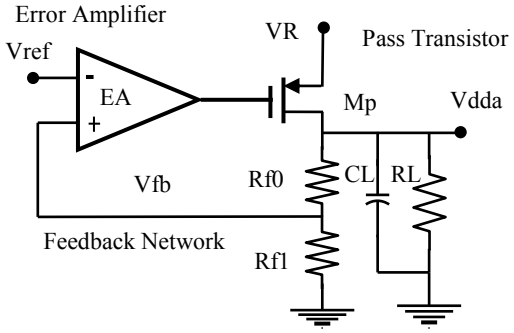

Fig. 9: Voltage regulator

Table 1. Simulations results of the proposed LDO

Specifications	Simulations results
Technology	90 nm
Input voltage (V)	Vin:0.9~1.2 VR:0.9~1.2
Output voltage (V)	Vref:0.504 Vreg:1.01
Line regulation (mV/V)	Vref:0.9 Vreg:5.9
Load capability (uA)	50
Load regulation (mV/uA)	1.5
Temperature range (°C)	-30~50
Temperature coefficient(ppm/°C)	Vref:12 Vreg:31.3075
Quiescent current (nA)	390

7 Simulation Results

The simulation results of the proposed regulated voltage supply circuit for a passive RFID tag are displayed in Figure 11. Practical design indicates that the output must approach 1V with a 50Ω antenna, a 920 MHz frequency, a 1MΩ load, and an input power of -21 dBm. Table 1 presents the summary results of the proposed LDO regulator used in this work.

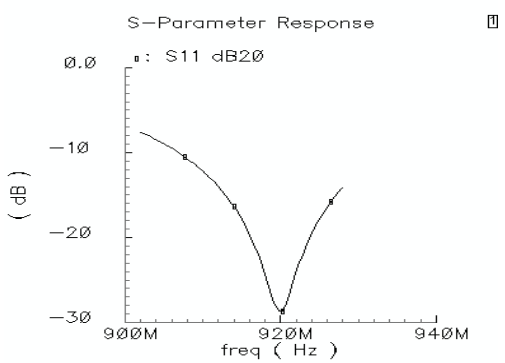

Fig. 10: S11 reflection coefficient

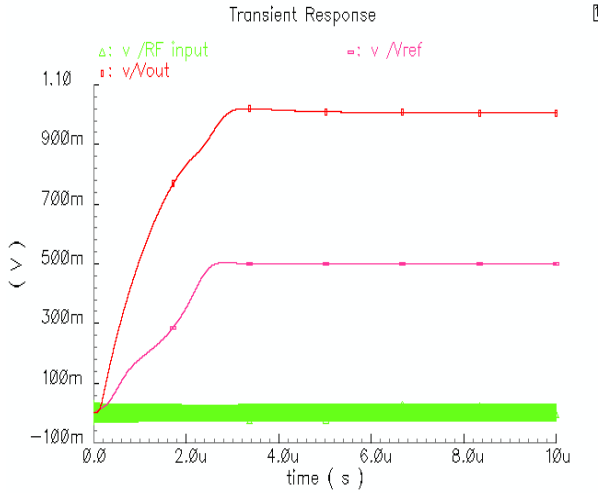

Fig. 11: The proposed regulated voltage supply circuit's simulation results

8 Conclusion

This paper covers a regulated voltage supply circuit that consists of a regulator, DC limiter, and rectifier and is designed for a passive UHF RFID tag. To optimize the design, the study combines both theoretical analysis and circuit simulations.

Simulation results show that the system can drive a 1MΩ equivalent load at 1V with an input power of -21 dBm. These findings improve performance and extend the communication range for relevant applications.

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