Reduced Loss Tristate SEPIC

FELIX A. HIMMELSTOSS
Faculty of Electronic Engineering and Entrepreneurship,
University of Applied Sciences Technikum Wien,
Hoechstaedtplatz 6, 1200 Vienna,
AUSTRIA

Abstract: - The Sepic is a very well-known DC/DC converter topology. A tristate converter extends the circuit by an additional electronic switch and a diode. Three modes follow each other within one switching period. During the first mode M1, both transistors are on and both diodes are off. In the second mode M2 only the second switch is on and the first diode is conducting, and in mode M3 only the second diode is conducting. The voltage transformation ratio is a function of the duty cycles of the two electronic switches. In a typical tristate converter, the current flows through the second switch during the first two modes. In the converter treated here, the current is flowing through the second switch only during the second mode, so the losses are reduced compared to the normal tristate converter. The function of the converter is described in the steady state by the voltages across and the currents through the components. The large and the small signal models are derived. When the duty cycle of the second switch is held constant and the duty cycle of the first switch is used as a variable, the voltage transformation ratio is linearized, and additionally, the converter operates as a phase minimum system. The calculation of the transfer functions is explained and further possible modifications are shown. The start-up and the reaction of a short-circuit are investigated. The considerations are proved by simulations with the help of LTSpice.

Key-Words: - Tristate, SEPIC, reduced losses, large signal model, small signal model, linearization, simulations

Received: May 26, 2024. Revised: November 14, 2024. Accepted: December 11, 2024. Published: February 18, 2025.

1 Introduction

The SEPIC (an abbreviation for single-ended primary inductor converter) is a very well-known converter topology treated in all the textbooks on Power Electronics, e.g., [1], [2], [3]. Looking at the IEEE Explore databank one finds 1650 items (2024/08/26), but directly no item about a tristate SEPIC. The tristate concept is shown in [4] with a comprehensive list of literature concerning this topic. Therefore, only the paper [5] with the basic idea for the Boost converter is mentioned here. The electronic switch of the Boost converter is replaced by a series connection of two electronic switches and a diode, where the cathode is connected to the connection point of the two electronic switches. Figure 1 shows the basic SEPIC converter and Figure 2 shows the application of the tristate concept. In the continuous operation, the converter has three modes. In the first mode M1 both electronic switches S1, and S2 are on and both diodes D1 and D2 are off. In the second mode, M2 the first switch S1 is off and the diode D1 is on, S2 is still on, and in the third mode M3 also the second switch S2 is turned off and only the second diode D2 is conducting.

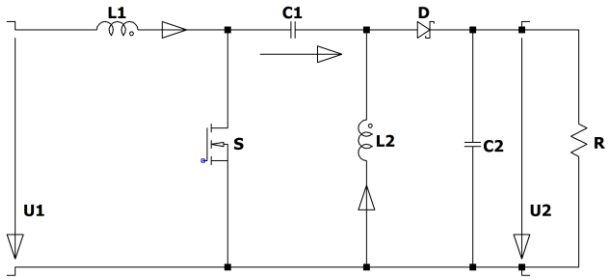

Fig. 1: Original SEPIC

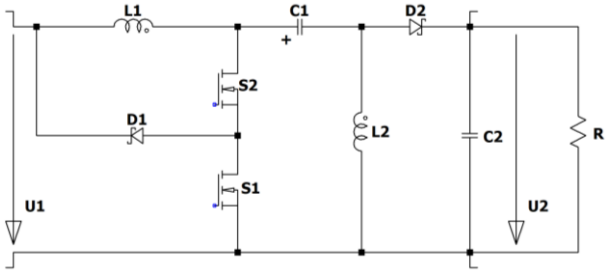

Fig. 2: Tristate SEPIC

In this basic tristate concept, the second switch S2 is on during the first and the second mode, and the sum of both currents through the coils L1, L2 is flowing through it and produces losses. Another disadvantage of the circuit according to Figure 2 is

that during M2 the current through L2 is flowing back into the source. So a part of the energy that was taken out of the source during mode M1 and M3 is fed back during M2. This can be interpreted analogously to a reactive power in a sinusoidal net which produces additional losses. Figure 3 shows the input current, the current through L2, the input voltage, the output voltage, the control signal of S2, and the control signal of S1. It can be seen that during M2 current flows back to the source.

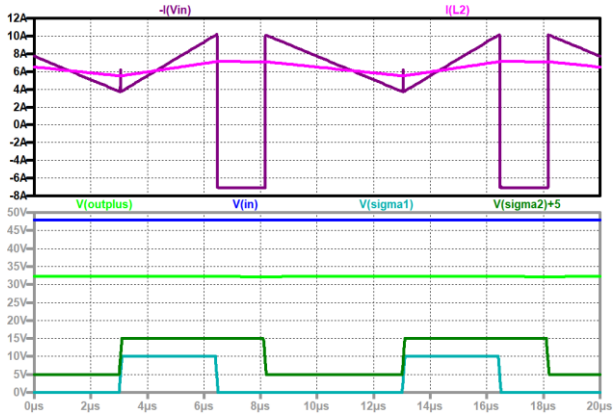

Fig. 3: Tristate SEPIC (L1=25 µH, L2=100 µH), up to down: input current (dark violet), current through L2 (violet); input voltage (blue), output voltage (green), control signal of S2 (dark green), control signal of S1 (turquoise)

In the here presented tristate converter (Figure 4) S2 is also turned on during M1 and M2, but only during M2 the currents through the inductors are flowing through it. Furthermore, the input current is continuous and no energy is oscillating at the input.

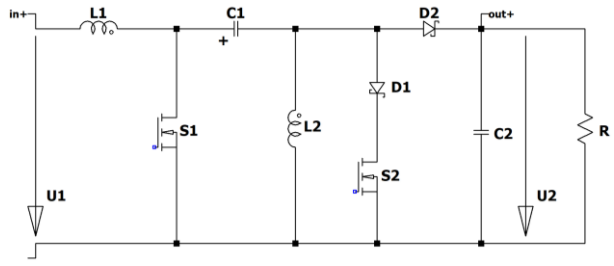

Fig. 4: Reduced loss tristate SEPIC

2 The Converter in the Steady-State

To better understand the converter one should study the voltages across and the current through the components. This can be done with a scattered paper and a pencil. Here we show the considerations and the results by a simulation.

Starting with the control signals and a duty cycle d1 of the first switch of 0.5 and a duty cycle d2 of the second switch of 0.75 one gets Figure 5.

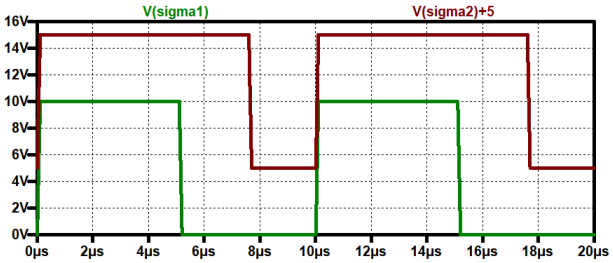

Fig. 5: Control signals of the first switch (green) and of the second switch (black, shifted)

The voltage across the first coil L1 has to be considered. During the on-time of the first switch S1, the input voltage U1 is across the inductor, in mode M2, when only the second switch S2 is conducting, the voltage is zero, and in the last mode M3 the voltage across the coil is the input voltage U1 minus the output voltage U2 minus the voltage across C1 UC1. Therefore, the voltage-time balance is given by:

$$U_1 d_1 = \left|(U_1 - U_2 - U_{C1})\right|(1-d_2)\,. \qquad (1)$$

Inspecting the loop U1, L1, C1, and L2 one can immediately see that in the steady-state the voltage across C1 must be equal to the input voltage:

$$U_{C1} = U_1\,. \qquad (2)$$

The voltage transformation ratio of the converter is therefore:

$$M = \frac{U_2}{U_1} = \frac{d_1}{1-d_2}\,. \qquad d_2 \geq d_1 \qquad (3)$$

The signal sequence of the voltage across L1 is shown in Figure 6.

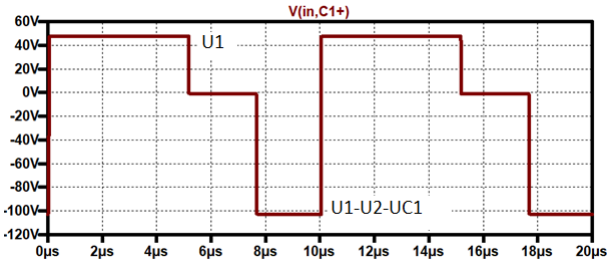

Fig. 6: Voltage across the first coil L1

Looking at the second coil L2 one sees that during M1 the voltage across C1 (which is equal to the input voltage) is across L2, during M2 the coil is short-circuited, and during M3 the negative output voltage is across L2. The voltage across L2 must

have the same shape as the voltage across L1 (Figure 7).

Now we consider the voltages across the semiconductors. For the first electronic switch one gets for the first mode M1 zero (the switch is turned on), during M2 the voltage across C1, and for M3 the sum of the voltages across both capacitors (Figure 8).

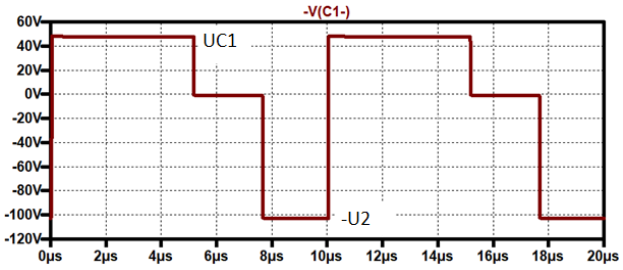

Fig. 7: Voltage across the second coil L2

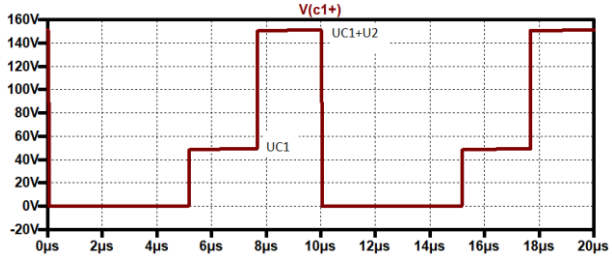

Fig. 8: Voltage across the first electronic switch S1

During the first two modes, the switch S2 is on and has to block the output voltage during M3. The signal is shown in Figure 9.

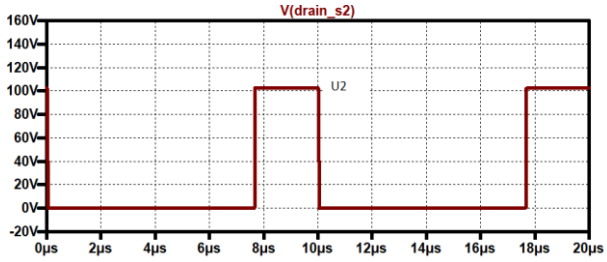

Fig. 9: Voltage across the second electronic switch S2

During mode M1 the first diode D1 has to block the voltage across C1. During M2 the voltage must be zero (a little bit positive due to the forward voltage of the diode) and during M3 the diode is not conducting but the voltage is still zero. The transistor S2 blocks the output voltage and the diode D1 is still forward biased (Figure 10).

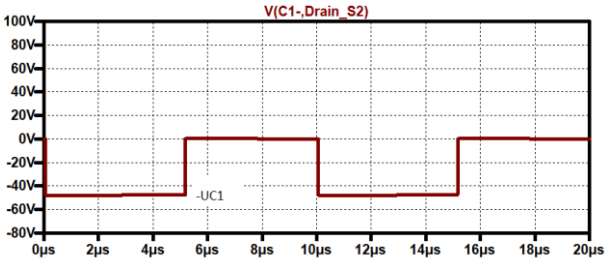

Fig. 10: Voltage across the first diode D1

During M1 the output diode D2 has to block the negative sum of the two voltages across the two capacitors. During M2 only the negative output voltage is across D2, and during M3 it is conducting and the voltage is zero (Figure 11).

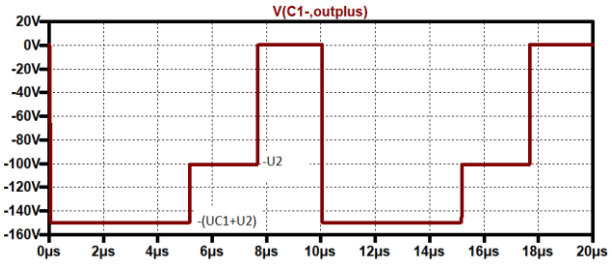

Fig. 11: Voltage across the second diode D2

The current through both coils increases during mode M1, stays constant during M2 and decreases by the same value during M3. The signal form is shown in Figure 12 for L1.

The change of the current through L1 (and L2 when both inductors have the same value because C1 is also charged to U1 in the steady state) is given by:

$$\Delta I_L = \frac{U_1 d_1 T}{L} = \frac{U_1 d_1}{Lf} \tag{4}$$

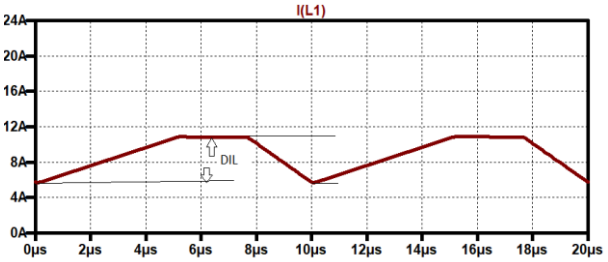

Fig. 12: Current through the first coil

The current through L2 must have the same form (because the voltages are equal across both coils) (Figure 13) as the current through L1. The starting point, however, differs.

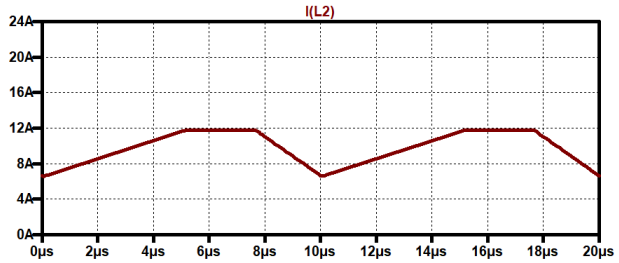

Fig. 13: Current through the second coil

During M1 the current through the first electronic switch is equal to the sum of both inductor currents (Figure 14). The spikes at the beginning of the modes M1 and M3 are caused by the turn-off of the diodes D2 at the beginning of M1 and D1 at the end of M2.

During M2 the current through S2 is equal to the current through D1 and both currents through the inductors are flowing through D1 and S2 (Figure 15). The spike is caused by the turn-off of D2 and the charging of the parasitic capacitors. The current is constant because both coils are short-circuited and the current through them stays constant.

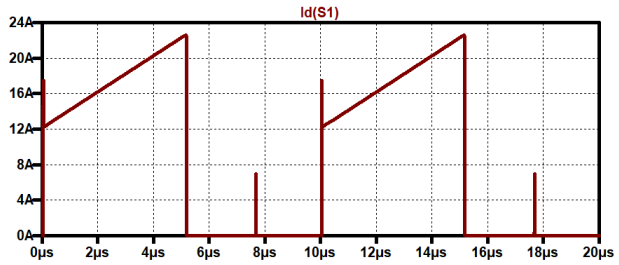

Fig. 14: Current through the first electronic switch

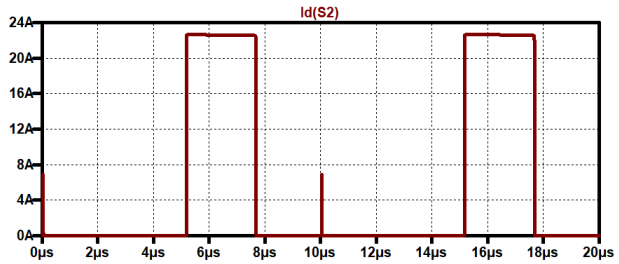

Fig. 15: Current through the second electronic switch S2 and the first diode D1

Figure 16 shows the current through D2. During mode M3 the current through the coils is flowing through this diode. The mean value of the current must be equal to the load current, because all charge transported through the diode D2 is used by the load, and no charge is necessary for the output capacitor in the mean.

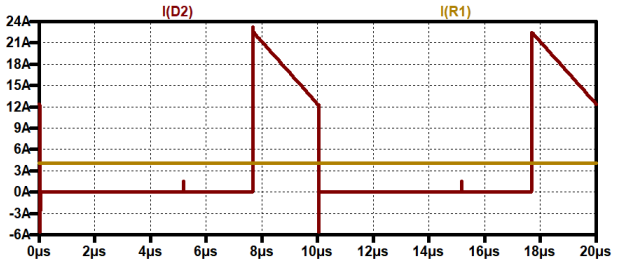

Fig. 16: Current through the second diode D2 (black) and the load (brown)

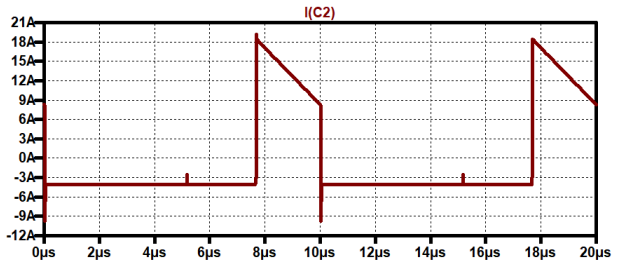

Fig. 17: Current through the output capacitor C2

The current through the output capacitor is zero in the mean. The time-axis is equal to the load current shown in Figure 17. During the modes M1 and M2 the load is supplied by the capacitor C2.

The current through the first capacitor C1 is shown in Figure 18. The current through L2 is flowing through the intermediate capacitor C1 during M1 in the negative direction. During M2 and M3 the current through L1 charges the capacitor C1. The mean value is zero in the steady state. The spikes are caused by the turn-off of the diodes.

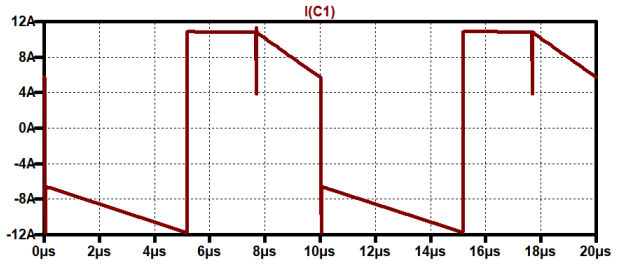

Fig. 18: Current through the intermediate capacitor C1

The voltage transformation ratio (3) has an interesting feature. When the duty cycle d2 of the second switch is constant, the voltage transformation ratio is a linear function of the duty cycle d1 of the first switch. This is shown in Figure 19.

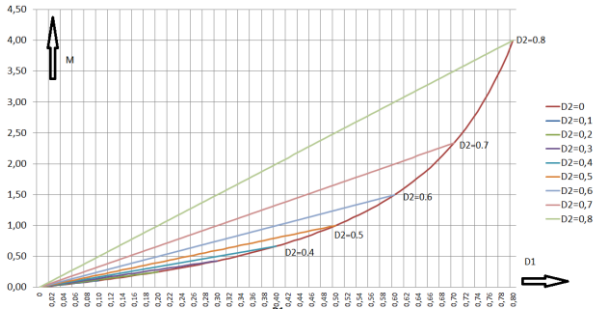

Fig. 19: Voltage transformation ratio with d1 as variable and d2 as parameter

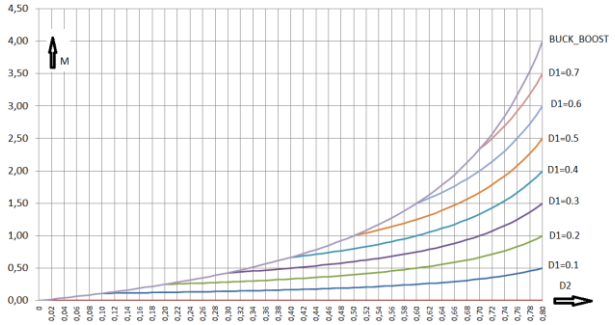

Fig. 20: Voltage transformation ratio with d2 as variable and d1 as parameter

Holding the duty cycle d1 of the first switch constant and using the duty cycle d2 of the second switch as a variable leads to a hyperbolic voltage transfer function as shown in Figure 20. Keep in mind that these curves are only valid for the continuous mode and in steady-state. So for low values very small load resistor would lead to these results.

3 Model of the Converter

In the model, the parasitic resistors of the coils and the capacitors are included. The on-resistors of the active switches describe the turned-on transistors. The conducting diodes are modeled by the differential resistor RD and a fixed voltage VD, representing the knee-voltage.

3.1 Mode M1: Both Switches S1, S2

Both switches are turned on but the diode D1 is reversed-biased so no current is flowing through the second switch. The equivalent circuit diagram is shown in Figure 21

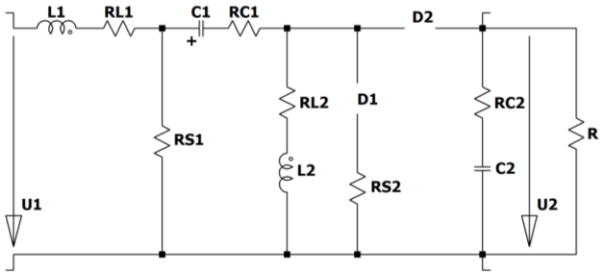

Fig. 21: Equivalent circuit diagram for mode M1

The state equations are

$$\frac{di_{L1}}{dt} = \frac{u_1 - R_{S1}(i_{L1} + i_{L2}) - R_{L1} i_{L1}}{L_1}, \tag{5}$$

$$\frac{di_{L2}}{dt} = \frac{-R_{S1}(i_{L1} + i_{L2}) + u_{C1} - R_{C1} i_{L2} - R_{L2} i_{L2}}{L_2}, \tag{6}$$

$$\frac{du_{C1}}{dt} = \frac{-i_{L2}}{C_1}, \tag{7}$$

$$\frac{du_{C2}}{dt} = \frac{-u_{C2}/(R + R_{C2})}{L_2}. \tag{8}$$

3.2 Mode M2: S1 has been Turned Off and therefore D1 has Turned On

Only during M2 current is flowing through S2 and through the diode D1. The equivalent circuit diagram is shown in Figure 22.

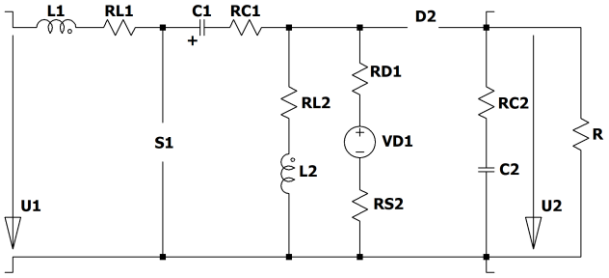

Fig. 22: Equivalent circuit diagram for mode M2

The state equations are:

$$\frac{di_{L1}}{dt} = \frac{u_1 - (R_{S2} + R_{D1})(i_{L1} + i_{L2}) - V_{D1} - (R_{C1} + R_{L2}) i_{L1} - u_{C1}}{L_1} \tag{9}$$

$$\frac{di_{L2}}{dt} = \frac{-(R_{S2} + R_{D1})(i_{L1} + i_{L2}) - V_{D1} - R_{L2} i_{L2}}{L_2} \tag{10}$$

$$\frac{du_{C1}}{dt} = \frac{i_{L1}}{C_2} \tag{11}$$

$$\frac{du_{C2}}{dt} = \frac{-u_{C2}/(R + R_{C2})}{L_2}. \tag{12}$$

3.3 Mode M3: Mode M3: The Second Switch S2 has been Turned Off and therefore the Second Diode D2 has Turned On

Now only the second diode D2 is conducting and feeding energy into the output. The equivalent circuit is shown in Figure 23.

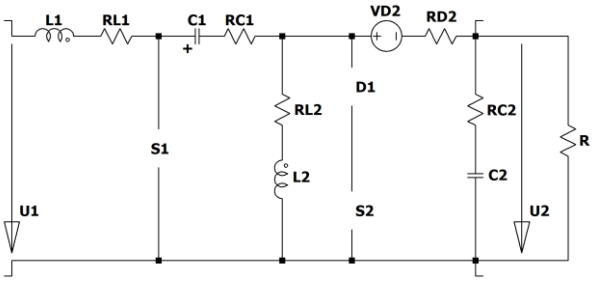

Fig. 23: Equivalent circuit diagram for mode M3

For the first state variable, one gets from Kirchhoff's voltage law (KVL)

$$\frac{di_{L1}}{dt}=\frac{\begin{array}{c}u_1-u_{C2}-R_{C2}i_{C2}-R_{D2}\left(i_{L1}+i_{L2}\right)-\\-V_{D2}-R_{C1}i_{L1}-u_{C1}-R_{L1}i_{L1}\end{array}}{L_1}. \tag{13}$$

The current through the capacitor C2 is neither a state variable nor an input variable. Therefore, it must be replaced. With Kirchhoff's current law (KCL) at the output and Ohm's law:

$$i_{L1}+i_{L2}=i_{C2}+\frac{R_{C2}i_{C2}+u_{C2}}{R} \tag{14}$$

one gets for the current through the output capacitor:

$$i_{C2}=\frac{R\left(i_{L1}+i_{L2}\right)-u_{C2}}{R+R_{C2}}. \tag{15}$$

Inserting into (13) leads to: (16)

$$\frac{di_{L1}}{dt}=\frac{\begin{array}{c}-i_{L1}\left(R_{C1}+R_{D2}+R_{L1}+R//R_{C2}\right)-\\i_{L2}\left(R_{D2}+R//R_{C2}\right)-u_{C1}-u_{C2}\left(\frac{R}{R+R_{C2}}\right)+u_1-V_{D2}\end{array}}{L_1}$$

For the second state variable, one obtains

$$\frac{di_{L2}}{dt}=\frac{\begin{array}{c}-i_{L1}\left(R_{D2}+R//R_{C2}\right)-i_{L2}\left(R_{D2}+R_{L2}+R//R_{C2}\right)\\-u_{C2}\left(\frac{R}{R+R_{C2}}\right)-V_{D2}\end{array}}{L_2} \tag{17}$$

The changes in the voltages across the capacitors are:

$$\frac{du_{C1}}{dt}=\frac{i_{L1}}{C_1} \tag{18}$$

$$\frac{du_{C2}}{dt}=\frac{R\left(i_{L1}+i_{L2}\right)-u_{C2}}{C_2\left(R+R_{C2}\right)}. \tag{19}$$

Weighting the set for M1 by d1, weighting the set for M2 by (d2-d1), and weighting the set for M3 by (1-d2) and combining them into the matrix form:

$$\frac{d}{dt}\underline{x}=\underline{\underline{A}}\,\underline{x}+\underline{\underline{B}}\,\underline{u}+\underline{V}, \tag{20}$$

and using the same parasitic parameters for the two electronic switches and the two diodes leads to the state matrix A, the input matrix B, and the constant vector V (given in the appendix).

3.4 Idealized Model

To get the idealized model, all parasitic resistors are set to zero and so is the forward voltage of the diodes leading to

$$\frac{d}{dt}\begin{pmatrix}i_{L1}\\i_{L2}\\u_{C1}\\u_{C2}\end{pmatrix}=\begin{bmatrix}0 & 0 & \frac{d_1-1}{L_1} & \frac{\left(d_2-1\right)}{L_1}\\0 & 0 & \frac{d_1}{L_2} & \frac{\left(d_2-1\right)}{L_2}\\\frac{1-d_1}{C_1} & -\frac{d_1}{C_1} & 0 & 0\\\frac{1-d_2}{C_2} & \frac{1-d_2}{C_2} & 0 & -\frac{1}{C_2R}\end{bmatrix}\begin{pmatrix}i_{L1}\\i_{L2}\\u_{C1}\\u_{C2}\end{pmatrix}+\begin{bmatrix}\frac{1}{L_1}\\0\\0\\0\end{bmatrix}\left(u_1\right). \tag{21}$$

3.4.1 Operation Point Connections

The operation point values are written in capital letters with an index of 0. From the equations of the derivations of the currents one gets:

$$\begin{bmatrix}D_{10}-1 & D_{20}-1\\D_{10} & D_{20}-1\end{bmatrix}\begin{pmatrix}U_{C10}\\U_{C20}\end{pmatrix}=\begin{pmatrix}-1\\0\end{pmatrix}U_{10} \tag{22}$$

leading to

$$\frac{U_{C10}}{U_{10}}=1 \tag{23}$$

and

$$\frac{U_{C20}}{U_{10}}=\frac{D_{10}}{1-D_{20}}. \tag{24}$$

The stationary voltage across the first capacitor must be equal to the input voltage. This can also be recognized by inspecting the loop U1, L1, C1, L2. In the steady state the voltages across the inductors must be zero in the mean. Therefore, the voltage across C1 must be equal to the input voltage.

From the third and the fourth lines of the matrix equation one gets the operating point currents:

$$\begin{bmatrix}1-D_{10} & -D_{10}\\1-D_{20} & 1-D_{20}\end{bmatrix}\begin{pmatrix}I_{L10}\\I_{L20}\end{pmatrix}=\begin{pmatrix}0\\1\end{pmatrix}I_{LOAD} \tag{25}$$

and for the currents in the steady state one gets:

$$\frac{I_{L10}}{I_{LOAD}} = \frac{D_{10}}{1-D_{20}} \tag{26}$$

$$\frac{I_{L20}}{I_{LOAD}} = \frac{1-D_{10}}{1-D_{20}} \; . \tag{27}$$

3.4.2 Linearization

Linearization around the operating point leads to:

$$\frac{d}{dt}\begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} = \begin{bmatrix} 0 & 0 & \frac{D_{10}-1}{L_1} & \frac{(D_{20}-1)}{L_1} \\ 0 & 0 & \frac{D_{10}}{L_2} & \frac{(D_{20}-1)}{L_2} \\ \frac{1-D_{10}}{C_1} & -\frac{D_{10}}{C_1} & 0 & 0 \\ \frac{1-D_{20}}{C_2} & \frac{1-D_{20}}{C_2} & 0 & -\frac{1}{C_2 R} \end{bmatrix} \begin{pmatrix} \hat{i}_{L1} \\ \hat{i}_{L2} \\ \hat{u}_{C1} \\ \hat{u}_{C2} \end{pmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{U_{C10}}{L_1} & \frac{U_{C20}}{L_1} \\ 0 & \frac{U_{C10}}{L_2} & \frac{U_{C20}}{L_2} \\ 0 & -\frac{I_{L10}+I_{L20}}{C_1} & 0 \\ 0 & 0 & -\frac{I_{L10}+I_{L20}}{C_2} \end{bmatrix} \begin{pmatrix} \hat{u}_1 \\ \hat{d}_1 \\ \hat{d}_2 \end{pmatrix} \tag{28}$$

The disturbances around the operating point are written in small letters with a roof on top.

3.4.3 Laplace Transformation

Laplace transformation of (28) leads to:

$$\begin{bmatrix} s & 0 & \frac{1-D_{10}}{L_1} & \frac{1-D_{20}}{L_1} \\ 0 & s & -\frac{D_{10}}{L_2} & \frac{1-D_{20}}{L_2} \\ \frac{D_{10}-1}{C_1} & \frac{D_{10}}{C_1} & s & 0 \\ \frac{D_{20}-1}{C_2} & \frac{D_{20}-1}{C_2} & 0 & s+\frac{1}{C_2 R} \end{bmatrix} \begin{pmatrix} I_{L1}(s) \\ I_{L2}(s) \\ U_{C1}(s) \\ U_{C2}(s) \end{pmatrix} = \begin{bmatrix} \frac{1}{L_1} & \frac{U_{C10}}{L_1} & \frac{U_{C20}}{L_1} \\ 0 & \frac{U_{C10}}{L_2} & \frac{U_{C20}}{L_2} \\ 0 & -\frac{I_{L10}+I_{L20}}{C_1} & 0 \\ 0 & 0 & -\frac{I_{L10}+I_{L20}}{C_2} \end{bmatrix} \begin{pmatrix} U_1(s) \\ D_1(s) \\ D_2(s) \end{pmatrix} \tag{29}$$

From this equation, twelve transfer functions can be calculated which describe the system around the operating point. Most important are the transfer functions of the output voltage (the voltage across the output capacitor) in dependence on the duty cycles. The transfer function between the output voltage and the input voltage is important to describe the disturbance caused by changes in the input voltage. All twelve transfer functions have the same denominator

3.4.4 Transfer Functions

The transfer functions can be calculated with the help of Crammer's law. The parameters of the converter for drawing the Bode plots are (with a tolerance of 10 % for the second coil and the second capacitor) L1= 47 µH, L2=51.7 µH, C1= 330 µF, C2=363 µF, U1=48 V, D10=0.5, D20=0.75, IL10=IL20=8 A, R=25 Ω. For the denominator one gets:

$$\text{Den} = s^4 + \frac{1}{C_2 R}s^3 + s^2\left[\frac{(1-D_{10})^2}{C_1 L_1} + \frac{D_{10}^2}{C_1 L_2} + \frac{(1-D_{20})^2}{C_2 L_1} + \frac{(1-D_{20})^2}{C_2 L_2}\right] + s\frac{1}{C_1 C_2 R}\left[\frac{(1-D_{10})^2}{L_1} + \frac{D_{10}^2}{L_2}\right] + \left[\frac{(1-D_{20})^2}{C_1 C_2 L_1 L_2}\right] \tag{30}$$

For the numerator of the transfer function between the output voltage and the duty cycle of switch S1 one gets:

$$\text{Num\_U2\_D1} = s^2\frac{(1-D_{20})U_{10}}{C_2}\frac{L_1+L_2}{L_1 L_2} + s\frac{I_{L10}+I_{L20}}{C_1 C_2}\left[\frac{(1-D_{10})}{L_1} - \frac{D_{10}}{L_2}\right] + \frac{(1-D_{20})U_{C10}}{C_1 C_2 L_1 L_2} \; . \tag{31}$$

The Bode plot is shown in Figure 24.

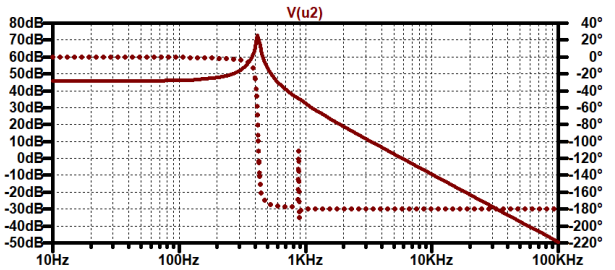

Fig. 24: RLT SEPIC, output voltage referred to the duty cycle of the first switch: Bode plot (solid line: gain response, dotted line: phase response)

The transfer function describes a phase-minimum system. The zeroes are on the left and compensate for the phase shift of two poles. The second complex pole pair is near to the complex zero which is on the left side of the complex plane.

For the numerator of the transfer function between the output voltage and the duty cycle of switch S2 one gets:

$$\text{Num\_U2\_D2} = s^2 \frac{(1-D_{20})U_{C20}}{C_2}\frac{L_1+L_2}{L_1L_2} - s\frac{I_{L10}+I_{L20}}{C_1C_2}\left[\frac{(1-D_{10})^2}{L_1}+\frac{D_{10}^2}{L_2}\right]+\frac{(1-D_{20})U_{C20}}{C_1C_2L_1L_2} \quad (32)$$

The Bode plot is shown in Figure 25. The complex zero is situated on the left side, and the real zero is on the right side of the complex plane. The phase shift is therefore -270° for high frequencies. One complex pole is compensated by the complex zero.

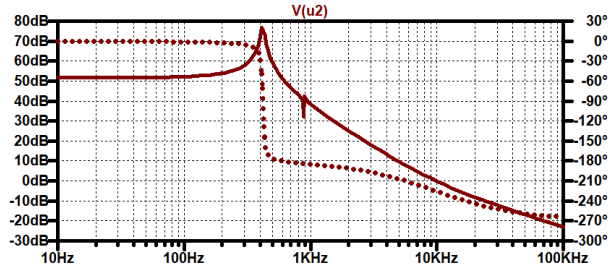

Fig. 25: RLT SEPIC, output voltage referred to the duty cycle of the second switch: Bode plot (solid line: gain response, dotted line: phase response)

For the numerator of the transfer function between the output voltage and the input voltage one gets

$$\text{Num\_U2\_U1} = \frac{D_{10}(1-D_{20})}{C_1C_2L_1L_2} \quad (33)$$

The Bode plot is shown in Figure 26. This transfer function is again a phase-minimum system. The two resonant pole pairs can be clearly seen.

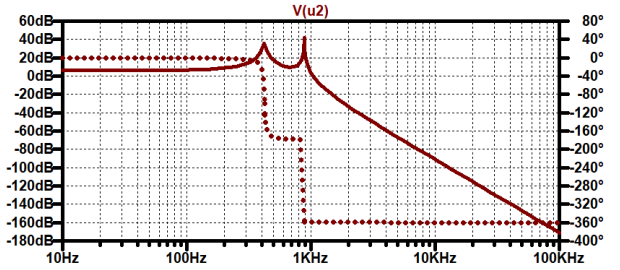

Fig. 26: RLT SEPIC, output voltage referred to the input voltage: Bode plot (solid line: gain response, dotted line: phase response)

4 Start-up and Short-Circuit

4.1 Ideal Inrush

Connecting the converter to a very stiff input voltage, e.g. car batteries, a large inrush current occurs. To demonstrate this a simulation is shown in Figure 27. No load is applied to the converter. The current through L1 is larger in the first half period because D2 turns on, too. The ringing is damped by the parasitic resistors. The currents go down to zero, and the voltage across C1 terminates at the value of the input voltage. For the simulation, the inductance values are taken constant. In reality, the coils will saturate and the current will even be larger. When the load is applied, the output returns to zero because the output capacitor is discharged by the load. The peak value of the resonant current is caused by the input voltage multiplied by the square root of the value of C1 divided by the sum of the inductors L1 and L2.

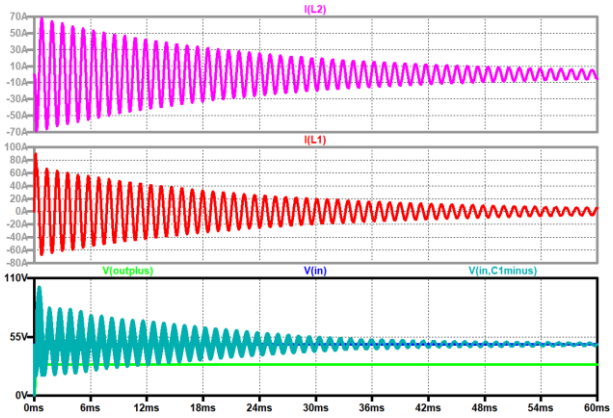

Fig. 27: Ideal inrush with no load, up to down: current through the second coil L2 (violet); current through the first coil L1 (red); voltage across the intermediate capacitor (turquoise), input voltage (blue), output voltage (green)

4.2 Start-up of the Converter with Additional Pre-Stage

To avoid the inrush current, an additional pre-stage consisting of an electronic switch SIN and a diode DIN can be connected between the input source and the converter. The circuit diagram is shown in Figure 28.

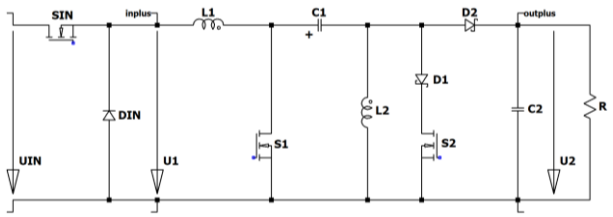

Fig. 28: RLT SEPIC with additional pre-stage

The circuit starts with a pwm signal beginning from zero up to the continuous on-time of the additional switch SIN. Figure 29 shows a simulation of the currents through the coils and the voltage across the intermediate capacitor. Within about 23 ms the switch SIN is completely turned on.

When the input switch is continuously on, a small damped ringing between the two inductors and the first capacitor C1 occurs. In the case of an error, the pre-stage can also be used as an electronic fuse. To avoid an overvoltage caused by the parasitic inductance between the pre-stage and the input source a pulse capacitor should be connected between the drain of SIN and the anode of DIN.

In the case of no load and constant clocking the voltage at the output increases and can lead to dangerous rates. The controller must stop the clocking. When the input current exceeds a limit, the electronic fuse can stop this, too.

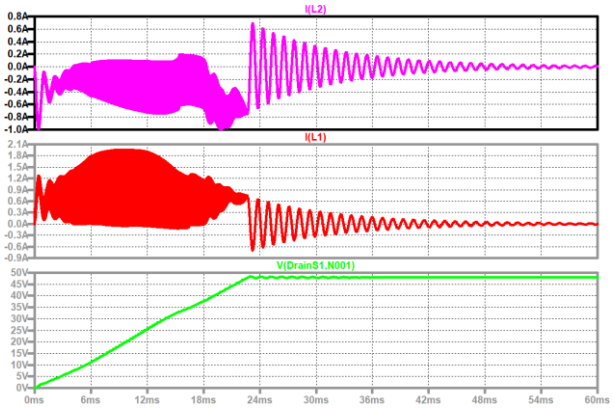

Fig. 29: Start-up of the pre-stage to avoid the inrush, up to down: current through the second coil L2 (violet); current through the first coil L1 (red); voltage across the intermediate capacitor (green)

4.3 Short Circuit at the Load Side

Using the converter with the pre-stage, the switch SIN can be used as an electronic fuse and the converter can be disconnected from the input source.

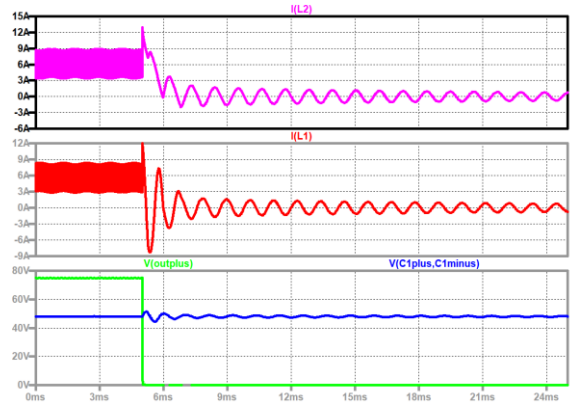

Fig. 30: Short circuit at the output, up to down: current through the second coil L2 (violet); current through the first coil L1 (red); output voltage (green), the voltage across the first capacitor C1 (blue)

Using the converter without pre-stage, an error on the load side leading to an output short circuit will engender a large current on the input side. When the error is detected (e.g. by measuring the input current which increases over a limit, a comparator can produce an error signal), the electronic switches are blocked. The currents go down and reach zero. A damped ringing occurs. This is shown in Figure 30. The intermediate capacitor blocks the input current.

5 Modifications

5.1 Floating Two-Stage Reduced-Loss Tristate SEPIC

Floating two-stage converters is an interesting concept for combining two converters. The references [6], [7], [8], [9] show examples. The circuit diagram of the two-stage RLT converter is shown in Figure 31.

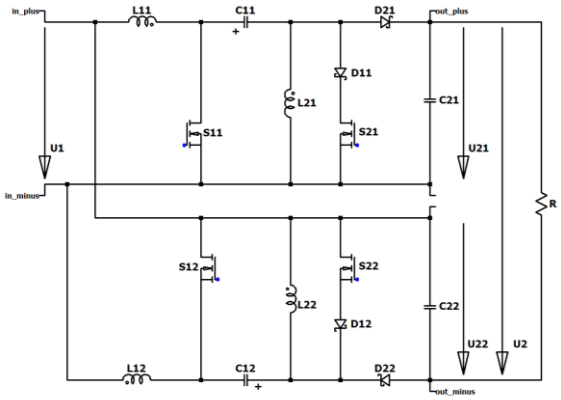

Fig. 31: Floating two-stage RLT SEPIC

The two converters work at the same input voltage, and the output voltage is the sum of the output voltages of the two converter stages minus the input voltage:

$$U_2 = U_{21} - U_1 + U_{22} . \tag{34}$$

For the tristate converter with two equally controlled stages, this leads to"

$$U_2 = \left(\frac{2d_1}{1-d_2} - 1 \right) U_1 = \frac{2d_1 + d_2 - 1}{1-d_2} U_1 . \tag{35}$$

The inequations:

$$2d_1 + d_2 > 1 , \qquad d_2 \geq d_1 \tag{36}$$

must be valid.

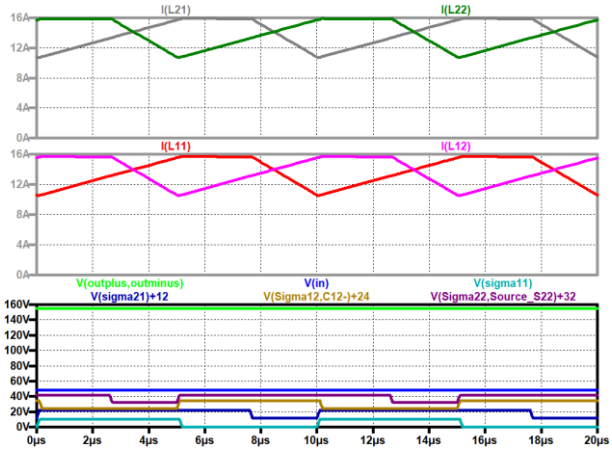

Fig. 32: Floating two-stage reduced loss tristate SEPIC, up to down: current through the second coils of stage 1 (grey), of stage 2 (dark green); current through the first coils of stage 1 (red), of stage 2 (violet); output voltage (green), input voltage (blue), the control signal of switch S22 of stage 2 (dark violet, shifted), the control signal of switch S12 of stage 2 (brown, shifted), the control signal of switch S21 of stage 1 (dark blue, shifted), the control signal of switch S11 of stage 1 (turquoise)

To increase (double) the frequency of the input current, the control signals are shifted by 180°. Figure 32 shows the current through the second coils of stage 1 and of stage 2, the currents through the first coils of stage 1 and of stage 2, the output voltage, the input voltage, the control signal of switch S2 from stage 2, the control signal of switch S1 from stage 2, the control signal of switch S2 from stage 1, and the control signal of switch S1 from stage 1.

5.2 Interleaved Two-Stage Reduced-Loss Tristate SEPIC

In the interleaved concept the converters are connected in parallel. Besides many others the references [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], treat this concept.

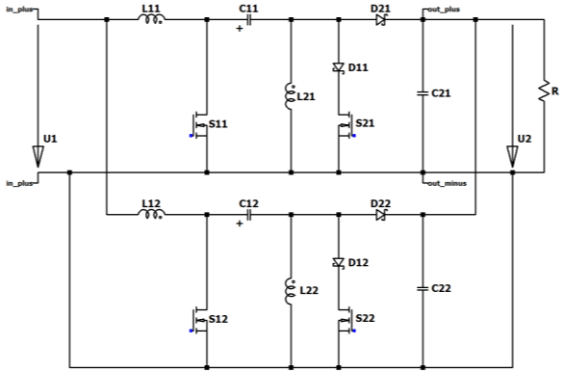

Fig. 33: Interleaved two-stage RLT SEPIC

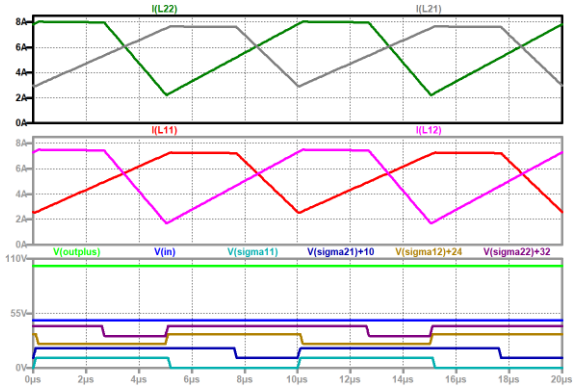

Fig. 34: Interleaved two-stage reduced-loss tristate SEPIC, up to down: current through the second coils of stage 1 (grey), of stage 2 (dark green); current through the first coils of stage 1 (red), of stage 2 (violet); output voltage (green), input voltage (blue), control signal of switch S22 of stage 2 (dark violet, shifted), control signal of switch S12 of stage 2 (brown, shifted), control signal of switch S21 of stage 1 (dark blue, shifted), control signal of switch S11 of stage 1 (turquoise)

The converter stages are supplied by the same input source and feed the same load. To increase the frequency of the input current, the control signals are shifted by 360° divided by the number of stages n. Figure 33 shows two converter stages connected in parallel. In Figure 34 the signals in the steady state are shown.

5.3 Modified Reduced-Loss Tristate SEPIC

The modification concerns the position of the second capacitor, [20]. Normally the capacitor is connected between the output terminals. Here now it is connected between the positive input and the positive output terminals. The direction of the voltage changes between the step-down and the step-up operation. Therefore, C2 cannot be an electrolytic capacitor. This must not be a disadvantage at higher frequencies, and it is necessary for systems built to last for a long lifetime. Figure 35 shows the circuit diagram, and the plus pole is marked for a step-up operation.

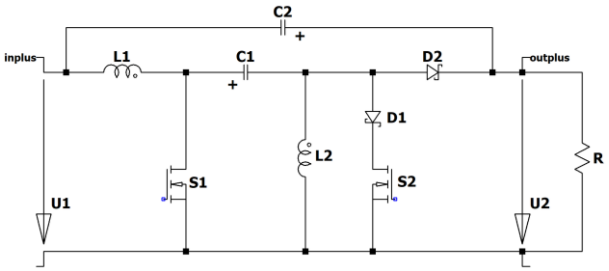

Fig. 35: Modified reduced-loss tristate SEPIC in the boost operation

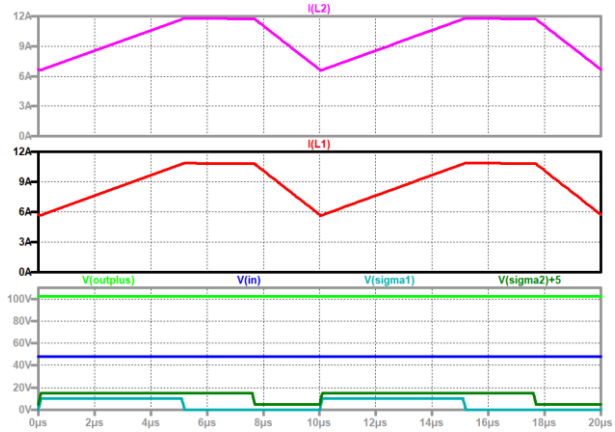

Fig. 36: Modified reduced-loss tristate SEPIC, up to down: current through the second coil L2 (violet); current through the first coil L1 (red); output voltage (green), input voltage (blue), control signal of switch S2 (dark green, shifted), control signal of switch S1 (turquoise)

Figure 36 shows the current through the second coil L2, the current through the first coil L1, the output voltage, the input voltage, and the control signals of the electronic switches.

6 Conclusion

The converter has several interesting features

- Voltage transformation ratio with two degrees of freedom
- Linearization of the voltage transformation ratio
- Avoiding a non-phase minimum system
- Continuous input current
- Both electronic switches are low-side ones
- Short circuit proved
- Improved efficiency

The converter can be used as switched-mode power supply and as a driving stage for a DC motor. It can be applied among other cars and in renewable energy applications.

References:

[1] (text in German) F. Zach, *Leistungselektronik*, Frankfurt: Springer, 6th edition 2022.

[2] N. Mohan, T. Undeland, & W. Robbins, *Power Electronics, Converters, Applications and Design*, New York: W. P. John Wiley & Sons.

[3] Y. Rozanov, S. Ryvkin, E. Chaplygin, P. Voronin, *Power Electronics Basics*, CRC Press.

[4] Felix A. Himmelstoss, Tristate Converters, WSEAS Transactions on Power Systems, vol. 18, pp. 259-269, 2023, DOI: 10.37394/232016.2023.18.27.

[5] K. Viswanathan, R. Oruganti and D. Srinivasan, A novel tri-state boost converter with fast dynamics, *IEEE Transactions on Power Electronics*, vol. 17, no. 5, pp. 677-683, Sept. 2002, DOI: 10.1109/TPEL.2002.802197.

[6] 1 M. G. Simões, C. L. Lute, A. N. Alsaleem, D. I. Brandao and J. A. Pomilio, Bidirectional floating interleaved buck-boost DC-DC converter applied to residential PV power systems, *2015 Clemson University Power Systems Conference (PSC)*, Clemson, SC, USA, 2015, pp. 1-8, DOI: 10.1109/PSC.2015.7101675.

[7] 2 D. Coutellier, V. G. Agelidis and S. Choi, Experimental verification of floating-output interleaved-input DC-DC high-gain transformer-less converter topologies, *2008 IEEE Power Electronics Specialists Conference*, Rhodes, Greece, 2008, pp. 562-568, DOI: 10.1109/PESC.2008.4591989.

[8] 4 A. N. Le, D. T. Nguyen, Q. D. Phan, P. H. Truong, M. D. Pham and C. V. Nguyen, 4-Phase Floating Buck Converter Based on Series Capacitor Structure, *2023 International Conference on System Science and Engineering (ICSSE)*, Ho Chi Minh, Vietnam, 2023, pp. 108-113, DOI: 10.1109/ICSSE58758.2023.10227149.

[9] 8 Y. Huangfu, L. Guo, R. Ma and F. Gao, An Advanced Robust Noise Suppression Control of Bidirectional DC–DC Converter for Fuel Cell Electric Vehicle, *IEEE Transactions on Transportation Electrification*, vol. 5, no. 4, pp. 1268-1278, Dec. 2019, DOI: 10.1109/TTE.2019.2943895.

[10] K. A. Singh, A. Prajapati and K. Chaudhary, High-Gain Compact Interleaved Boost Converter With Reduced Voltage Stress for PV Application, *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 10, no. 4, pp. 4763-4770, Aug. 2022, DOI: 10.1109/JESTPE.2021.3120802.

[11] F. S. Alargt, A. S. Ashur and A. H. Kharaz, Multiphase Interleaved SEPIC Converter Using ADM Control loop Suitable for Hybrid Energy Source Integration, *2022 Second International Conference on Sustainable*

Mobility Applications, Renewables and Technology (SMART), Cassino, Italy, 2022, pp. 1-8, DOI: 10.1109/SMART55236.2022.9990097.

[12] S. Kollati, D. R. Kishore, K. Mounika, M. S. B. R. V. Ajay and O. N. N. M. Krishna, Firefly Optimized Interleaved Sepic Converter for EV Charging Applications, *2024 1st International Conference on Innovative Sustainable Technologies for Energy, Mechatronics, and Smart Systems (ISTEMS)*, Dehradun, India, 2024, pp. 1-6, DOI: 10.1109/ISTEMS60181.2024.10560235.

[13] Prajof P. and V. Agarwal, Novel boost-SEPIC type interleaved dc-dc converter for low-voltage bipolar dc microgrid-tied solar pv applications, *2015 IEEE 42nd Photovoltaic Specialist Conference (PVSC)*, New Orleans, LA, USA, 2015, pp. 1-6, DOI: 10.1109/PVSC.2015.7356272

[14] A. Yadav and A. Verma, Sepic DC–DC Converter: Review of Different Voltage Boosting Techniques and Applications, *2020 2nd International Conference on Innovative Mechanisms for Industry Applications (ICIMIA)*, Bangalore, India, 2020, pp. 733-739, DOI: 10.1109/ICIMIA48430.2020.9074897.

[15] S. Prasad, S. Mandal, P. Prabhakaran and A. D. D, A Novel Input-Parallel Output-Series SEPIC-Cuk Converter for Bipolar Voltage Balancing, *2023 IEEE 2nd Industrial Electronics Society Annual On-Line Conference (ONCON)*, SC, USA, 2023, pp. 1-6, DOI: 10.1109/ONCON60463.2023.10430951.

[16] U. V V, S. George and P. J. Paul, A Comprehensive study on Traditional and Derived SEPIC Topologies, *2022 Third International Conference on Intelligent Computing Instrumentation and Control Technologies (ICICICT)*, Kannur, India, 2022, pp. 1471-1476, DOI: 10.1109/ICICICT54557.2022.9917661.,

[17] P. Prabhakaran and V. Agarwal, Novel Boost-SEPIC Type Interleaved DC–DC Converter for Mitigation of Voltage Imbalance in a Low-Voltage Bipolar DC Microgrid, *IEEE Transactions on Industrial Electronics*, vol. 67, no. 8, pp. 6494-6504, Aug. 2020, DOI: 10.1109/TIE.2019.2939991.

[18] E. D. Aranda, S. P. Litrán and M. B. F. Prieto, Combination of interleaved single-input multiple-output DC-DC converters, *CSEE Journal of Power and Energy Systems*, vol. 8, no. 1, pp. 132-142, Jan. 2022, DOI: 10.17775/CSEEJPES.2020.00300.

[19] M. Karunakaran, R. Sridevi, V. Suresh and V. K. Dinesh Prabu, Active Synchronous Rectifier based Parallel Interleaved Converter for EV Battery Charging, 2024 7th International Conference on Circuit Power and Computing Technologies (ICCPCT), Kollam, India, 2024, pp. 1697-1702, DOI: 10.1109/ICCPCT61902.2024.10672840.

[20] F. A. Himmelstoss and J. V. Gragger, Tristate Modified Boost Converter, PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2024, pp. 2099-2106, DOI: 10.30420/566262297.

Contribution of Individual Authors to the Creation of a Scientific Article (Ghostwriting Policy)

The author contributed to the present research, in all stages from the formulation of the problem to the final findings and solution.

Sources of Funding for Research Presented in a Scientific Article or Scientific Article Itself

No funding was received for conducting this study.

Conflict of Interest

The author has no conflicts of interest to declare.

APPENDIX

The parallel connection between the load R and the parasitic resistor RC2 of the output capacitor C2 is abbreviated by R//RC2 in the state matrix (A3).
The input matrix (A1, transposed) becomes:

$$B^T = \begin{bmatrix} \frac{1}{L_1} & 0 & 0 & 0 \end{bmatrix}. \quad \text{(A1)}$$

The fixed forward voltages of the diodes are written in the additional vector V (A2)

$$V = \begin{pmatrix} \frac{(1-d_1)V_D}{L_1} \\ \frac{(1-d_1)V_D}{L_2} \\ 0 \\ 0 \end{pmatrix}. \quad \text{(A2)}$$

$$\begin{bmatrix} -\frac{(R_{C1}+R_D)(1-d_1)+R_{L1}+R_S d_2+R//R_{C2}(1-d_2)}{L_1} & -\frac{R_D(1-d_1)+R_S d_2+R//R_{C2}(1-d_2)}{L_1} & \frac{d_1-1}{L_1} & \frac{(d_2-1)R}{L_1(R+R_{C2})} \\ -\frac{R_D(1-d_1)+R_S d_2+R//R_{C2}(1-d_2)}{L_2} & -\frac{R_{C1}d_1+R_{L2}+R_S d_2+R//R_{C2}(1-d_2)}{L_2} & \frac{d_1}{L_2} & \frac{(d_2-1)R}{L_2(R+R_{C2})} \\ \frac{1-d_1}{C_1} & -\frac{d_1}{C_1} & 0 & 0 \\ \frac{R(1-d_2)}{C_2(R+R_{C2})} & \frac{R(1-d_2)}{C_2(R+R_{C2})} & 0 & -\frac{1}{C_2(R+R_{C2})} \end{bmatrix} \quad \text{(A3)}$$

Using abbreviations for the elements of the state matrix A and for the input matrix B, one gets the denominator of the transfer functions:

$$Den = s^4 - A_{44}s^3 - (A_{14}A_{41} + A_{24}A_{42} + A_{13}A_{31} + A_{23}A_{32})s^2 + A_{44}(A_{13}A_{31} + A_{23}A_{32})s + A_{13}A_{24}A_{31}A_{42} - - A_{14}A_{23}A_{31}A_{42} - A_{13}A_{24}A_{32}A_{41} + A_{14}A_{23}A_{32}A_{41}. \quad \text{(A4)}$$

The numerator of the transfer function between the output voltage and the duty cycle of switch S1 is given by:

$$\begin{aligned} \text{NUMU2D1} = {} & (A_{41}B_{12} + A_{42}B_{22})s^2 \\ & + (A_{13}A_{41}B_{32} + A_{23}A_{42}B_{32} +)s + \\ & (A_{13}A_{32}A_{41}B_{22} - A_{23}A_{32}A_{41}B_{12} - \\ & - A_{13}A_{31}A_{42}B_{22} + A_{23}A_{31}A_{42}B_{12}) \end{aligned} \quad \text{(A5)}$$

The numerator of the transfer function between the output voltage and the duty cycle of switch S2 is given by:

$$\begin{aligned} \text{NUMU2D2} = {} & B_{24}s^3 + (A_{41}B_{13} - A_{42}B_{23})s^2 \\ & - (A_{23}A_{32}B_{43} + A_{13}A_{31}B_{43})s + \\ & (A_{13}A_{32}A_{41}B_{23} - A_{23}A_{32}A_{41}B_{13} - A_{13}A_{31}A_{42}B_{23} + \\ & A_{23}A_{31}A_{42}B_{13}) \end{aligned} \quad \text{(A6)}$$

The numerator of the transfer function between the output voltage and the input voltage is given by:

$$\text{NUMU2U1} = +A_{23}A_{31}A_{42}B_{11} - A_{23}A_{32}A_{41}B_{11}. \quad \text{(A7)}$$

Improvement of the efficiency

The improvement of the efficiency is shown by a simulation. Figure A shows the current through the second switch for the normal tristate converter and for the reduced loss tristate converter.

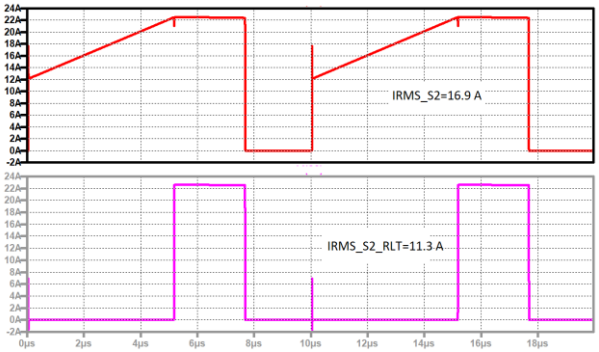

Fig. A: Current through the second switch, up to down: normal tristate converter; reduced loss tristate converter

The losses at all components are equal between the traditional tristate converter and the one with reduced losses, except the losses across S2. Figure shows the currents through these devices for both concepts. The rms value is also given. Corresponding to the normal tristate converter, the reduction of the rms value can be given by:

$$\frac{I_{RMS,T} - I_{RMS,RLT}}{I_{RMS,RLT}} = 33\,\%. \quad \text{(A8)}$$

The losses are therefore reduced with equal transistors by:

$$\frac{I^2_{RMS,T} - I^2_{RMS,RLT}}{I^2_{RMS,RLT}} = 55\,\%. \quad \text{(A9)}$$

In this case, this leads to an improved overall efficiency by 1 %